

Before hitting the “Run Script” button

Step 6: PLLs

Update red fields to control the DPLL characteristics.

The transfer function and error function allowed peaking can be left at the default values, if there is no application requirement specifying these values.

Running the script will yield attenuation values (in dB) for the specified transfer/error function offsets.

DPLL LBW (Hz)

DPLL Transfer Function Allowed Peaking (dB)

DPLL Error Function Allowed Peaking (dB)

DCO Step Size (ppb)

Transfer Function Attenuation

Error Function Attenuation

DPLL1

VCO1 Freq. (MHz)

5000.0

Range: 4800e6 to 5350e6

☐ Disable Fastlock

Target Actual

10 10.107

0.1 —

1 —

0 0

Offset (Hz)

100 -27.12 dB

100 0.35 dB

DPLL2

VCO2 Freq. (MHz)

5625.0

Range: 5595e6 to 5950e6

☐ Disable Fastlock

Target Actual

10 10.143

0.1 —

1 —

10366.60 10366.6036356

100 -25.72 dB

100 0.41 dB

DPLL3

VCO3 Freq. (MHz)

2500.0

Range: 2500 MHz +/- 100 ppm

☐ Disable Fastlock

Target Actual

10 10.107

0.1 —

1 —

0 0

100 -27.12 dB

100 0.35 dB

Step 7: Run Script

When red fields are changed, click **Calculate DPLL Settings** to generate updated DPLL settings for selected DPLLs below.

☐ Calc DPLL1

☐ Calc DPLL2

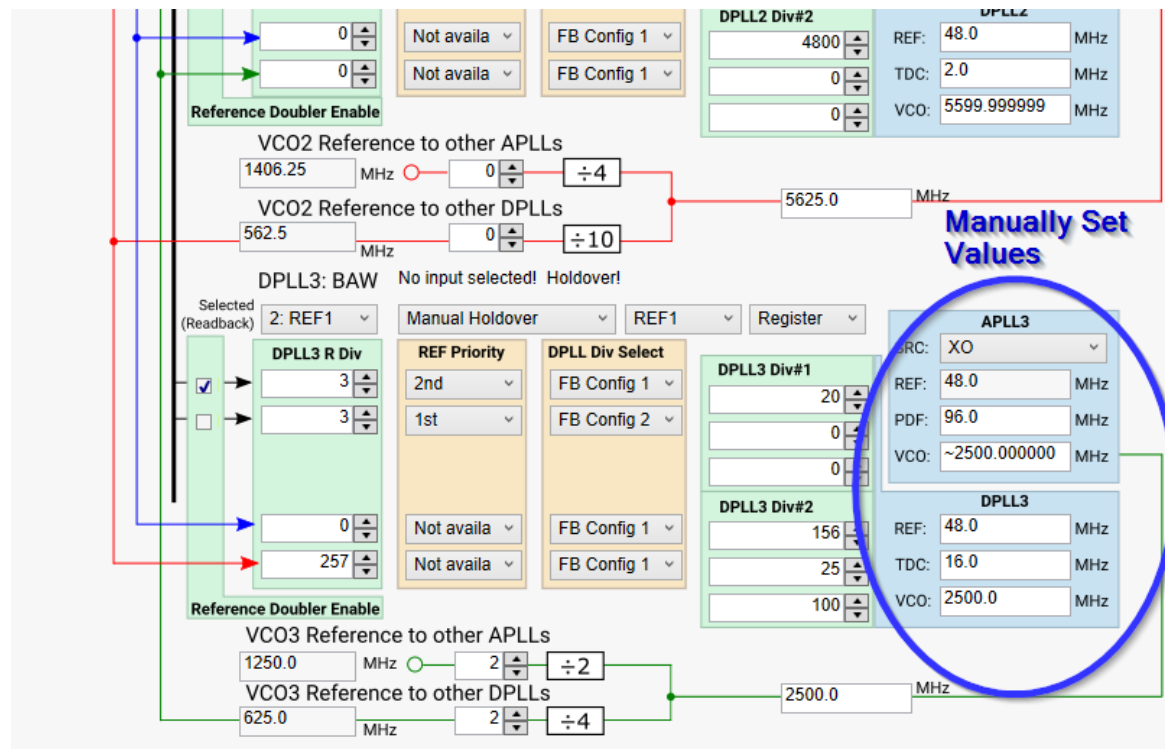
☒ Calc DPLL3

Run Script

☐ Bypass run script warning

If ZDM mode is being used for a DPLL, re-run step 5

"Assign Selected VCO Settings to Device" and "Apply Output Clock Settings to Device" to set DPLL dividers for ZDM.



After hitting “Run Script” button

Step 6: PLLs

Update red fields to control the DPLL characteristics.

The transfer function and error function allowed peaking can be left at the default values, if there is no application requirement specifying these values.

Running the script will yield attenuation values (in dB) for the specified transfer/error function offsets.

DPLL LBW (Hz)

DPLL Transfer Function Allowed Peaking (dB)

DPLL Error Function Allowed Peaking (dB)

DCO Step Size (ppb)

Transfer Function Attenuation

Error Function Attenuation

DPLL1

VCO1 Freq. (MHz)

5000.0

Range: 4800e6 to 5350e6

☐ Disable Fastlock

Target	Actual
10	10.107

0.1

1

0

Offset (Hz)

100 -27.12 dB

100 0.35 dB

DPLL2

VCO2 Freq. (MHz)

8437.5

Range: 5595e6 to 5950e6

☐ Disable Fastlock

Target	Actual
10	10.143

0.1

1

10366.60

10366.6036356

100 -25.72 dB

100 0.41 dB

DPLL3

VCO3 Freq. (MHz)

3750.0

Range: 2500 MHz +/- 100 ppm

☐ Disable Fastlock

Target	Actual
10	10.102

0.1

1

0

100 -27.45 dB

100 0.34 dB

Step 7: Run Script

When red fields are changed, click **Calculate DPLL Settings** to generate updated DPLL settings for selected DPLLs below.

☐ Calc DPLL1

☐ Calc DPLL2

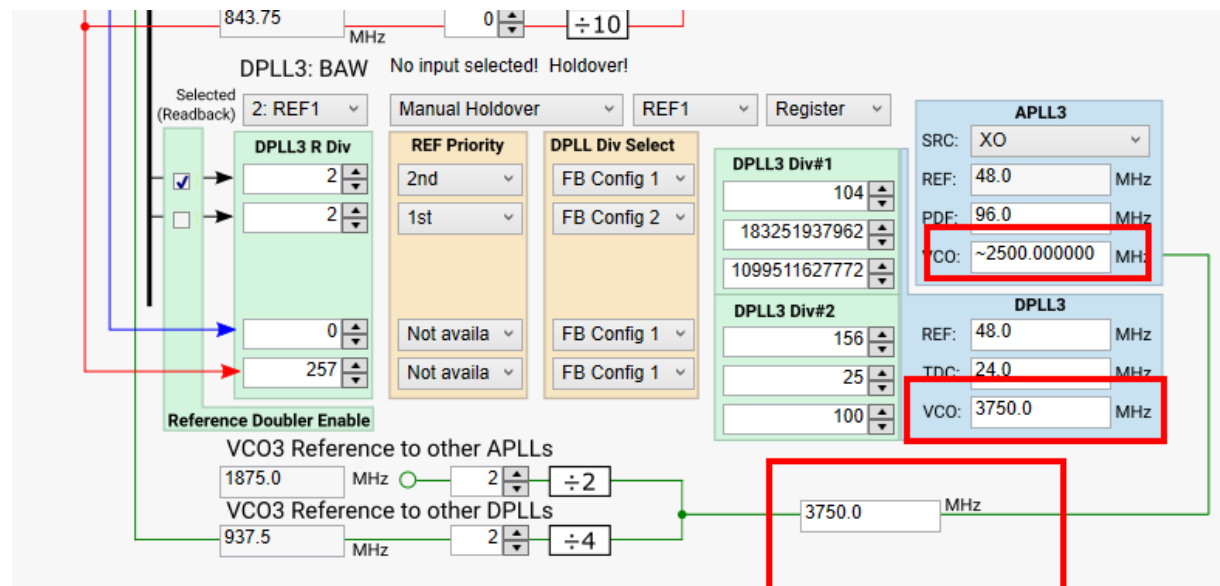
☒ Calc DPLL3

Run Script

☐ Bypass run script warning

If ZDM mode is being used for a DPLL, re-run step 5

"Assign Selected VCO Settings to Device" and "Apply Output Clock Settings to Device" to set DPLL dividers for ZDM.



APLL3, BAW, 2500 MHz $\pm$ 100 ppm

