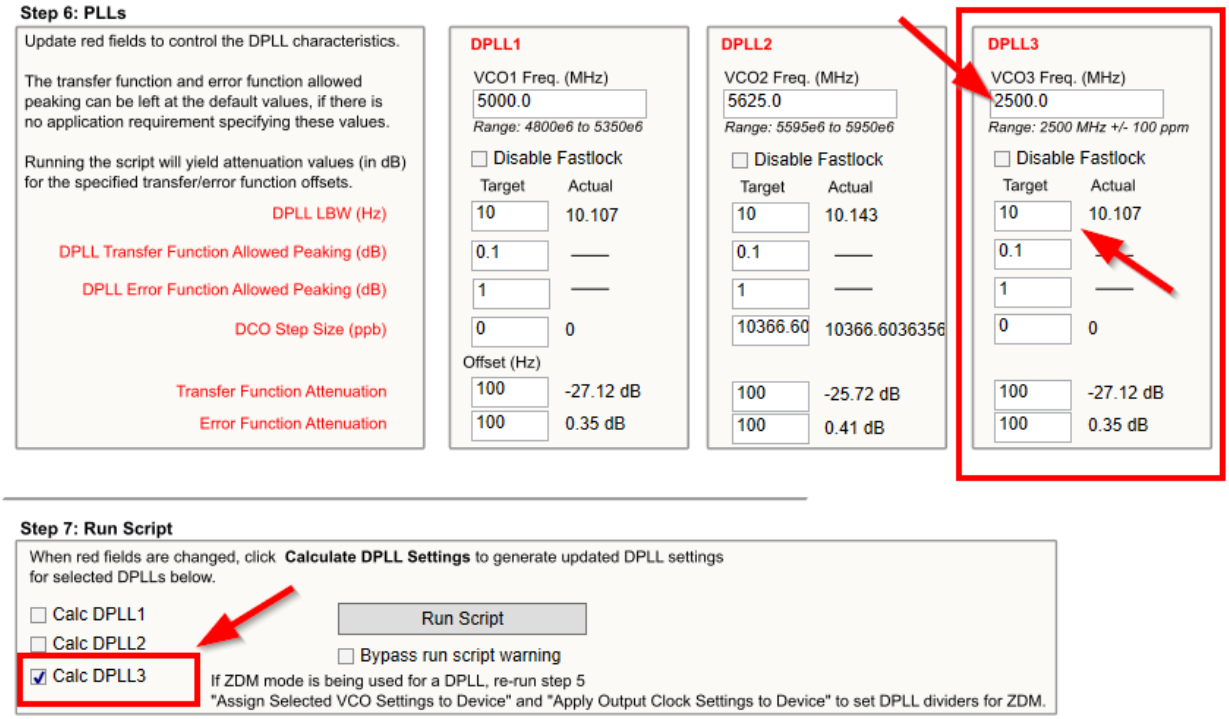
Before hitting the “Run Script” button



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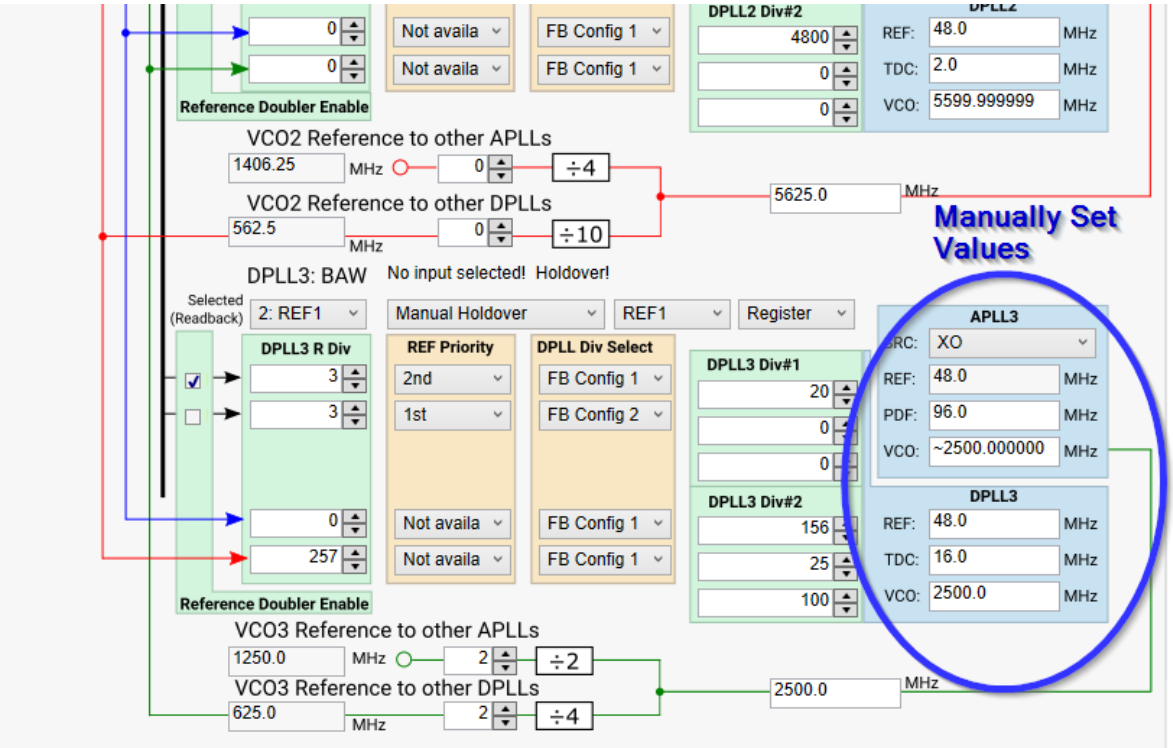
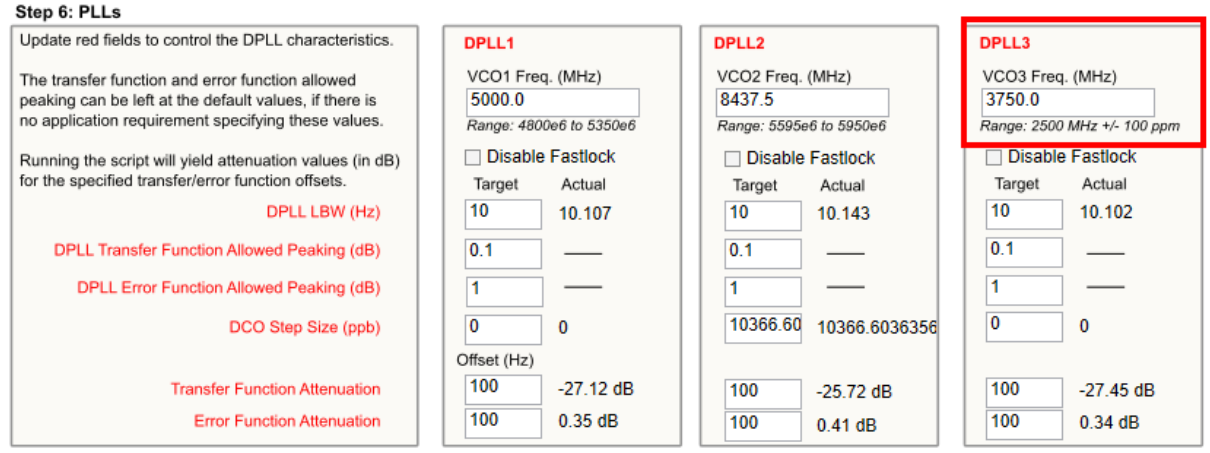
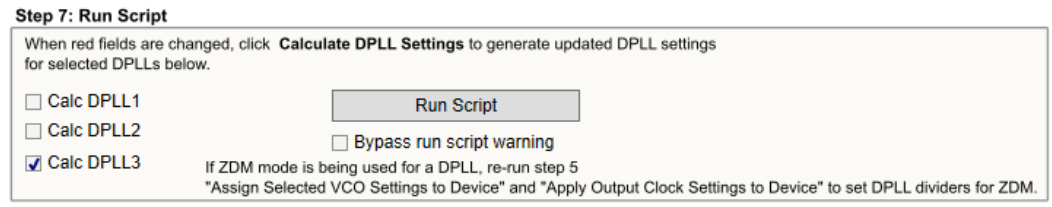
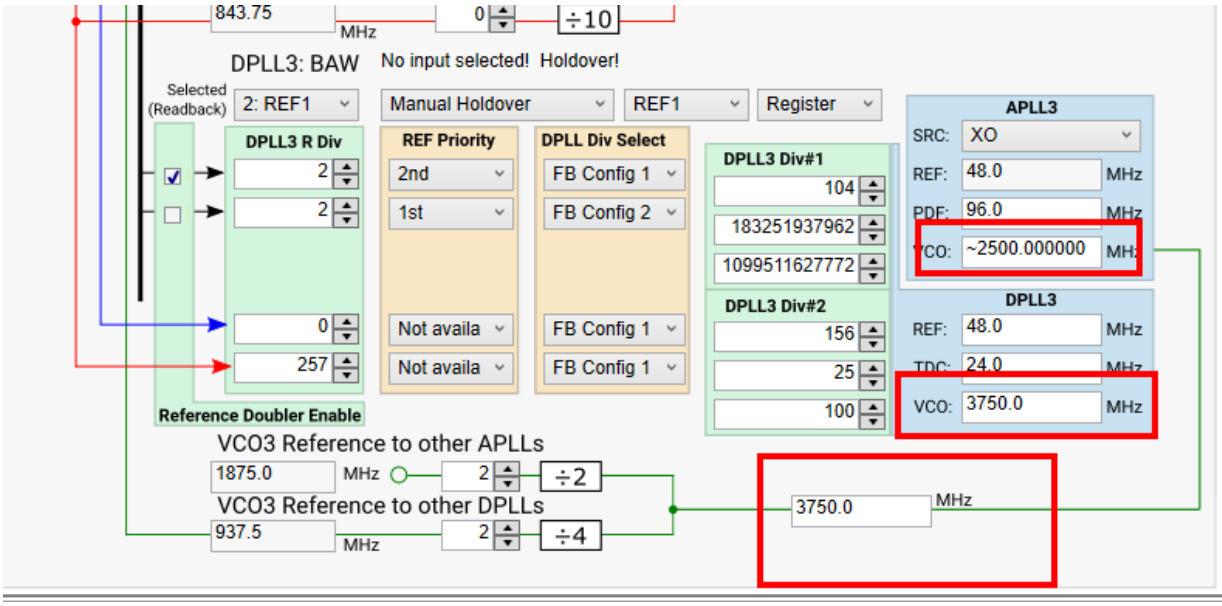
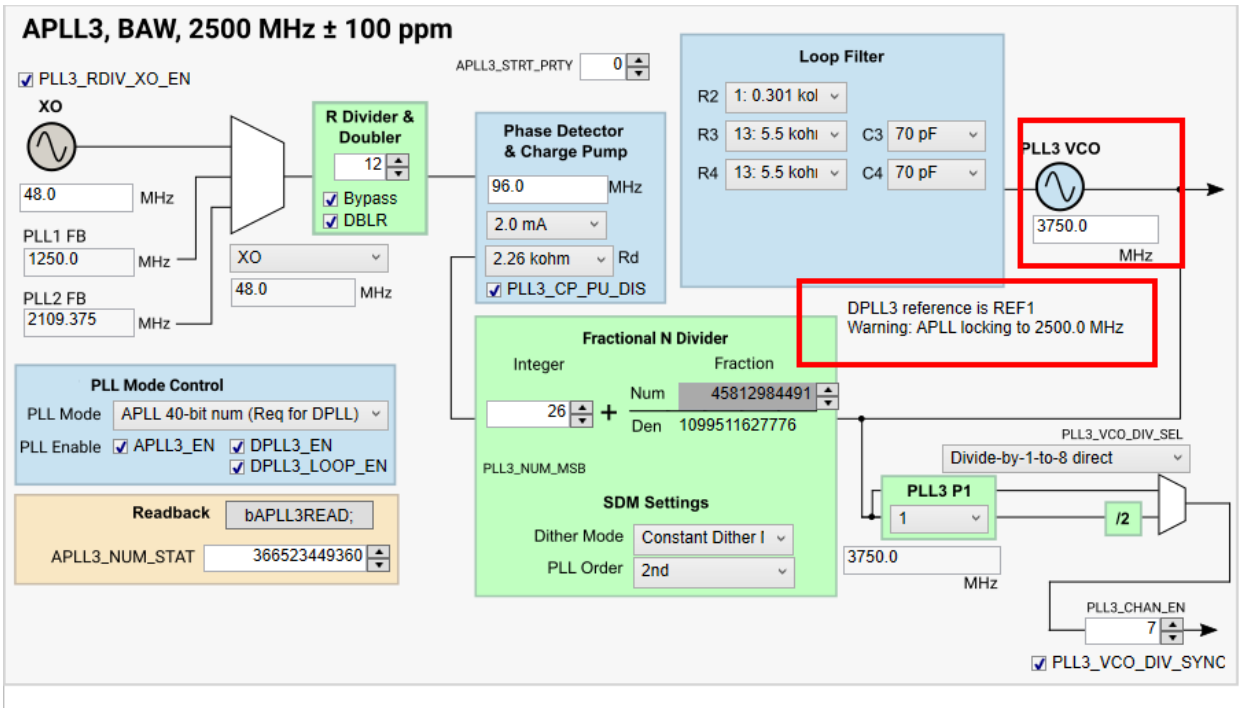


After hitting “Run Script” button








APLL3, BAW, 2500 MHz ± 100 ppm
PLL3_RDIV_XO_EN
APLL3_STRT_PRTY
0
XO
48.0
MHz
PLL1 FB
1250.0
MHz
PLL2 FB
2109.375
MHz
R Divider & Doubler
12
Bypass
DBLR
XO
48.0
MHz
Phase Detector & Charge Pump
96.0
MHz
2.0 mA
2.26 kohm
Rd
PLL3_CP_PU_DIS
Loop Filter
R2
1: 0.301 kol
R3
13: 5.5 kohı
C3
70 pF
R4
13: 5.5 kohı
C4
70 pF
PLL3 VCO
3750.0
MHz
DPLL3 reference is REF1
Warning: APLL locking to 2500.0 MHz
PLL Mode Control
PLL Mode
APLL 40-bit num (Req for DPLL)
PLL Enable
APLL3_EN
DPLL3_EN
DPLL3_LOOP_EN
Fractional N Divider
Integer
Fraction
26
+
Num
45812984491
Den
1099511627776
PLL3_NUM_MSB
SDM Settings
Dither Mode
Constant Dither I
PLL Order
2nd
PLL3_VCO_DIV_SEL
Divide-by-1-to-8 direct
PLL3 P1
1
/2
3750.0
MHz
Readback
bAPLL3READ;
APLL3_NUM_STAT
366523449360
PLL3_CHAN_EN
7
PLL3_VCO_DIV_SYNC