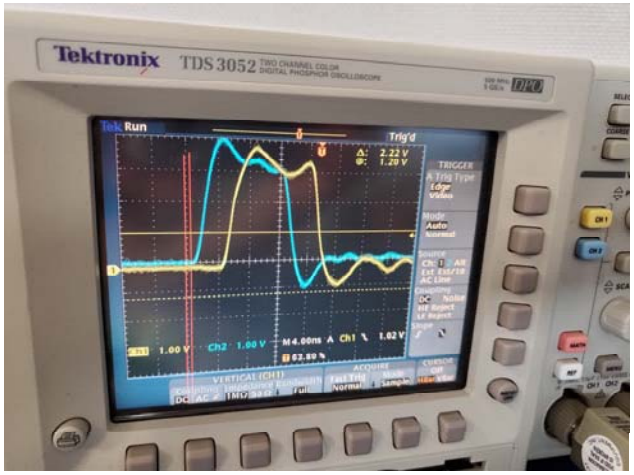

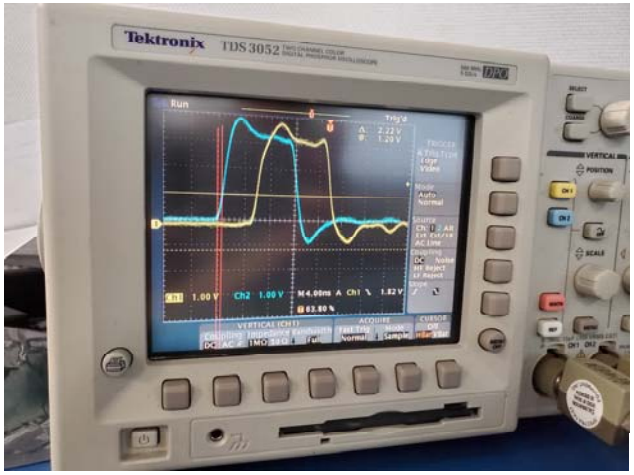

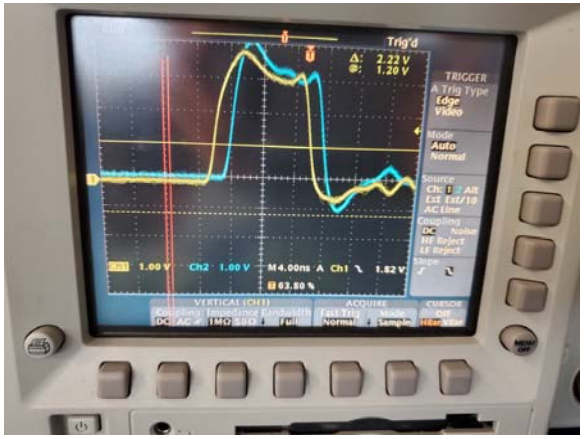

We have a problem that we don't fully understand with regards to locking of PLL1.
In our experiment, we have tried 3 different cards as a reference clock source. They all provide a clock that is 98.304MHz. However, we kept the same receiver card that way the loop components, OCXO (98.304MHz) and LMK04826 remained the same.
The Phase detector frequency for PLL1 is set to 1.536MHz.
In the 3 pictures, the blue line refers to Status_LD1 and yellow line refers to Status_LD2.
Here we configured Status_LD1 to be output of the R-divider and Status_LD2 to be the Output of the N-divider.
As you can see in each of the pix, the phase difference between the yellow and blue is different between cards. Furthermore, sometimes the Blue leads yellow but other times, Yellow leads blue.
What can be the problem? Changing the clock source shouldnt affect the LMK.