LMK05318B TICS Pro GUI Overview

Clock and Timing Solutions

April 25 2023

Introduction

In order to program the LMK05318B using TICS Pro, the following procedure must be performed:

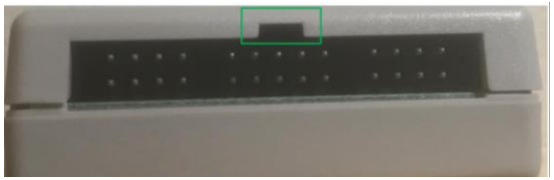
1. Establish communication between the LMK05318B and TICS Pro
2. Initialize key features of the device on the Wizard home page
3. Configure the XO input
4. Set the outputs
5. Set the reference and its validation detectors
6. Configure the DPLL

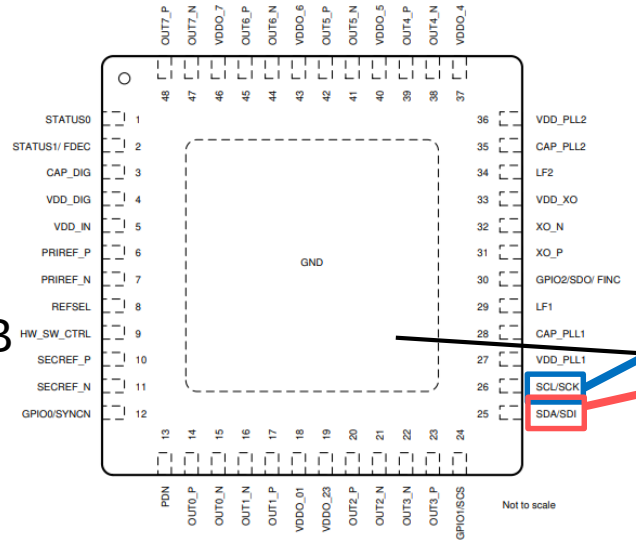
Step 0: Using external USB2ANY

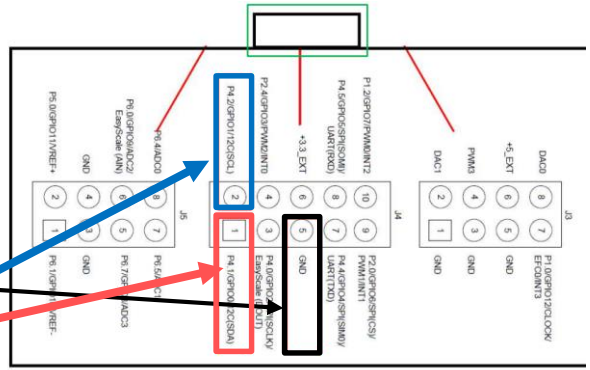
(skip if using EVM with on-board USB2ANY)

Wiring external USB2ANY

- Link to USB2ANY document
- Only need to connect 3 lines for I2C connection
  - SDA
  - SCL
  - GND
- Ensure LMK05318B is powered.



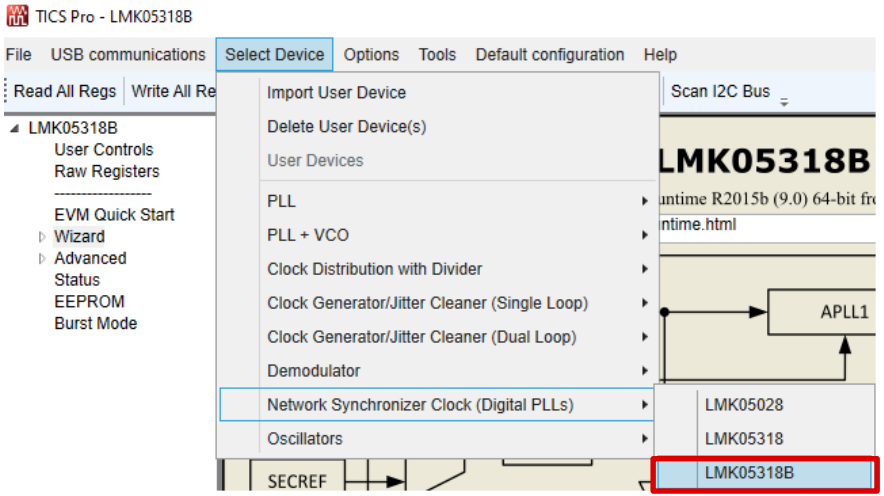




Step 1: Establish Connection

Step 1a: Open the LMK05318B Profile

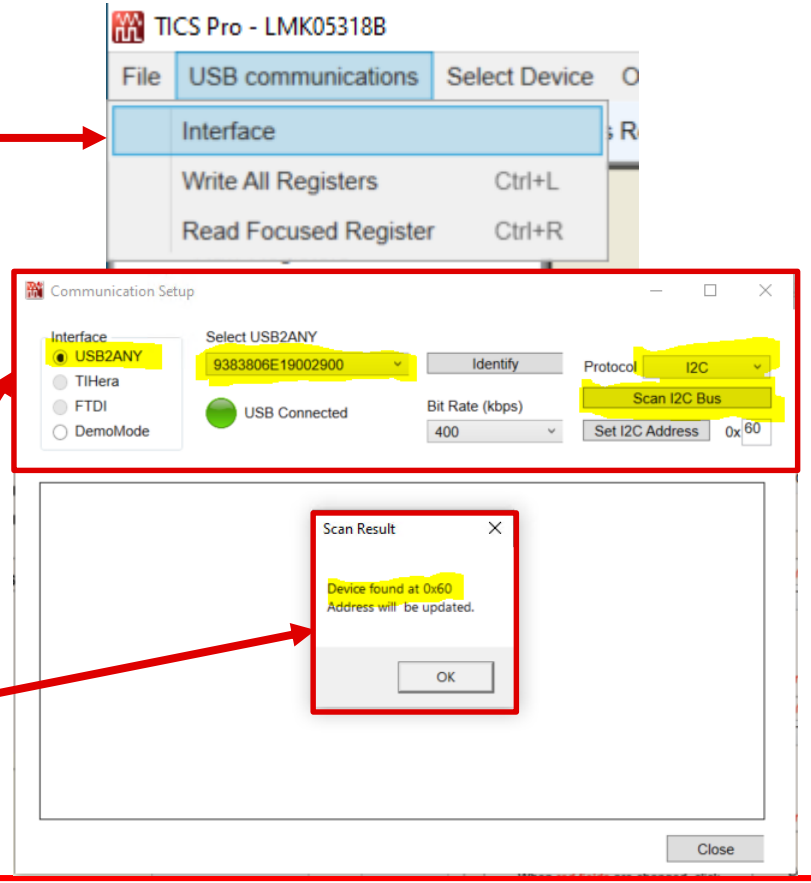
- Navigate to **Select Device → Network Synchronizer Clock (Digital PLLs) → LMK05318B** to open the correct profile.



Step 1b: Establish Connection between TICS Pro and the LMK05318B (I2C)

- To establish connection between the device and GUI, navigate to **USB communications → Interface** in the toolbar.

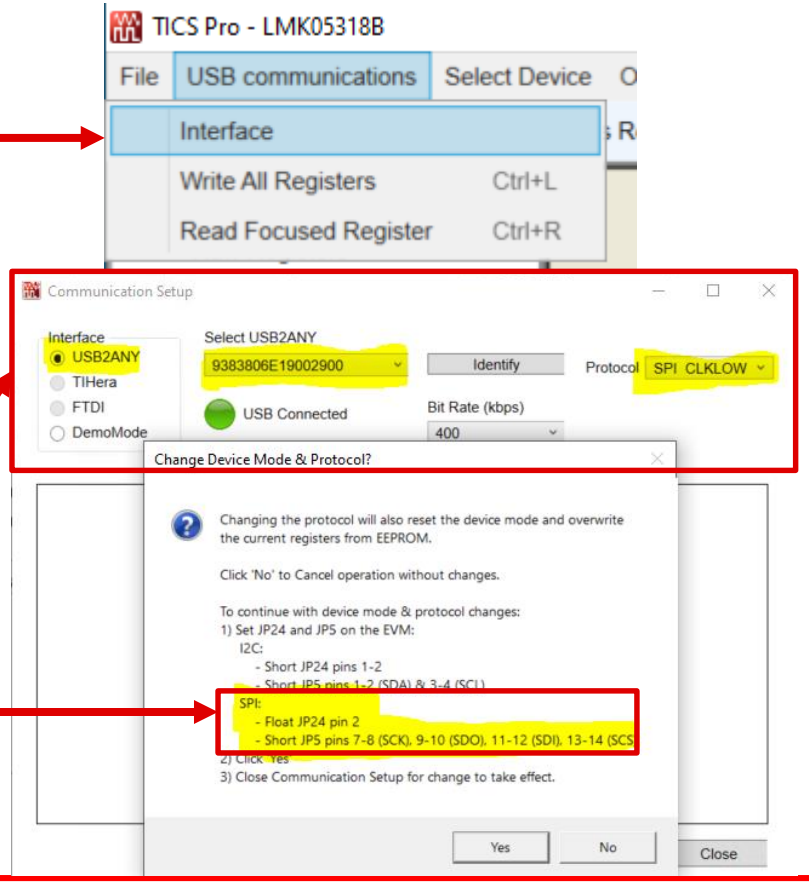
- Once **Interface** has been selected, a communication setup window will appear.
  - In the window, select the **USB2ANY** interface, select a USB2ANY ID number, set the protocol to **I2C** and then press **Scan I2C Bus**.
    - Once the I2C bus has been scanned and a address is found, you will have obtain successful connection.



Step 1b: Establish Connection between TICS Pro and the LMK05318B (SPI)

- To establish connection between the device and GUI, navigate to **USB communications → Interface** in the toolbar.

- Once **Interface** has been selected, a communication setup window will appear.
  - In the window, select the **USB2ANY** interface, select a USB2ANY ID number, and then set the protocol to **SPI**.
    - When using SPI, ensure that the jumpers are set as shown here:



Step 2: Initialize key features of the device on the Wizard home page

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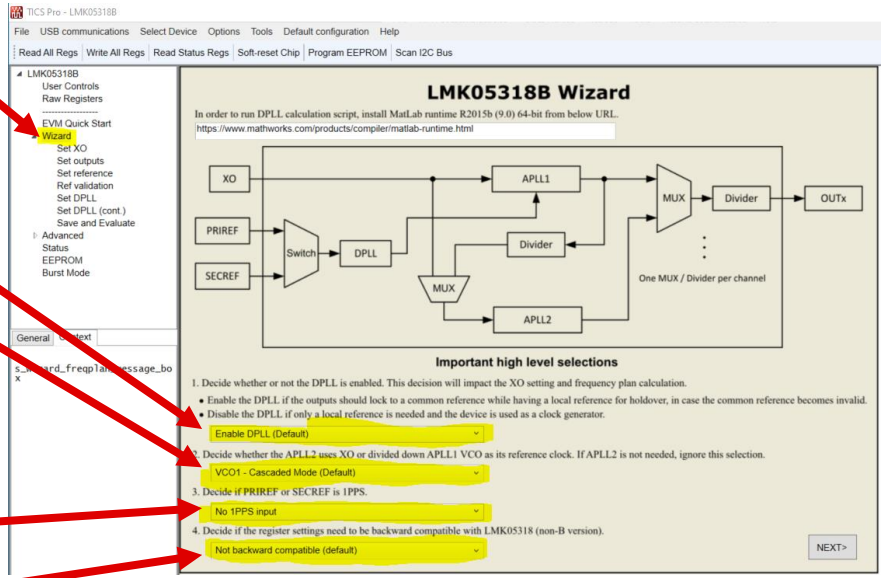
- Navigate to the Wizard home page
  - The wizard home page will be used to initialize key devices.
- Key features:
  - Select whether the DPLL will be used.
  - Determine APLL2's reference clock.
    - VCO1 – Cascaded Mode
      - Recommended setting as it will result in better output phase noise performance for APLL2 clocks.
    - XO
  - Decide if PRIREF or SECREF is 1PPS.
  - Decide if the register settings need to be compatible with the non-B version.



Step 3: Configure the XO input

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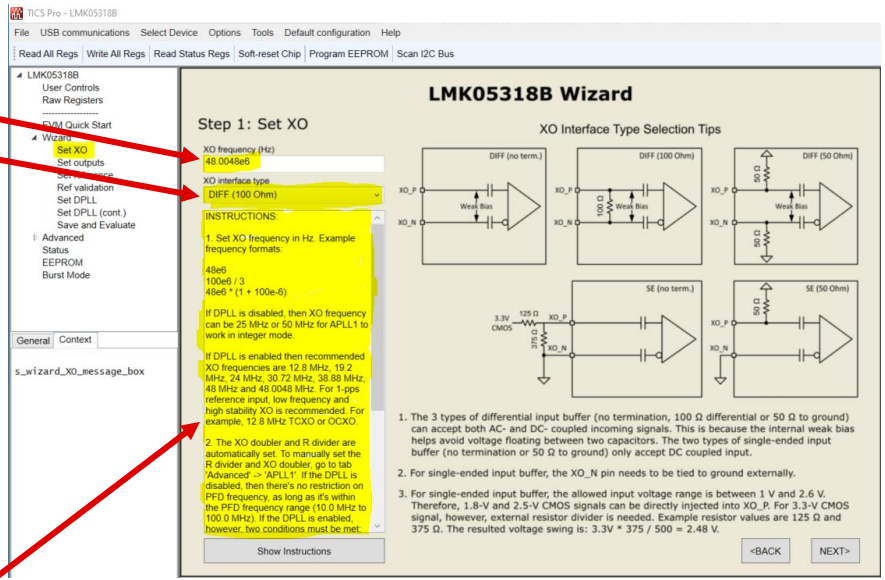
- Navigate to the Set XO page
  - The Set XO page is used to configure the XO input
- Enter your desired XO frequency
- Enter your desired XO interface type
  - Interface options are:
    - DIFF (no term.)
      - Used for AC or DC coupled differential input types where terminations are external to the input.
    - DIFF (100 Ohm)
      - Used for AC or DC coupled differential input types. 100 ohm termination set internal to LMK05318B, so no external termination required.
    - DIFF (50 Ohm)
      - Used for DC-coupled HCSL input.
    - SE (no term.)
      - Used for DC-coupled LVCMOS input.
    - SE (50 ohm)
      - Used for DC-coupled LVCMOS input and places a 50 ohm to GND on XO_P pin.
- The Instructions message box provides more information on how to configure your XO input.



Step 4: Set the output frequencies and output format types

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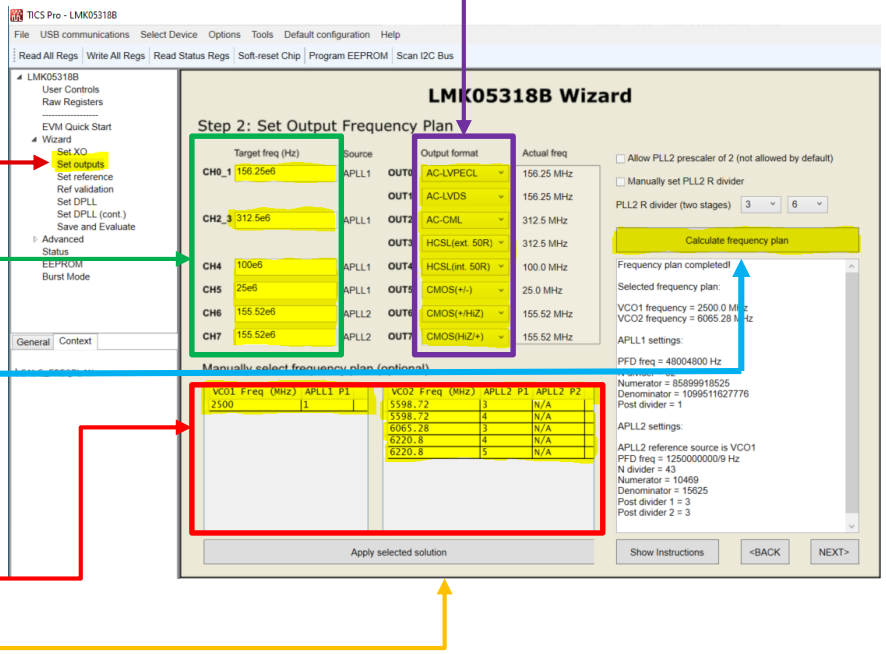
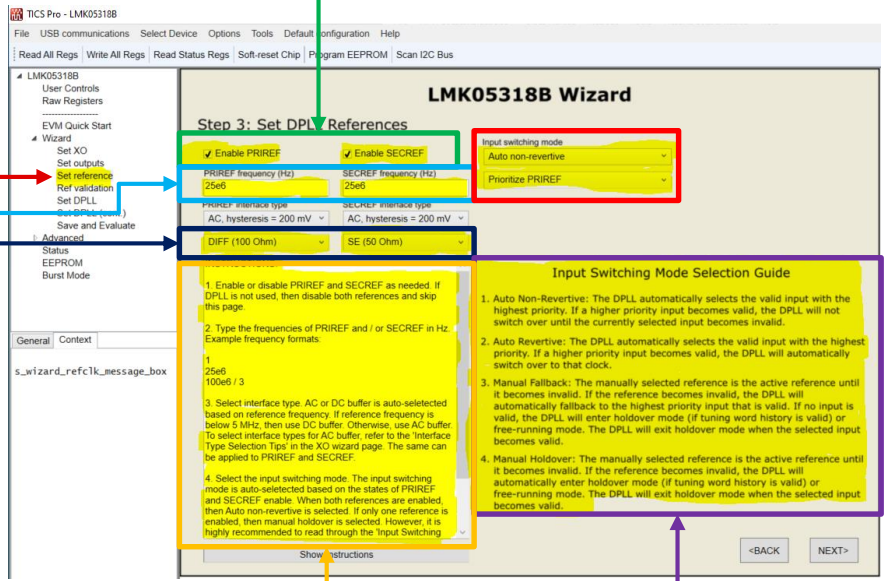
- Navigate to the **Set Outputs** page
- Enter your desired output frequencies
- Select your desired output formats
  - Format options are:
    - AC-LVDS
    - AC-LVPECL
    - AC-CML
    - HCSL (external 50 ohm)
    - HCSL (internal 50 ohm)
    - OUT 4 to OUT7 also support CMOS
- Once you have set the output frequencies and formats, press **Calculate frequency plan**
  - The APLL configuration of the device will now be completed.
  - The APLL settings will be shown in the instruction box
- If you would like to use different VCO frequencies from the ones automatically calculated, you can select them in the manual selection box.
  - Then press **Apply selected solution** for the new VCO settings to be applied.



Step 5: Set the reference and its validation detectors

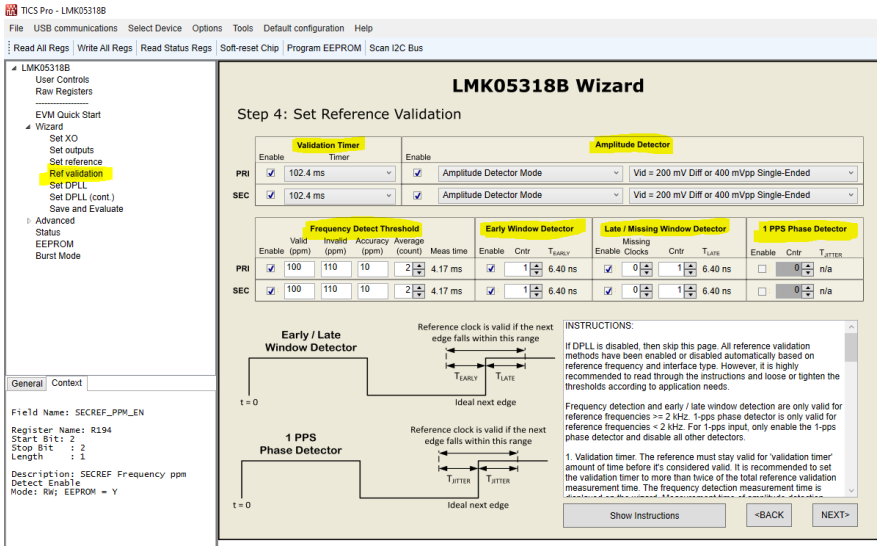
Step 5A: Set the reference

- Navigate to the **Set reference** page
- Enable or disable PRIREF and SECREF as needed. **If DPLL is not used, then disable both references and skip this page.**
- Type the frequencies of PRIREF and / or SECREF in Hz.
- Enter your desired REF interface type
  - Interface options are:
    - DIFF (no term.)
      - Used for AC or DC coupled differential input types where terminations are external to the input.
    - DIFF (100 Ohm)
      - Used for AC or DC coupled differential input types. 100 ohm termination set internal to LMK05318B, so no external termination required.
    - DIFF (50 Ohm)
      - Used for DC-coupled HCSL input.
    - SE (no term.)
      - Used for DC-coupled LVCMOS input.
    - SE (50 ohm)
      - Used for DC-coupled LVCMOS input and places a 50 ohm to GND on the _P pin of the reference
- Select the input switching mode and priorities inside red box in image
  - descriptions of each mode are shown here
- **The Instructions message box provides more information on how to configure your reference inputs. Please read for greater details.**



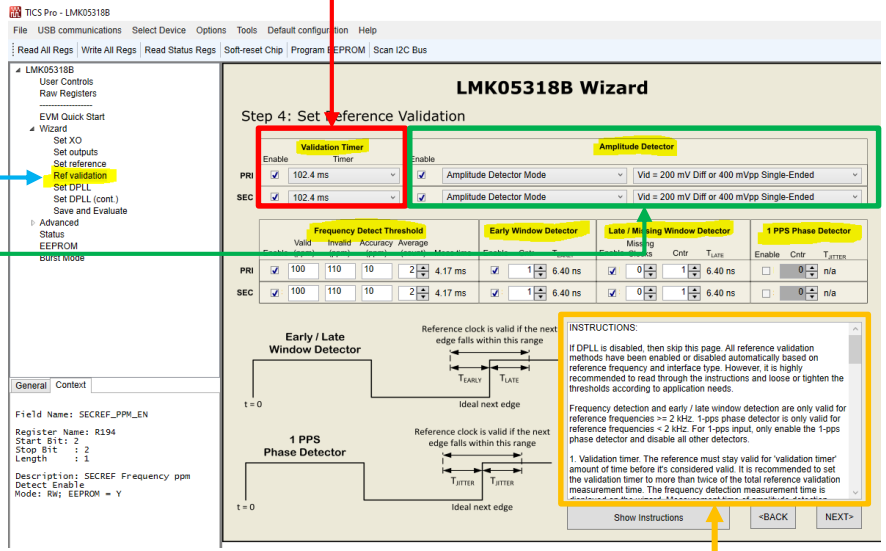
Step 5B: Set the reference validation detectors overview

- If DPLL is disabled, then skip this page.
- All reference validation methods have been enabled or disabled automatically based on reference frequency and interface type.
  - However, it is highly recommended to read through the instructions and loose or tighten the thresholds according to application needs.
- The **Frequency Detect Threshold, Early Window Detector, and Late/Missing Window Detector** are only valid for reference frequencies >= 2 kHz.
- The **1-PPS Phase Detector** is only valid for reference frequencies < 2 kHz.
- For 1-pps input, only enable the **1-pps phase detector** and disable all other detectors.



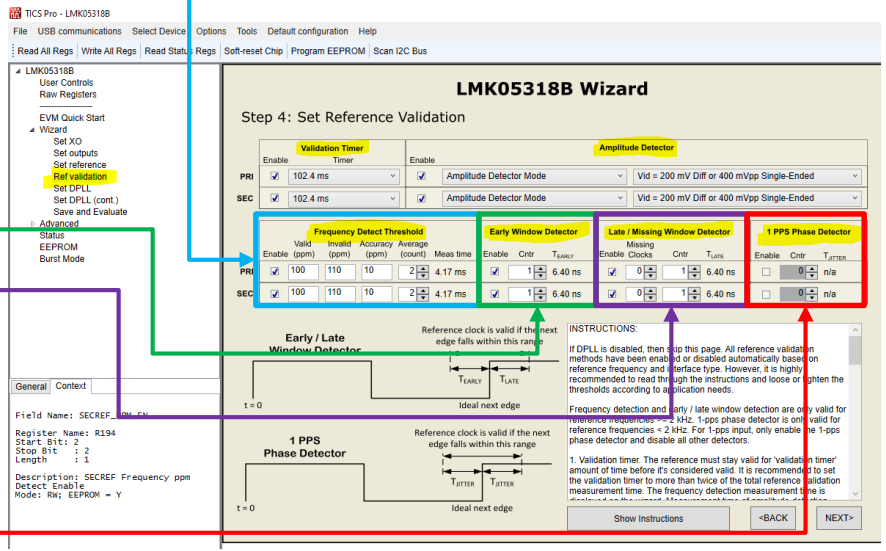
Step 5C: Set the reference validation detectors configuration

- Navigate to the **Ref validation** page
- Set the Validation Timer
  - The validation timer setting determines the amount of time the reference must stay valid before it's considered valid.
- Set the Amplitude Detector
  - There are two modes: amplitude detector mode and CMOS slew rate detector mode
    - In amplitude detector mode, the reference is considered valid if the signal swing is higher than the selected threshold.
    - In CMOS slew rate detector mode, the detection method can be either slew rate detection or VIH / VIL detection.
      - For slew rate detection, the input slew rate must be faster than 0.2 V/ns.
      - For VIH / VIL detection, the input high level must be above 1.8 V and the low level must be below 0.6 V.
- **The Instructions message box provides more information on how to configure your reference validation settings. Please read for greater details.**



Step 5C: Set the reference validation detectors configuration (continued)

- For reference frequencies >= 2 kHz
  - Set the Frequency Detect Threshold
    - Frequency detection needs 4 parameters:
      - Valid threshold in ppm
      - Invalid threshold in ppm
      - Accuracy in ppm
      - Average count
    - Please read the instruction box (bullet 3) for more details on how to configure the frequency detector parameters.
  - Set the Early Window Detector
    - Determines T_early
  - Set the Late/Missing Window Detector
    - Determines T_late
    - The reference input is considered valid if its next clock edge falls within the T_early and T_late range
    - Please read the instruction box (bullet 4) for more details on how to configure the early and late detector parameters.
- For a 1PPS reference
  - Set the 1PPS Phase Detector
    - Determines T_jitter
    - The reference input is considered valid if its next clock edge falls within the T_jitter range



Step 6: Configure the DPLL

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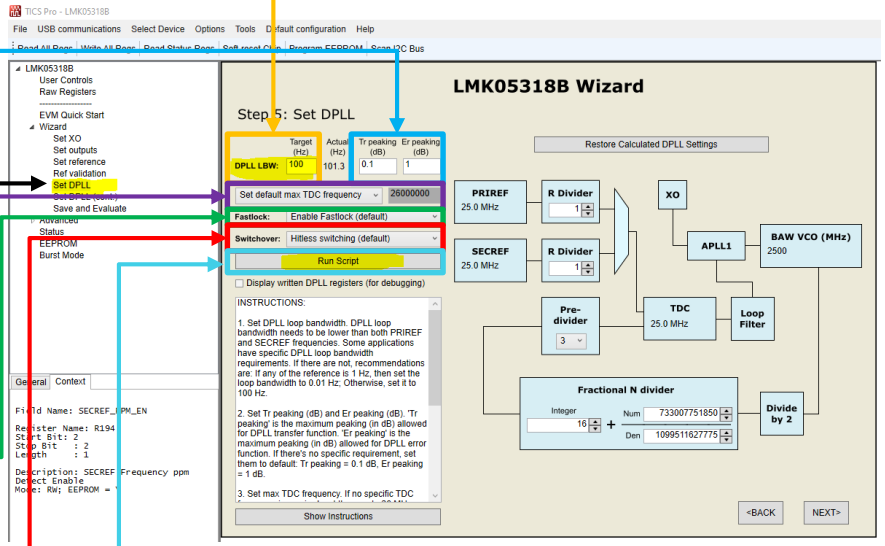
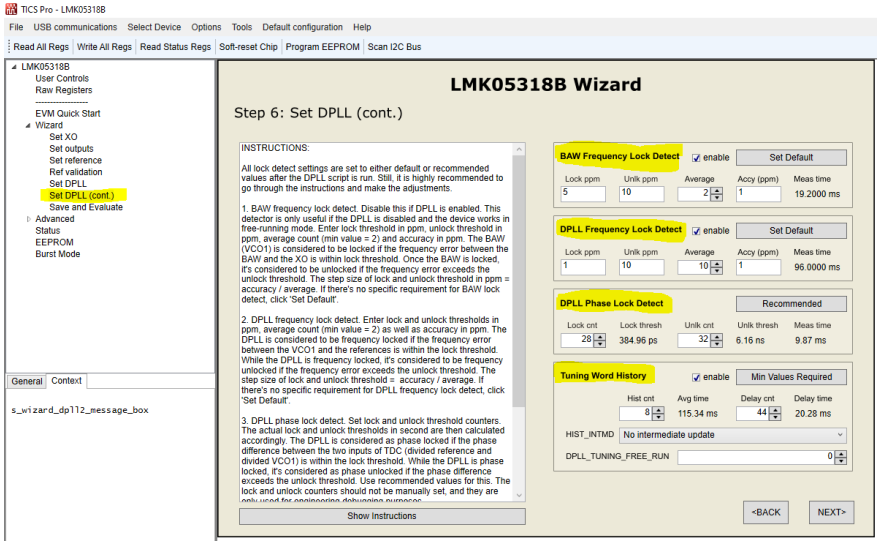
- Navigate to the **Set DPLL** page
- Set the DPLL loop bandwidth
  - The DPLL loop bandwidth needs to be lower than both PRIREF and SECREF frequencies
- Set Tr peaking (dB) and Er peaking (dB)
  - Tr peaking is the maximum peaking (in dB) allowed for DPLL transfer function
    - default: Tr peaking = 0.1 dB
  - Er peaking is the maximum peaking (in dB) allowed for DPLL error function.
    - Default: Er peaking = 1 dB
- Set max TDC frequency
  - If no specific TDC frequency is required, set the max to 26 MHz
- Fastlock should only be disabled for 1pps input
- For most use cases, switchover method should always be set to 'hitless switching'.
- Click 'Run Script' button and wait for 1 ~ 2 minutes while the script is running. Make sure that the MATLAB runtime is installed as instructed in the first wizard page.



Step 6: Configure the DPLL (continued)

- Navigate to the **Set DPLL (cont.)** page
- Configure the BAW Frequency Lock Detect
  - Disable if DPLL is enabled
  - Used to determine if BAW (VCO1) is locked
- Configure the DPLL Frequency Lock Detect
  - Used to determine if DPLL is frequency locked
- Configure the DPLL Phase Lock Detect
  - Used to determine if DPLL is phase locked
- Configure the Tuning Word History
  - This block sets the tuning word history for holdover.
  - Refer to datasheet section '9.3.7.4 Tuning Word History' for details.
- **The Instructions message box provides more information on how to configure the lock detectors and tuning word history settings. Please read for greater details.**



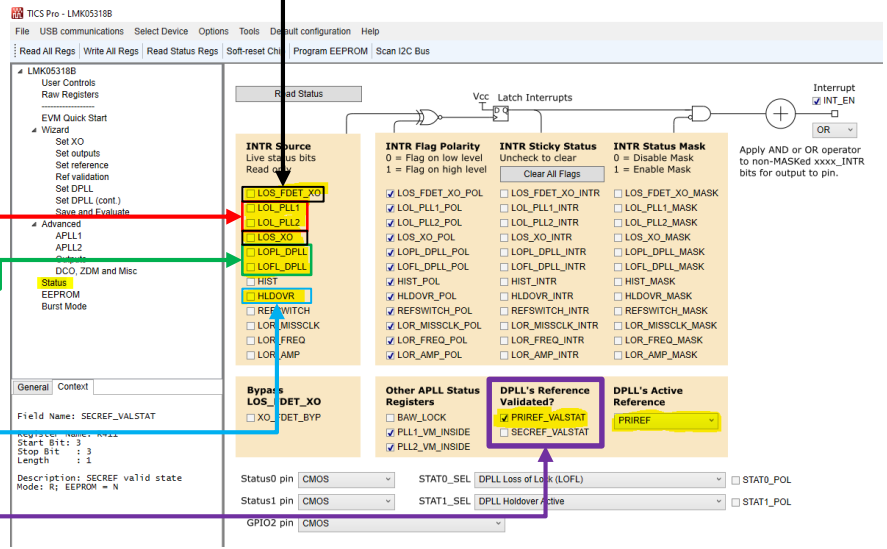
Appendix: Additional GUI Features

Appendix Introduction

- The following appendix slides will display additional features of the LMK05318B.
- Please note that these are features are not required for obtaining an initial configuration, but can be beneficial features after the initial configuration is created by following steps 1 to 6 on the previous slides.
- The additional features include:
  - Status page
  - DCO and ZDM page
  - Outputs page
  - EEPROM page
  - APLL1 page
  - APLL2 page
  - User controls page
  - Raw registers page

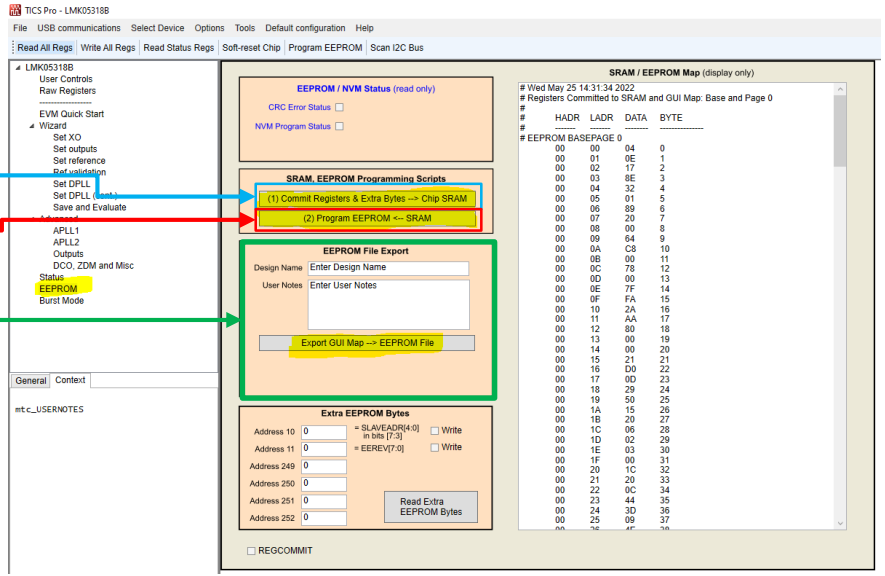
Status Page

- The Status Page can be used to validate the device is locking properly
- LOS_FDET_XO and LOS_XO indicate whether a clock is present at the XO input for the APLLs to lock to
  - When the bits are low, the XO is present and valid
- LOL_PLL1 and LOL_PLL2 indicate whether the APLLs are locking to the XO input
  - When the bits are low, the APLLs are locked properly
- LOPL_DPLL and LOFL_DPLL indicate whether the DPLL is frequency and phase locked to the REF input
  - When the bits are low, the DPLL has successful locked to the REF input
- HLDOVER indicates whether the device is in holdover
- PRIREF_VALSTAT and SECREF_VALSTAT indicate whether the PRIREF or SECREF are present and validated by the reference validation detectors set in step 5
  - When the bits are high, the reference is valid



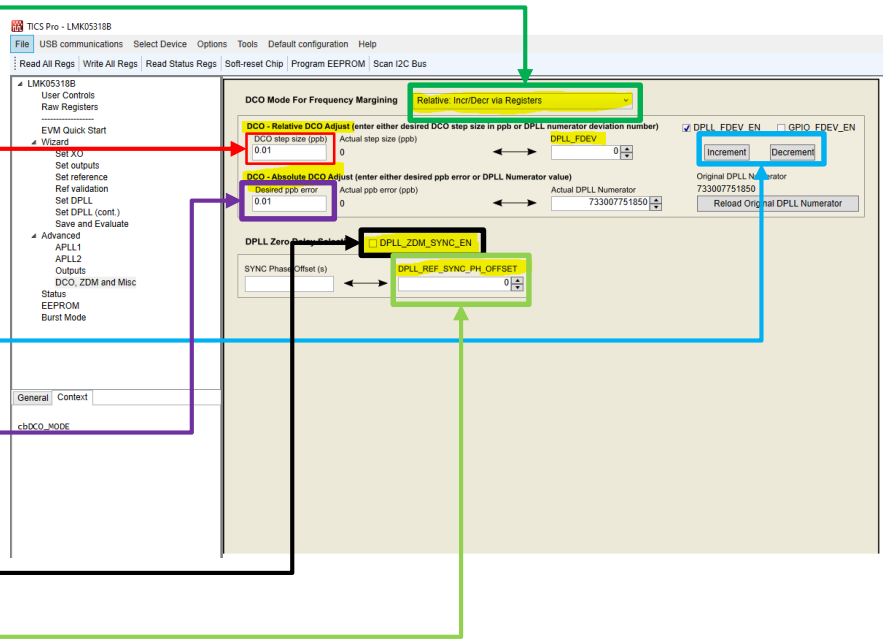
EEPROM Page

- The EEPROM page contains the following features:
  - Program the EEPROM
    - To program the EEPROM, you must
      - Commit the register to the SRAM
      - Program the EEPROM
  - Export the GUI Map to a EEPROM file



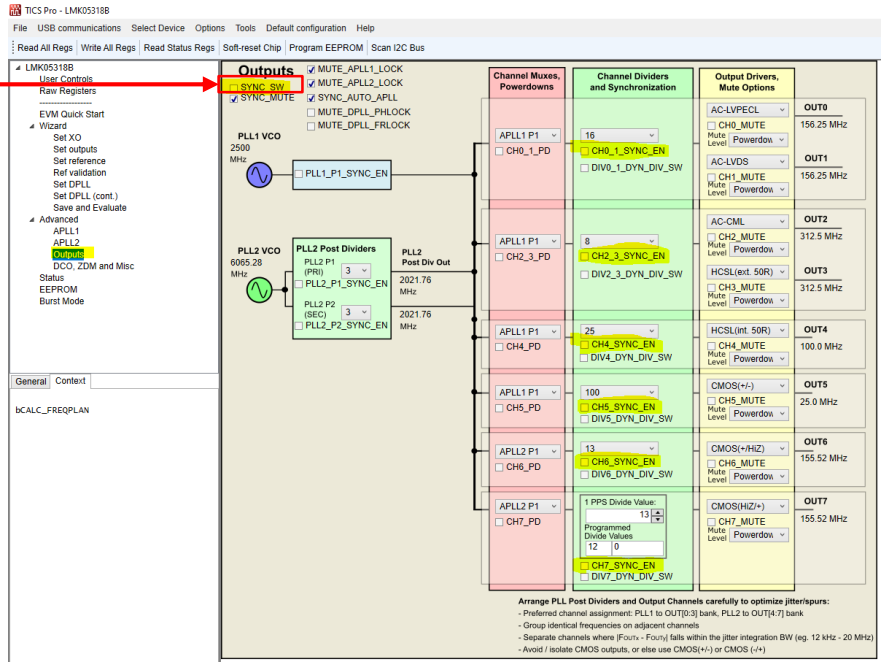
DCO and ZDM Page

- The DCO and ZDM Page can be used to:
  - Perform frequency/phase adjustments with the DCO
    - DCO adjustments can be performed relatively or absolutely
      - Select whether a relative or absolute adjustment is required
      - Relative adjustment
        - » Enter a ppb adjustment that is required and a DPLL_FDEV will be calculated
          - » The DPLL_FDEV will be the numerator deviation that will be adjusted from the DPLL numerator to result in the required ppb adjustment
        - » Press the Increment or decrement button to add or subtract the required ppb adjustment
      - Absolute adjustment
        - » Enter a ppb adjustment that is required and the output clock will automatically be adjusted by that ppb value
  - Enable zero-delay mode to achieve phase alignment between the input clock and output clock on OUT7
    - When the DPLL_ZDM_SYNC_EN is set, ZDM is enabled to achieve input and output phase alignment
    - The DPLL_REF_SYNC_PH_OFFSET can be used to adjust the phase offset between the input and output clocks



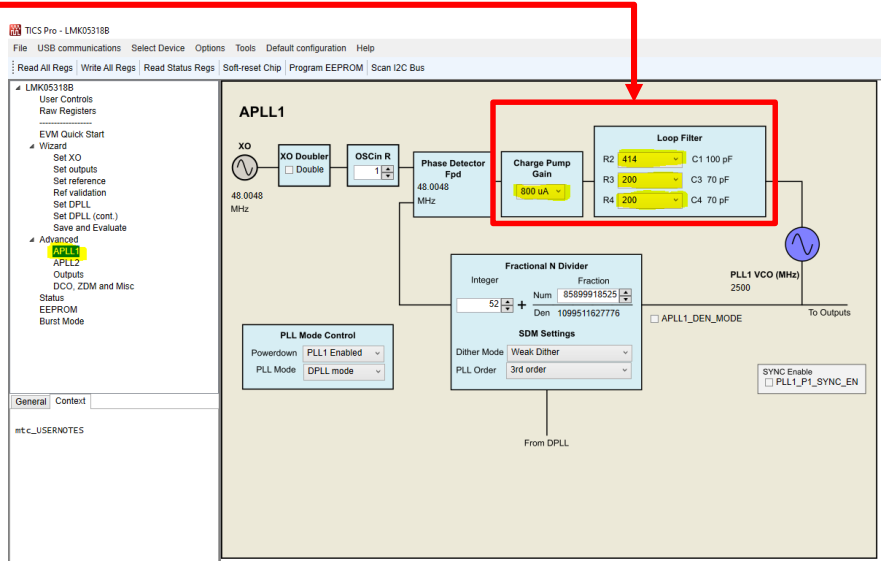
Outputs Page

- The channel muxes, channel dividers, output formats, and output frequencies shown on the outputs page are configured in step 4
- The outputs page provides the following additional features:
  - Output clock synchronization
    - Output sync can be accomplished by enabling the CHx_SYNC_EN bits highlighted in the image to the right
    - For the synchronization to take place, the SYNC_SW bit must be toggled (turned on/off)



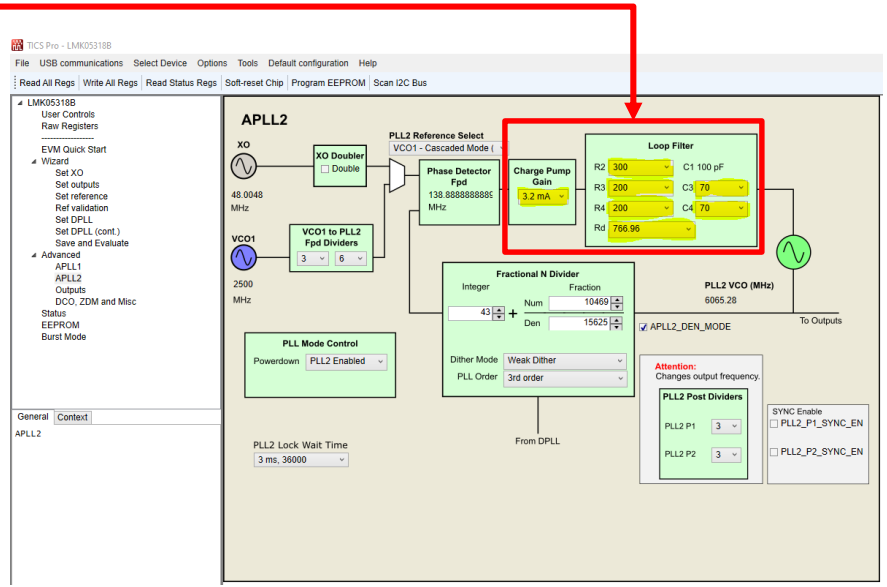
APLL1 Page

- The APLL1 page can be used to configure the charge pump current and loop filter to optimize the output clocks performance
- The rest of the controls on this page will be configured in step 4 and should not be change



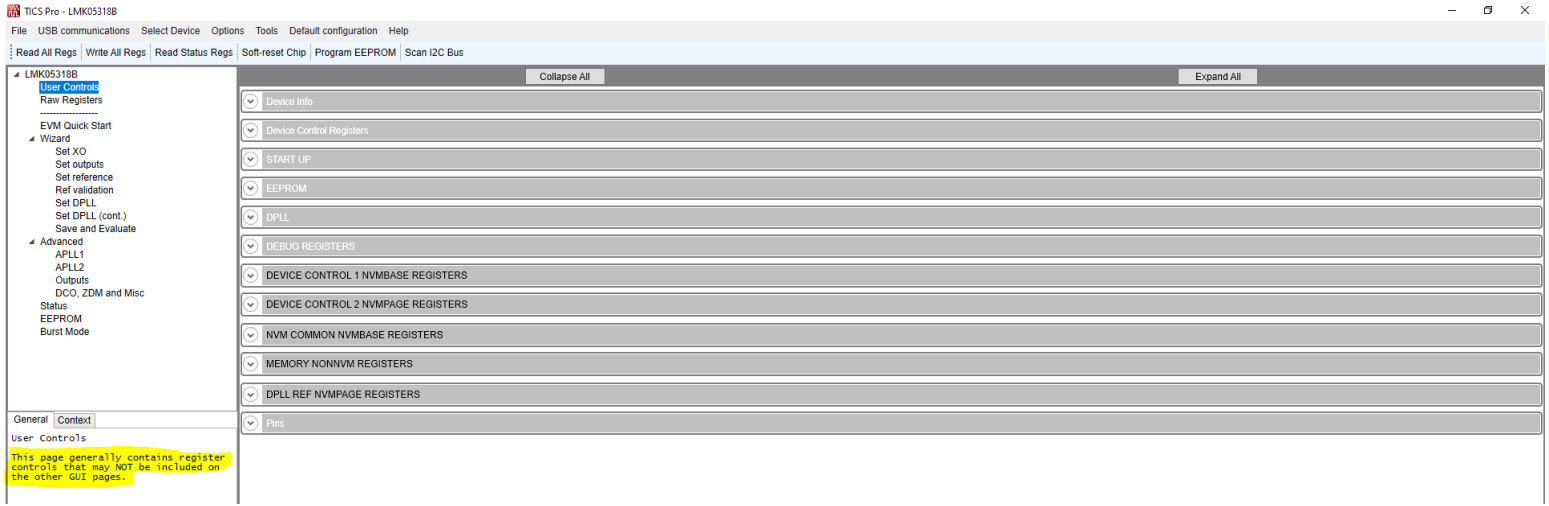
APLL2 Page

- The APLL2 page can be used to configure the charge pump current and loop filter to optimize the output clocks performance
- The rest of the controls on this page will be configured in step 4 or step 2 and should not be change



User Controls Page

- The user control page contains register controls that may not be included on the other GUI pages
  - For example, the device info registers such as PRTID, PRODID, etc.



Raw Registers Page

- The raw register page allows for low-level register write/read operations by register address