

LMK05318B TICS Pro GUI Overview

Clock and Timing Solutions

April 25 2023

Introduction

In order to program the LMK05318B using TICS Pro, the following procedure must be performed:

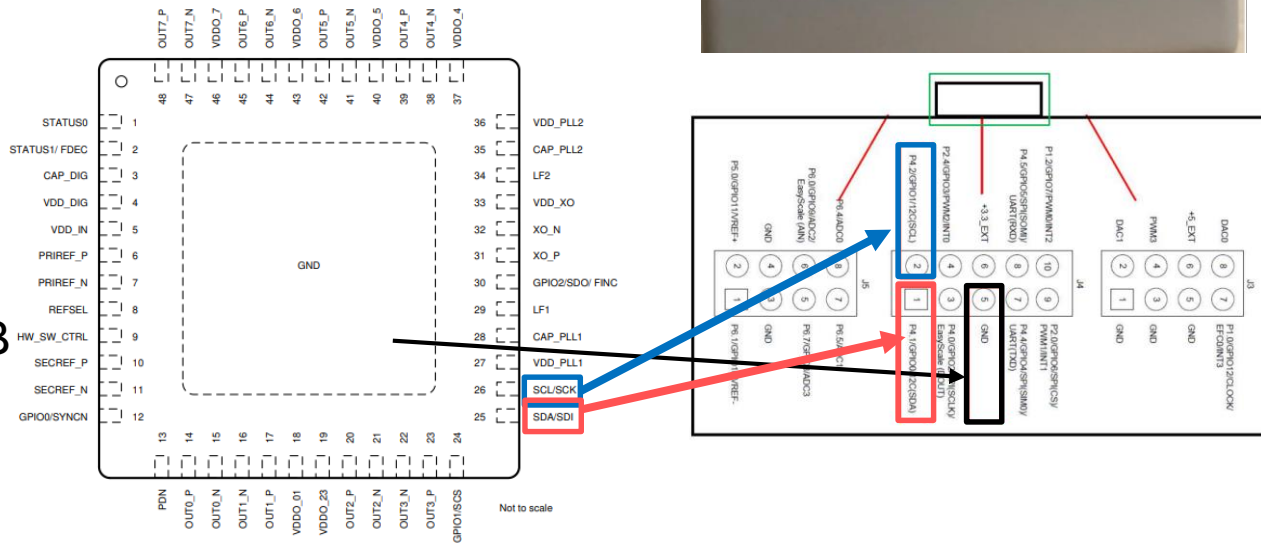
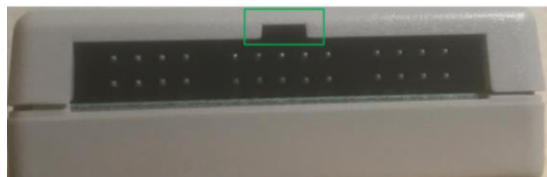
1. Establish communication between the LMK05318B and TICS Pro
2. Initialize key features of the device on the Wizard home page
3. Configure the XO input
4. Set the outputs
5. Set the reference and its validation detectors
6. Configure the DPLL

Step 0: Using external USB2ANY

(skip if using EVM with on-board USB2ANY)

Wiring external USB2ANY

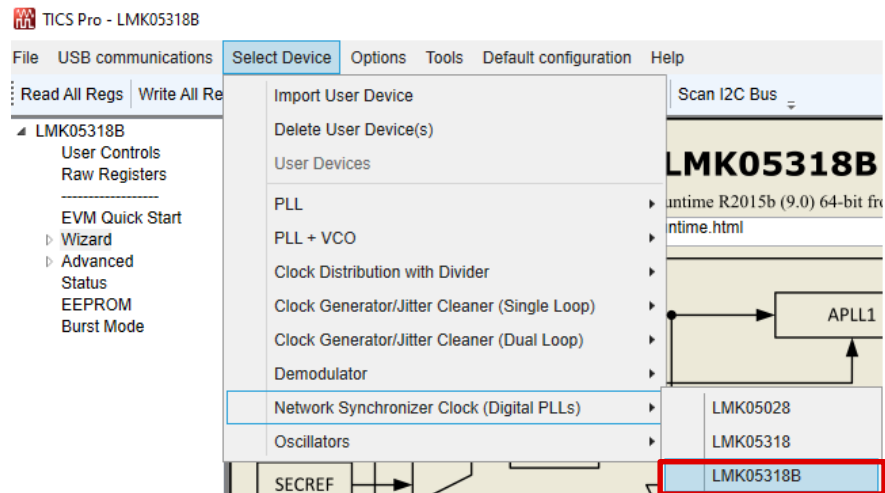
- Link to [USB2ANY document](#)
- Only need to connect 3 lines for I2C connection
 - SDA
 - SCL
 - GND
- Ensure LMK05318B is powered.



Step 1: Establish Connection

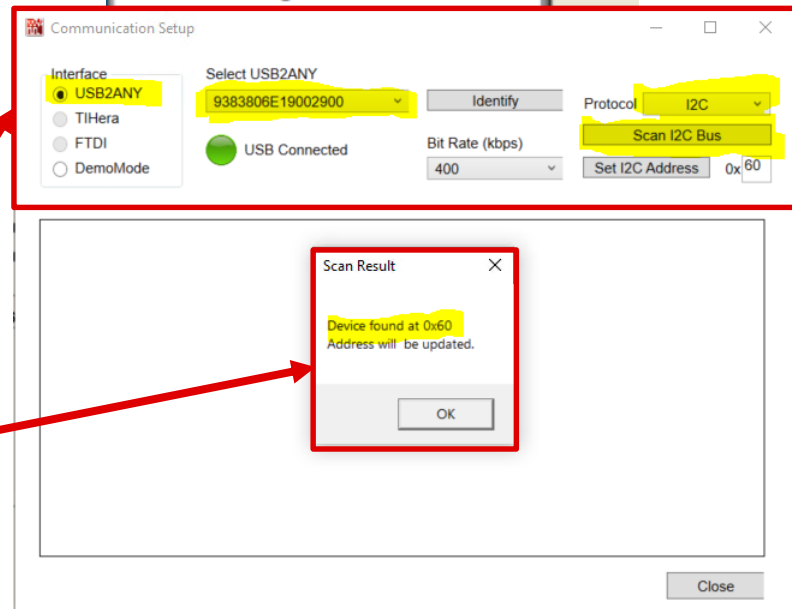
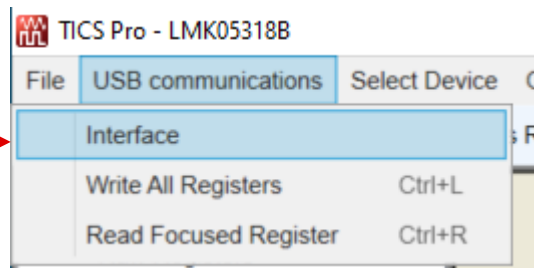
Step 1a: Open the LMK05318B Profile

- Navigate to **Select Device** → **Network Synchronizer Clock (Digital PLLs)** → **LMK05318B** to open the correct profile.



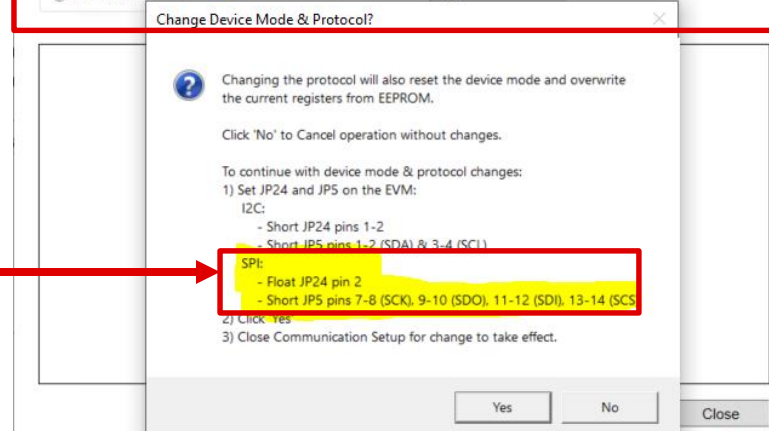
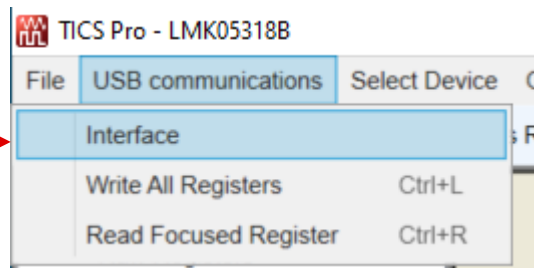
Step 1b: Establish Connection between TICS Pro and the LMK05318B (I2C)

- To establish connection between the device and GUI, navigate to **USB communications** → **Interface** in the toolbar.
- Once **Interface** has been selected, a communication setup window will appear.
 - In the window, select the **USB2ANY** interface, select a USB2ANY ID number, set the protocol to **I2C** and then press **Scan I2C Bus**.
 - Once the I2C bus has been scanned and a address is found, you will have obtain successful connection.



Step 1b: Establish Connection between TICS Pro and the LMK05318B (SPI)

- To establish connection between the device and GUI, navigate to **USB communications** → **Interface** in the toolbar.
- Once **Interface** has been selected, a communication setup window will appear.
 - In the window, select the **USB2ANY** interface, select a USB2ANY ID number, and then set the protocol to **SPI**.
 - When using SPI, ensure that the jumpers are set as shown here:



Step 2: Initialize key features of the device on the Wizard home page

Step 2: Initialize key features of the device on the Wizard home page

- Navigate to the Wizard home page
 - The wizard home page will be used to initialize key devices.
- Key features:
 - Select whether the DPLL will be used.
 - Determine APLL2's reference clock.
 - VCO1 – Cascaded Mode
 - Recommended setting as it will result in better output phase noise performance for APLL2 clocks.
 - XO
 - Decide if PRIREF or SECREf is 1PPS.
 - Decide if the register settings need to be compatible with the non-B version.

LMK05318B Wizard

In order to run DPLL calculation script, install Matlab runtime R2015b (9.0) 64-bit from below URL.
<https://www.mathworks.com/products/compiler/matlab-runtime.html>

The block diagram shows the following components and connections:
- Inputs: XO, PRIREF, SECREf.
- A Switch selects between PRIREF and SECREf.
- The Switch output goes to a DPLL block.
- The DPLL output goes to a MUX block.
- The MUX output goes to a Divider block.
- The Divider output goes to an APLL1 block.
- The APLL1 output goes to another MUX block.
- The APLL1 output also goes to a second Divider block.
- The second Divider output goes to an APLL2 block.
- The APLL2 output goes to a third MUX block.
- The third MUX output goes to a final Divider block.
- The final Divider output goes to the OUTx block.
- Note: One MUX / Divider per channel.

Important high level selections

1. Decide whether or not the DPLL is enabled. This decision will impact the XO setting and frequency plan calculation.
 - Enable the DPLL if the outputs should lock to a common reference while having a local reference for holdover, in case the common reference becomes invalid.
 - Disable the DPLL if only a local reference is needed and the device is used as a clock generator.

Enable DPLL (Default)
2. Decide whether the APLL2 uses XO or divided down APLL1 VCO as its reference clock. If APLL2 is not needed, ignore this selection.
 - VCO1 - Cascaded Mode (Default)

VCO1 - Cascaded Mode (Default)
3. Decide if PRIREF or SECREf is 1PPS.
 - No 1PPS input

No 1PPS input
4. Decide if the register settings need to be backward compatible with LMK05318 (non-B version).
 - Not backward compatible (default)

Not backward compatible (default)

NEXT>

Step 3: Configure the XO input

Step 3: Configure the XO input

- Navigate to the Set XO page
 - The Set XO page is used to configure the XO input
- Enter your desired XO frequency
 - Used for AC or DC coupled differential input types where terminations are external to the input.
- Enter your desired XO interface type
 - Interface options are:
 - DIFF (no term.)
 - Used for AC or DC coupled differential input types where terminations are external to the input.
 - DIFF (100 Ohm)
 - Used for AC or DC coupled differential input types. 100 ohm termination set internal to LMK05318B, so no external termination required.
 - DIFF (50 Ohm)
 - Used for DC-coupled HCSL input.
 - SE (no term.)
 - Used for DC-coupled LVCMOS input.
 - SE (50 ohm)
 - Used for DC-coupled LVCMOS input and places a 50 ohm to GND on XO_P pin.
- The Instructions message box provides more information on how to configure your XO input.

Step 1: Set XO

XO frequency (Hz)
48.0048e6

XO interface type
DIFF (100 Ohm)

INSTRUCTIONS

1. Set XO frequency in Hz. Example frequency formats:
48e6
100e6 / 3
48e6 * (1 + 100e-6)

If DPLL is disabled, then XO frequency can be 25 MHz or 50 MHz for APLL1 to work in integer mode.

If DPLL is enabled then recommended XO frequencies are 12.8 MHz, 19.2 MHz, 24 MHz, 30.72 MHz, 38.88 MHz, 48 MHz and 48.0048 MHz. For 1-pps reference input, low frequency and high stability XO is recommended. For example, 12.8 MHz TCXO or OCXO.

2. The XO doubler and R divider are automatically set. To manually set the R divider and XO doubler, go to tab 'Advanced' -> 'APLL1'. If the DPLL is disabled, then there's no restriction on PFD frequency, as long as it's within the PFD frequency range (10.0 MHz to 100.0 MHz). If the DPLL is enabled, however, two conditions must be met:

Show Instructions

LMK05318B Wizard

XO Interface Type Selection Tips

The diagram shows six circuit configurations for XO_P and XO_N pins:

- DIFF (no term.): Differential input with no termination.
- DIFF (100 Ohm): Differential input with 100 Ohm termination.
- DIFF (50 Ohm): Differential input with 50 Ohm termination.
- SE (no term.): Single-ended input with no termination.
- SE (50 Ohm): Single-ended input with 50 Ohm termination.

3. The 3 types of differential input buffer (no termination, 100 Ω differential or 50 Ω to ground) can accept both AC- and DC- coupled incoming signals. This is because the internal weak bias helps avoid voltage floating between two capacitors. The two types of single-ended input buffer (no termination or 50 Ω to ground) only accept DC coupled input.

2. For single-ended input buffer, the XO_N pin needs to be tied to ground externally.

3. For single-ended input buffer, the allowed input voltage range is between 1 V and 2.6 V. Therefore, 1.8-V and 2.5-V CMOS signals can be directly injected into XO_P. For 3.3-V CMOS signal, however, external resistor divider is needed. Example resistor values are 125 Ω and 375 Ω. The resulted voltage swing is: $3.3V * 375 / 500 = 2.46 V$.

BACK NEXT

Step 4: Set the output frequencies and output format types

Step 4: Set the output frequencies and output format types

- Navigate to the **Set Outputs** page
- Enter your desired output frequencies
- Select your desired output formats
 - Format options are:
 - AC-LVDS
 - AC-LVPECL
 - AC-CML
 - HCSL (external 50 ohm)
 - HCSL (internal 50 ohm)
 - OUT 4 to OUT7 also support CMOS
- Once you have set the output frequencies and formats, press **Calculate frequency plan**
 - The APLL configuration of the device will now be completed.
 - The APLL settings will be shown in the instruction box
- If you would like to use different VCO frequencies from the ones automatically calculated, you can select them in the manual selection box.
 - Then press **Apply selected solution** for the new VCO settings to be applied.

The screenshot shows the LMK05318B Wizard software interface. The main window is titled "Step 2: Set Output Frequency Plan". It features a table with columns for Channel, Target freq (Hz), Source, Output format, and Actual freq. The table contains the following data:

Channel	Target freq (Hz)	Source	Output format	Actual freq
CH0_1	156.25e6	APLL1	AC-LVPECL	156.25 MHz
OUT1			AC-LVDS	156.25 MHz
CH2_3	312.5e6	APLL1	AC-CML	312.5 MHz
OUT2			AC-CML	312.5 MHz
CH4	100e6	APLL1	HCSL(ext. 50R)	100.0 MHz
OUT3			HCSL(int. 50R)	100.0 MHz
CH5	25e6	APLL1	CMOS(+/-)	25.0 MHz
OUT4			CMOS(+/-)	25.0 MHz
CH6	155.52e6	APLL2	CMOS(+/-)	155.52 MHz
OUT5			CMOS(+/-)	155.52 MHz
CH7	155.52e6	APLL2	CMOS(HZ/+)	155.52 MHz
OUT6			CMOS(HZ/+)	155.52 MHz
OUT7			CMOS(HZ/+)	155.52 MHz

Below the table, there is a section for "Manually select frequency plan (optional)" with a table for VCO frequencies:

VCO1 Freq (MHz)	APLL1 P1	VCO2 Freq (MHz)	APLL2 P1	APLL2 P2
2500	1	5598.72	3	N/A
		5598.72	4	N/A
		6065.28	3	N/A
		6220.8	4	N/A
		6220.8	5	N/A

The interface also includes a "Calculate frequency plan" button, a "Frequency plan completed" message, and APLL settings: Numerator = 85899918525, Denominator = 1099511627776, Post divider = 1. APLL2 settings: APLL2 reference source is VCO1, N divider = 43, Numerator = 10469, Denominator = 15625, Post divider 1 = 3, Post divider 2 = 3. At the bottom, there are buttons for "Apply selected solution", "Show Instructions", "<BACK", and "NEXT>".

Step 5: Set the reference and its validation detectors

Step 5A: Set the reference

- Navigate to the **Set reference** page
- Enable or disable PRIREF and SECREF as needed. **If DPLL is not used, then disable both references and skip this page.**
- Type the frequencies of PRIREF and / or SECREF in Hz.
- Enter your desired REF interface type
 - Interface options are:
 - DIFF (no term.)
 - Used for AC or DC coupled differential input types where terminations are external to the input.
 - DIFF (100 Ohm)
 - Used for AC or DC coupled differential input types. 100 ohm termination set internal to LMK05318B, so no external termination required.
 - DIFF (50 Ohm)
 - Used for DC-coupled HCSL input.
 - SE (no term.)
 - Used for DC-coupled LVCMOS input.
 - SE (50 ohm)
 - Used for DC-coupled LVCMOS input and places a 50 ohm to GND on the _P pin of the reference
- Select the input switching mode and priorities inside **red** box in image
 - descriptions of each mode are shown here
- **The Instructions message box provides more information on how to configure your reference inputs. Please read for greater details.**

The screenshot shows the LMK05318B Wizard interface. The main configuration area is titled "Step 3: Set DPLL References". It includes the following fields and options:

- Enable PRIREF
- Enable SECREF
- PRIREF frequency (Hz): 25e6
- SECREF frequency (Hz): 25e6
- PRIREF interface type: AC, hysteresis = 200 mV
- SECREF interface type: AC, hysteresis = 200 mV
- DIFF (100 Ohm)
- SE (50 Ohm)

The "Input switching mode" dropdown is set to "Auto non-revertive". The "Prioritize PRIREF" checkbox is checked.

The "Advanced" section shows "DIFF (100 Ohm)" and "SE (50 Ohm)" selected.

The "Input Switching Mode Selection Guide" provides the following information:

- 1. Auto Non-Revertive:** The DPLL automatically selects the valid input with the highest priority. If a higher priority input becomes valid, the DPLL will not switch over until the currently selected input becomes invalid.
- 2. Auto Revertive:** The DPLL automatically selects the valid input with the highest priority. If a higher priority input becomes valid, the DPLL will automatically switch over to that clock.
- 3. Manual Failback:** The manually selected reference is the active reference until it becomes invalid. If the reference becomes invalid, the DPLL will automatically fallback to the highest priority input that is valid. If no input is valid, the DPLL will enter holdover mode (if tuning word history is valid) or free-running mode. The DPLL will exit holdover mode when the selected input becomes valid.
- 4. Manual Holdover:** The manually selected reference is the active reference until it becomes invalid. If the reference becomes invalid, the DPLL will automatically enter holdover mode (if tuning word history is valid) or free-running mode. The DPLL will exit holdover mode when the selected input becomes valid.

The "Show instructions" button is located at the bottom of the wizard.

Step 5B: Set the reference validation detectors overview

- If DPLL is disabled, then skip this page.
- All reference validation methods have been enabled or disabled automatically based on reference frequency and interface type.
 - However, it is highly recommended to read through the instructions and loose or tighten the thresholds according to application needs.
- The **Frequency Detect Threshold, Early Window Detector, and Late/Missing Window Detector** are only valid for reference frequencies ≥ 2 kHz.
- The **1-PPS Phase Detector** is only valid for reference frequencies < 2 kHz.
- For 1-pps input, only enable the **1-pps phase detector** and disable all other detectors.

LMK053188 Wizard
Step 4: Set Reference Validation

Enable	Validation Timer	Enable	Amplitude Detector
<input checked="" type="checkbox"/>	102.4 ms	<input checked="" type="checkbox"/>	Amplitude Detector Mode
<input checked="" type="checkbox"/>	102.4 ms	<input checked="" type="checkbox"/>	Amplitude Detector Mode

Enable	Valid (ppm)	Invalid (ppm)	Accuracy (ppm)	Average (count)	Meas time	Enable	Cntr	T _{EARLY}	Enable	Cntr	T _{LATE}	Enable	Cntr	T _{JITTER}
<input checked="" type="checkbox"/>	100	110	10	2	4.17 ms	<input checked="" type="checkbox"/>	1	6.40 ns	<input checked="" type="checkbox"/>	0	6.40 ns	<input type="checkbox"/>	0	n/a
<input checked="" type="checkbox"/>	100	110	10	2	4.17 ms	<input checked="" type="checkbox"/>	1	6.40 ns	<input checked="" type="checkbox"/>	0	6.40 ns	<input type="checkbox"/>	0	n/a

Early / Late Window Detector
Reference clock is valid if the next edge falls within this range
T_{EARLY} T_{LATE}
Ideal next edge

1 PPS Phase Detector
Reference clock is valid if the next edge falls within this range
T_{JITTER} T_{JITTER}
Ideal next edge

INSTRUCTIONS:
If DPLL is disabled, then skip this page. All reference validation methods have been enabled or disabled automatically based on reference frequency and interface type. However, it is highly recommended to read through the instructions and loose or tighten the thresholds according to application needs.
Frequency detection and early / late window detection are only valid for reference frequencies ≥ 2 kHz. 1-pps phase detector is only valid for reference frequencies < 2 kHz. For 1-pps input, only enable the 1-pps phase detector and disable all other detectors.
1. Validation timer. The reference must stay valid for "validation timer" amount of time before it's considered valid. It is recommended to set the validation timer to more than twice of the total reference validation measurement time. The frequency detection measurement time is...

Show Instructions -BACK NEXT>

Step 5C: Set the reference validation detectors configuration

- Navigate to the **Ref validation** page
- Set the Validation Timer
 - The validation timer setting determines the amount of time the reference must stay valid before it's considered valid.
- Set the Amplitude Detector
 - There are two modes: amplitude detector mode and CMOS slew rate detector mode
 - In amplitude detector mode, the reference is considered valid if the signal swing is higher than the selected threshold.
 - In CMOS slew rate detector mode, the detection method can be either slew rate detection or VIH / VIL detection.
 - For slew rate detection, the input slew rate must be faster than 0.2 V/ns.
 - For VIH / VIL detection, the input high level must be above 1.8 V and the low level must be below 0.6 V.
- **The Instructions message box provides more information on how to configure your reference validation settings. Please read for greater details.**

The screenshot shows the TICS Pro - LMK053188 Wizard interface. The left sidebar lists various configuration options, with 'Ref validation' highlighted in yellow. The main window displays 'Step 4: Set Reference Validation' with several configuration sections:

- Validation Timer:** Includes 'Enable' (checked), 'Timer' (102.4 ms), and 'PRI' (checked).
- Amplitude Detector:** Includes 'Enable' (checked), 'Amplitude Detector Mode' (selected), and 'Vid = 200 mV Diff or 400 mVpp Single-Ended'.
- Frequency Detect Threshold:** Includes 'Valid' (checked), 'Invld' (checked), 'Accuracy' (10), 'Average' (2), and '4.17 ms'.
- Early Window Detector:** Includes 'Enable' (checked), 'T_EARLY' (1), and 'T_LATE' (6.40 ns).
- Late / Missing Window Detector:** Includes 'Enable' (checked), 'T_LATE' (6.40 ns), and 'T_TOTTER' (6.40 ns).
- 1 PPS Phase Detector:** Includes 'Enable' (checked), 'Cntr' (0), and 'T_TOTTER' (n/a).

Below the configuration sections are two timing diagrams:

- Early / Late Window Detector:** Shows a reference clock signal with 'Ideal next edge' and 'Reference clock is valid if the next edge falls within this range' between T_{EARLY} and T_{LATE} .
- 1 PPS Phase Detector:** Shows a reference clock signal with 'Ideal next edge' and 'Reference clock is valid if the next edge falls within this range' between T_{TETTER} and T_{TETTER} .

An 'INSTRUCTIONS' box is highlighted in yellow, containing the following text:

INSTRUCTIONS:
If DPLL is disabled, then skip this page. All reference validation methods have been enabled or disabled automatically based on reference frequency and interface type. However, it is highly recommended to read through the instructions and loose or tighten the thresholds according to application needs.
Frequency detection and early / late window detection are only valid for reference frequencies ≥ 2 kHz. 1-pps phase detector is only valid for reference frequencies < 2 kHz. For 1-pps input, only enable the 1-pps phase detector and disable all other detectors.
1. Validation timer. The reference must stay valid for 'validation timer' amount of time before it's considered valid. It is recommended to set the validation timer to more than twice of the total reference validation measurement time. The frequency detection measurement time is

Buttons at the bottom include 'Show Instructions', '<-BACK', and 'NEXT>'.

Step 5C: Set the reference validation detectors configuration (continued)

- For reference frequencies ≥ 2 kHz

- Set the Frequency Detect Threshold
 - Frequency detection needs 4 parameters:
 - Valid threshold in ppm
 - Invalid threshold in ppm
 - Accuracy in ppm
 - Average count

Please read the instruction box (bullet 3) for more details on how to configure the frequency detector parameters.

- Set the Early Window Detector

- Determines T_{early}

- Set the Late/Missing Window Detector

- Determines T_{late}

- The reference input is considered valid if its next clock edge falls within the T_{early} and T_{late} range

Please read the instruction box (bullet 4) for more details on how to configure the early and late detector parameters.

- For a 1PPS reference

- Set the 1PPS Phase Detector

- Determines T_{jitter}

- The reference input is considered valid if its next clock edge falls within the T_{jitter} range

LMK05318B Wizard
Step 4: Set Reference Validation

	Enable	Timer	Enable	Amplitude Detector Mode	Vid = 200 mV Div or 400 mVpp Single-Ended
PRI	<input checked="" type="checkbox"/>	102.4 ms	<input checked="" type="checkbox"/>	Amplitude Detector Mode	Vid = 200 mV Div or 400 mVpp Single-Ended
SEC	<input checked="" type="checkbox"/>	102.4 ms	<input checked="" type="checkbox"/>	Amplitude Detector Mode	Vid = 200 mV Div or 400 mVpp Single-Ended

	Valid (ppm)	Invalid (ppm)	Accuracy (ppm)	Average (count)	Meas time	Enable	Cntr	T_{EARLY}	Enable	Cntr	T_{LATE}	Enable	Cntr	T_{JITTER}	
PRI	<input checked="" type="checkbox"/>	100	110	10	2	4.17 ms	<input checked="" type="checkbox"/>	1	6.40 ns	<input checked="" type="checkbox"/>	0	6.40 ns	<input type="checkbox"/>	0	n/a
SEC	<input checked="" type="checkbox"/>	100	110	10	2	4.17 ms	<input checked="" type="checkbox"/>	1	6.40 ns	<input checked="" type="checkbox"/>	0	6.40 ns	<input type="checkbox"/>	0	n/a

Early / Late Window Detector
Reference clock is valid if the next edge falls within this range

1 PPS Phase Detector
Reference clock is valid if the next edge falls within this range

INSTRUCTIONS:
If DPLL is disabled, then skip this page. All reference validation methods have been enabled or disabled automatically based on reference frequency and interface type. However, it is highly recommended to read through the instructions and loosen the thresholds according to application needs.
Frequency detection and early / late window detector are only valid for reference frequencies ≥ 2 kHz. 1-pps phase detector is only valid for reference frequencies < 2 kHz. For 1-pps input, only enable the 1-pps phase detector and disable all other detectors.
1. Validation timer. The reference must stay valid for "validation timer" amount of time before it's considered valid. It is recommended to set the validation timer to more than twice of the total reference validation measurement time. The frequency detection measurement time is

Step 6: Configure the DPLL

Step 6: Configure the DPLL

- Navigate to the **Set DPLL** page
- Set the DPLL loop bandwidth
 - The DPLL loop bandwidth needs to be lower than both PRREF and SECREF frequencies
- Set Tr peaking (dB) and Er peaking (dB)
 - Tr peaking is the maximum peaking (in dB) allowed for DPLL transfer function
 - default: Tr peaking = 0.1 dB
 - Er peaking is the maximum peaking (in dB) allowed for DPLL error function.
 - Default: Er peaking = 1 dB
- Set max TDC frequency
 - If no specific TDC frequency is required, set the max to 26 MHz
- Fastlock should only be disabled for 1pps input
- For most use cases, switchover method should always be set to 'hitless switching'.
- Click 'Run Script' button and wait for 1 ~ 2 minutes while the script is running. Make sure that the MATLAB runtime is installed as instructed in the first wizard page.

The screenshot shows the 'LMK05318B Wizard' software interface. The main window is titled 'Step 5: Set DPLL'. It contains a table with the following data:

Parameter	Target (Hz)	Actual (Hz)	Tr peaking (dB)	Er peaking (dB)
DPLL LBW	100	101.3	0.1	1

Below the table, there are several configuration options:

- Set default max TDC frequency: 26000000
- Fastlock: Enable Fastlock (default)
- Switchover: Hitless switching (default)
- Run Script button
- Display written DPLL registers (for debugging) checkbox

INSTRUCTIONS:

1. Set DPLL loop bandwidth. DPLL loop bandwidth needs to be lower than both PRREF and SECREF frequencies. Some applications have specific DPLL loop bandwidth requirements. If there are not, recommendations are: if any of the reference is 1 Hz, then set the loop bandwidth to 0.01 Hz. Otherwise, set it to 100 Hz.
2. Set Tr peaking (dB) and Er peaking (dB). Tr peaking is the maximum peaking (in dB) allowed for DPLL transfer function. Er peaking is the maximum peaking (in dB) allowed for DPLL error function. If there's no specific requirement, set them to default: Tr peaking = 0.1 dB, Er peaking = 1 dB.
3. Set max TDC frequency. If no specific TDC

The right side of the wizard shows a block diagram of the PLL system with components like PRREF, SECREF, R Dividers, Pre-dividers, TDC, Loop Filter, APLL1, BAW VCO (MHz), and a Fractional N divider.

Step 6: Configure the DPLL (continued)

- Navigate to the **Set DPLL (cont.)** page
- Configure the BAW Frequency Lock Detect
 - Disable if DPLL is enabled
 - Used to determine if BAW (VCO1) is locked
- Configure the DPLL Frequency Lock Detect
 - Used to determine if DPLL is frequency locked
- Configure the DPLL Phase Lock Detect
 - Used to determine if DPLL is phase locked
- Configure the Tuning Word History
 - This block sets the tuning word history for holdover.
 - Refer to datasheet section '9.3.7.4 Tuning Word History' for details.
- **The Instructions message box provides more information on how to configure the lock detectors and tuning word history settings. Please read for greater details.**

The screenshot shows the LMK05318B Wizard software interface. The title bar reads "TICS Pro - LMK05318B". The menu bar includes "File", "USB Communications", "Select Device", "Options", "Tools", "Default configuration", and "Help". The toolbar contains "Read All Regs", "Write All Regs", "Read Status Regs", "Soft-reset Chip", "Program EEPROM", and "Scan I2C Bus".

The left sidebar shows a tree view with the following items: LMK05318B, User Controls, Raw Registers, EVM Quick Start, Wizard, Set XO, Set outputs, Self reference, Ref validation, Set DPLL, **Set DPLL (cont.)** (highlighted), Save and Evaluate, Advanced, Status, EEPROM, and Burst Mode. Below the sidebar are "General" and "Context" tabs, and a text box labeled "s_wizard_dp112_message_box".

The main window is titled "LMK05318B Wizard" and "Step 6: Set DPLL (cont.)". It features an "INSTRUCTIONS:" message box on the left and several configuration panels on the right:

- BAW Frequency Lock Detect:** enable (checked), Set Default. Lock ppm: 5, Unlk ppm: 10, Average: 2, Acy (ppm): 1, Meas time: 19,2000 ms.
- DPLL Frequency Lock Detect:** enable (checked), Set Default. Lock ppm: 1, Unlk ppm: 10, Average: 10, Acy (ppm): 1, Meas time: 96,0000 ms.
- DPLL Phase Lock Detect:** Recommended. Lock cnt: 28, Lock thresh: 384.96 ps, Unlk cnt: 32, Unlk thresh: 6.16 ns, Meas time: 9.87 ms.
- Tuning Word History:** enable (checked), Min Values Required. Hist cnt: 0, Avg time: 115.34 ms, Delay cnt: 44, Delay time: 20.28 ms.

At the bottom right, there are "HIST_INTMD" (No intermediate update) and "DPLL_TUNING_FREE_RUN" (0) settings. A "Show Instructions" button is at the bottom left, and "<BACK" and "NEXT>" buttons are at the bottom right.

Appendix: Additional GUI Features

Appendix Introduction

- The following appendix slides will display additional features of the LMK05318B.
- Please note that these are features are not required for obtaining an initial configuration, but can be beneficial features after the initial configuration is created by following steps 1 to 6 on the previous slides.
- The additional features include:
 - Status page
 - DCO and ZDM page
 - Outputs page
 - EEPROM page
 - APLL1 page
 - APLL2 page
 - User controls page
 - Raw registers page

Status Page

- The Status Page can be used to validate the device is locking properly
- LOS_FDET_XO and LOS_XO indicate whether a clock is present at the XO input for the APLLs to lock to
 - When the bits are low, the XO is present and valid
- LOL_PLL1 and LOL_PLL2 indicate whether the APLLs are locking to the XO input
 - When the bits are low, the APLLs are locked properly
- LOPL_DPLL and LOFL_DPLL indicate whether the DPLL is frequency and phase locked to the REF input
 - When the bits are low, the DPLL has successfully locked to the REF input
- HLDOVR indicates whether the device is in holdover
- PRIREF_VALSTAT and SECREF_VALSTAT indicate whether the PRIREF or SECREF are present and validated by the reference validation detectors set in step 5
 - When the bits are high, the reference is valid

The screenshot shows the TICS Pro software interface for the LMK053188 device. The 'INTR Source' section has checkboxes for LOS_FDET_XO, LOL_PLL1, LOL_PLL2, LOS_XO, LOPL_DPLL, LOFL_DPLL, and HLDOVR. The 'INTR Flag Polarity' section has checkboxes for LOS_FDET_XO_POL, LOL_PLL1_POL, LOL_PLL2_POL, LOS_XO_POL, LOPL_DPLL_POL, and LOFL_DPLL_POL. The 'INTR Sticky Status' section has checkboxes for LOS_FDET_XO_INTR, LOL_PLL1_INTR, LOL_PLL2_INTR, LOS_XO_INTR, LOPL_DPLL_INTR, and LOFL_DPLL_INTR. The 'INTR Status Mask' section has checkboxes for LOS_FDET_XO_MASK, LOL_PLL1_MASK, LOL_PLL2_MASK, LOS_XO_MASK, LOPL_DPLL_MASK, and LOFL_DPLL_MASK. The 'By-pass' section has checkboxes for LOS_DET_XO and XO_DET_BYP. The 'Other APLL Status Registers' section has checkboxes for BAW_LOCK, PLL1_VM_INSIDE, and PLL2_VM_INSIDE. The 'DPLL's Reference Validated?' section has checkboxes for PRIREF_VALSTAT and SECREF_VALSTAT. The bottom of the screen shows pin configurations for Status0, Status1, and GPIO2.

EEPROM Page

- The EEPROM page contains the following features:
 - Program the EEPROM
 - To program the EEPROM, you must
 - Commit the register to the SRAM
 - Program the EEPROM
 - Export the GUI Map to a EEPROM file

TICS Pro - LMK053188

File USB communications Select Device Options Tools Default configuration Help

Read All Regs Write All Regs Read Status Regs Soft-reset Chip Program EEPROM Scan I2C Bus

LMK053188

- User Controls
- Raw Registers
- EVM Quick Start
- Wizard
 - Set XO
 - Set outputs
 - Set reference
 - Ref-validation
 - Set DPLL
 - Set DPLL
 - Save and Evaluate
- APLL1
- APLL2
- Outputs
- DCO, ZDM and Misc
- Slaves
- EEPROM
- Burst Mode

General Context

mt_c_USERNOTES

EEPROM / NVN Status (read only)

CRC Error Status

NVM Program Status

SRAM, EEPROM Programming Scripts

(1) Commit Registers & Extra Bytes -> Chip SRAM

(2) Program EEPROM <- SRAM

EEPROM File Export

Design Name Enter Design Name

User Notes Enter User Notes

Export GUI Map -> EEPROM File

Extra EEPROM Bytes

Address 10 0 = SLAVEADR[4:0] Write

Address 11 0 in bits [7:3] Write

Address 249 0 = EEREV[7:0] Write

Address 250 0

Address 251 0

Address 252 0

Read Extra EEPROM Bytes

REGCOMMIT

SRAM / EEPROM Map (display only)

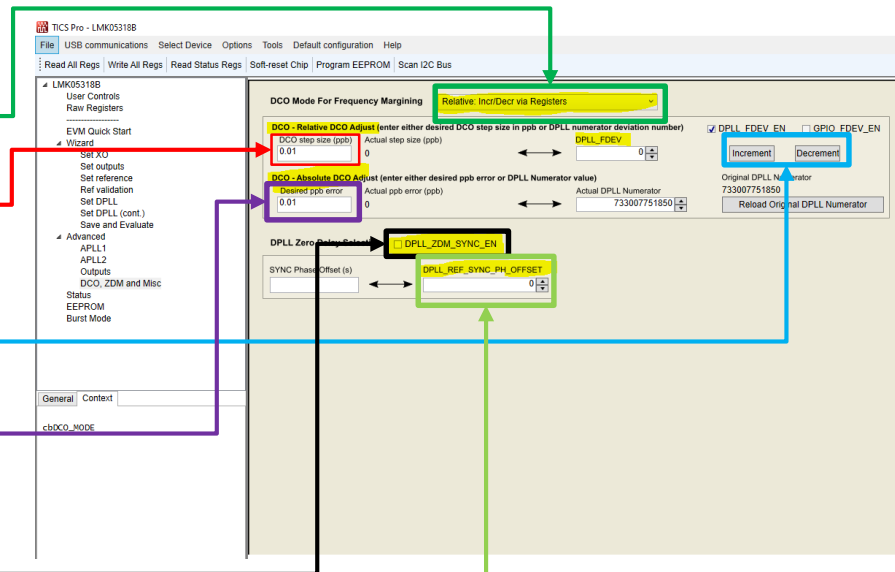
Wed May 25 14:31:34 2022

Registers Committed to SRAM and GUI Map: Base and Page 0

#	HADR	LADR	DATA	BYTE
# EEPROM BASEPAGE 0				
00	00	04	0	
00	01	0E	1	
00	02	17	2	
00	03	8E	3	
00	04	32	4	
00	05	01	5	
00	06	89	6	
00	07	20	7	
00	08	00	8	
00	09	64	9	
00	0A	C8	10	
00	0B	00	11	
00	0C	75	12	
00	0D	00	13	
00	0E	7F	14	
00	0F	FA	15	
00	10	2A	16	
00	11	AA	17	
00	12	80	18	
00	13	00	19	
00	14	00	20	
00	15	21	21	
00	16	DD	22	
00	17	0D	23	
00	18	29	24	
00	19	59	25	
00	1A	15	26	
00	1B	20	27	
00	1C	06	28	
00	1D	02	29	
00	1E	03	30	
00	1F	00	31	
00	20	1C	32	
00	21	23	33	
00	22	0C	34	
00	23	44	35	
00	24	3D	36	
00	25	09	37	
00	26	4C	38	

DCO and ZDM Page

- The DCO and ZDM Page can be used to:
 - Perform frequency/phase adjustments with the DCO
 - DCO adjustments can be performed relatively or absolutely
 - Select whether a relative or absolute adjustment is required
 - Relative adjustment
 - Enter a ppb adjustment that is required and a DPLL_FDEV will be calculated
 - The DPLL_FDEV will be the numerator deviation that will be adjusted from the DPLL numerator to result in the required ppb adjustment
 - Press the Increment or decrement button to add or subtract the required ppb adjustment
 - Absolute adjustment
 - Enter a ppb adjustment that is required and the output clock will automatically be adjusted by that ppb value
 - Enable zero-delay mode to achieve phase alignment between the input clock and output clock on OUT7
 - When the DPLL_ZDM_SYNC_EN is set, ZDM is enabled to achieve input and output phase alignment
 - The DPLL_REF_SYNC_PH_OFFSET can be used to adjust the phase offset between the input and output clocks



Outputs Page

- The channel muxes, channel dividers, output formats, and output frequencies shown on the outputs page are configured in step 4
- The outputs page provides the following additional features:
 - Output clock synchronization
 - Output sync can be accomplished by enabling the CHx_SYNC_EN bits highlighted in the image to the right
 - For the synchronization to take place, the SYNC_SW bit must be toggled (turned on/off)

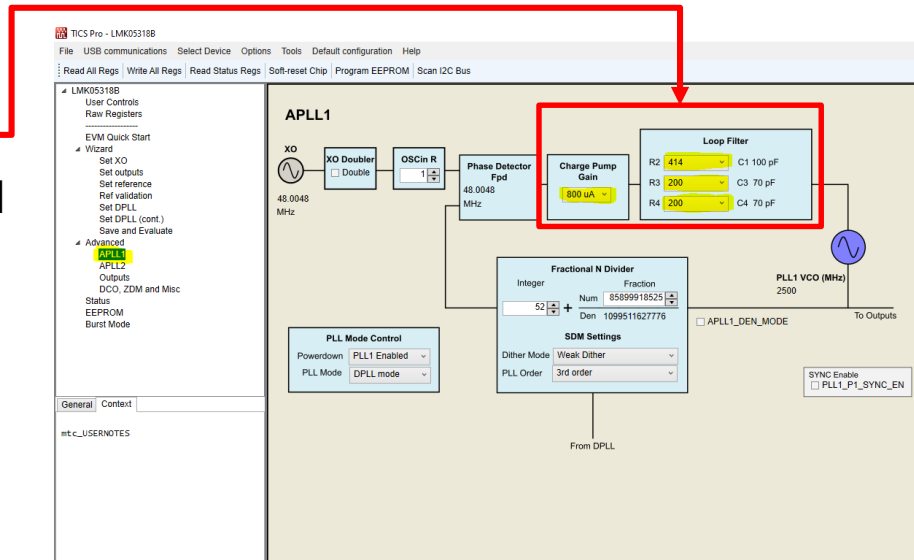
The screenshot shows the TI CICS Pro software interface for configuring the LMK053188. The 'Outputs' section is highlighted with a red box and a red arrow pointing to the 'SYNC_SW' bit. The 'Channel Muxes, Powerdowns' section shows channel dividers and muxes for APLL1 and APLL2. The 'Channel Dividers and Synchronization' section shows sync enable bits for each channel. The 'Output Drivers, Mute Options' section shows output drivers and mute options for each channel. The 'General' section shows the PLL2 Post Dividers configuration.

Channel Muxes, Powerdowns	Channel Dividers and Synchronization	Output Drivers, Mute Options
APLL1 P1 CH0_1_PD	16 CH0_1_SYNC_EN DIV0_1_DYN_DIV_SW	AC-LVPECL CH0_MUTE OUT0 156.25 MHz
APLL1 P1 CH2_3_PD	8 CH2_3_SYNC_EN DIV2_3_DYN_DIV_SW	AC-LVDS CH1_MUTE OUT1 156.25 MHz
APLL1 P1 CH4_PD	25 CH4_SYNC_EN DIV4_DYN_DIV_SW	AC-CML CH2_MUTE OUT2 312.5 MHz
APLL1 P1 CH5_PD	100 CH5_SYNC_EN DIV5_DYN_DIV_SW	HCSL(ext. 50R) CH3_MUTE OUT3 312.5 MHz
APLL2 P1 CH6_PD	13 CH6_SYNC_EN DIV6_DYN_DIV_SW	HCSL(int. 50R) CH4_MUTE OUT4 100.0 MHz
APLL2 P1 CH7_PD	1 PPS Divide Value: 13 12 0 CH7_SYNC_EN DIV7_DYN_DIV_SW	CMOS(+/-) CH5_MUTE OUT5 25.0 MHz
		CMOS(+/-HZ) CH6_MUTE OUT6 155.52 MHz
		CMOS(+/-HZ+) CH7_MUTE OUT7 155.52 MHz

Arrange PLL Post Dividers and Output Channels carefully to optimize jitter/ripples:
- Preferred channel assignment: PLL1 to OUT[0:3] bank, PLL2 to OUT[4:7] bank
- Group identical frequencies on adjacent channels
- Separate channels where (F_{OutN} - F_{OutM}) falls within the jitter integration BW (eg. 12 kHz - 20 MHz)
- Avoid / isolate CMOS outputs, or else use CMOS(+/-) or CMOS (+/-)

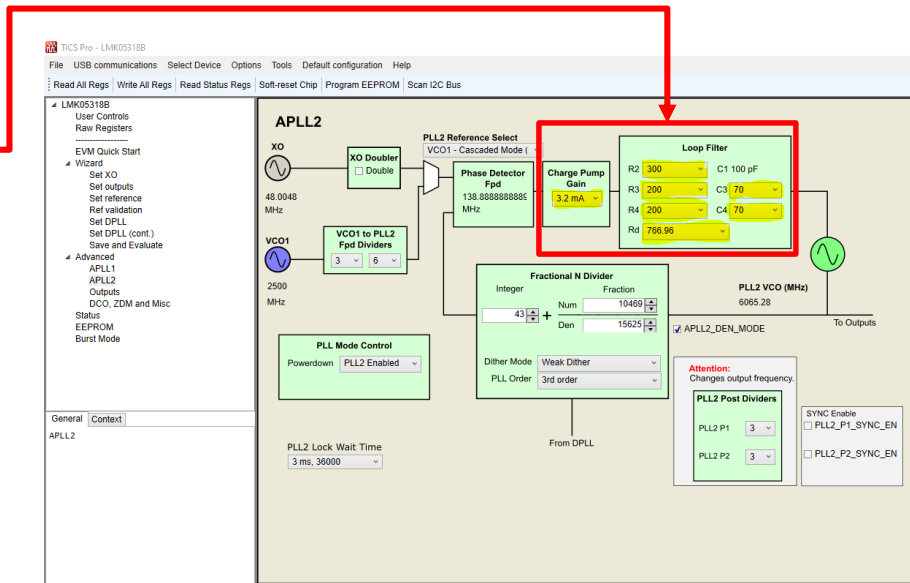
APLL1 Page

- The APLL1 page can be used to configure the charge pump current and loop filter to optimize the output clocks performance
- The rest of the controls on this page will be configured in step 4 and should not be change



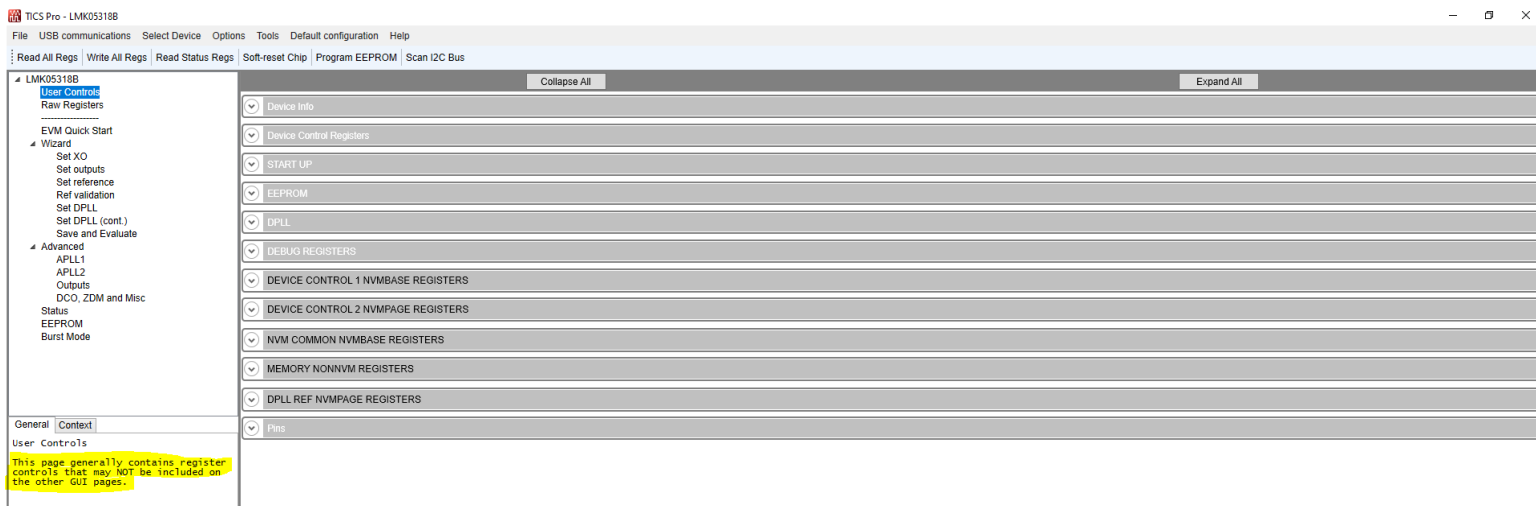
APLL2 Page

- The APLL2 page can be used to configure the charge pump current and loop filter to optimize the output clocks performance
- The rest of the controls on this page will be configured in step 4 or step 2 and should not be change



User Controls Page

- The user control page contains register controls that may not be included on the other GUI pages
 - For example, the device info registers such as PRTID, PRODID, etc.



The screenshot displays the TICS Pro - LMK053188 interface. The main window shows a list of expandable sections under the 'User Controls' heading. The sections are: Device Info, Device Control Registers, START UP, EEPROM, DPLL, DEBUG REGISTERS, DEVICE CONTROL 1 NVMBASE REGISTERS, DEVICE CONTROL 2 NVMPAGE REGISTERS, NVM COMMON NVMBASE REGISTERS, MEMORY NONNVM REGISTERS, DPLL REF NVMPAGE REGISTERS, and Pins. The left sidebar shows a tree view with 'User Controls' selected. A yellow highlight is present on the 'User Controls' section in the left sidebar, with a text box stating: 'This page generally contains register controls that may NOT be included on the other GUI pages.'

Raw Registers Page

- The raw register page allows for low-level register write/read operations by register address

The screenshot shows the 'Raw Registers' page for the LMK05318B device. The interface includes a menu bar with options like 'Read All Regs', 'Write All Regs', and 'Soft-reset Chip'. A sidebar on the left contains navigation options such as 'Line Controls', 'Raw Registers', and 'Advanced'. The main area displays a table of registers with columns for 'Register Name', 'Address/Value', and 'Data'. The 'Data' column shows the current value of each register in hexadecimal. On the right side, there are buttons for 'Write Register', 'Read Register', 'Read All Registers', and 'Write All Registers', along with a 'Read' button for the selected register.

Register Name	Address/Value	Data
R0	0x000010	00000000000000000000000000000000
R1	0x000016	00000000000000000000000000000000
R2	0x000018	00000000000000000000000000000000
R3	0x00001E	00000000000000000000000000000000
R4	0x000024	00000000000000000000000000000000
R5	0x00002A	00000000000000000000000000000000
R6	0x000030	00000000000000000000000000000000
R7	0x000036	00000000000000000000000000000000
R8	0x00003C	00000000000000000000000000000000
R9	0x000042	00000000000000000000000000000000
R10	0x000048	00000000000000000000000000000000
R11	0x00004E	00000000000000000000000000000000
R12	0x000054	00000000000000000000000000000000
R13	0x00005A	00000000000000000000000000000000
R14	0x000060	00000000000000000000000000000000
R15	0x000066	00000000000000000000000000000000
R16	0x00006C	00000000000000000000000000000000
R17	0x000072	00000000000000000000000000000000
R18	0x000078	00000000000000000000000000000000
R19	0x00007E	00000000000000000000000000000000
R20	0x000084	00000000000000000000000000000000
R21	0x00008A	00000000000000000000000000000000
R22	0x000090	00000000000000000000000000000000
R23	0x000096	00000000000000000000000000000000
R24	0x00009C	00000000000000000000000000000000
R25	0x0000A2	00000000000000000000000000000000
R26	0x0000A8	00000000000000000000000000000000
R27	0x0000AE	00000000000000000000000000000000
R28	0x0000B4	00000000000000000000000000000000
R29	0x0000BA	00000000000000000000000000000000
R30	0x0000C0	00000000000000000000000000000000
R31	0x0000C6	00000000000000000000000000000000
R32	0x0000CC	00000000000000000000000000000000
R33	0x0000D2	00000000000000000000000000000000
R34	0x0000D8	00000000000000000000000000000000
R35	0x0000DE	00000000000000000000000000000000
R36	0x0000E4	00000000000000000000000000000000
R37	0x0000EA	00000000000000000000000000000000
R38	0x0000F0	00000000000000000000000000000000
R39	0x0000F6	00000000000000000000000000000000
R40	0x0000FC	00000000000000000000000000000000
R41	0x000102	00000000000000000000000000000000
R42	0x000108	00000000000000000000000000000000
R43	0x00010E	00000000000000000000000000000000
R44	0x000114	00000000000000000000000000000000
R45	0x00011A	00000000000000000000000000000000
R46	0x000120	00000000000000000000000000000000
R47	0x000126	00000000000000000000000000000000
R48	0x00012C	00000000000000000000000000000000
R49	0x000132	00000000000000000000000000000000
R50	0x000138	00000000000000000000000000000000
R51	0x00013E	00000000000000000000000000000000
R52	0x000144	00000000000000000000000000000000
R53	0x00014A	00000000000000000000000000000000