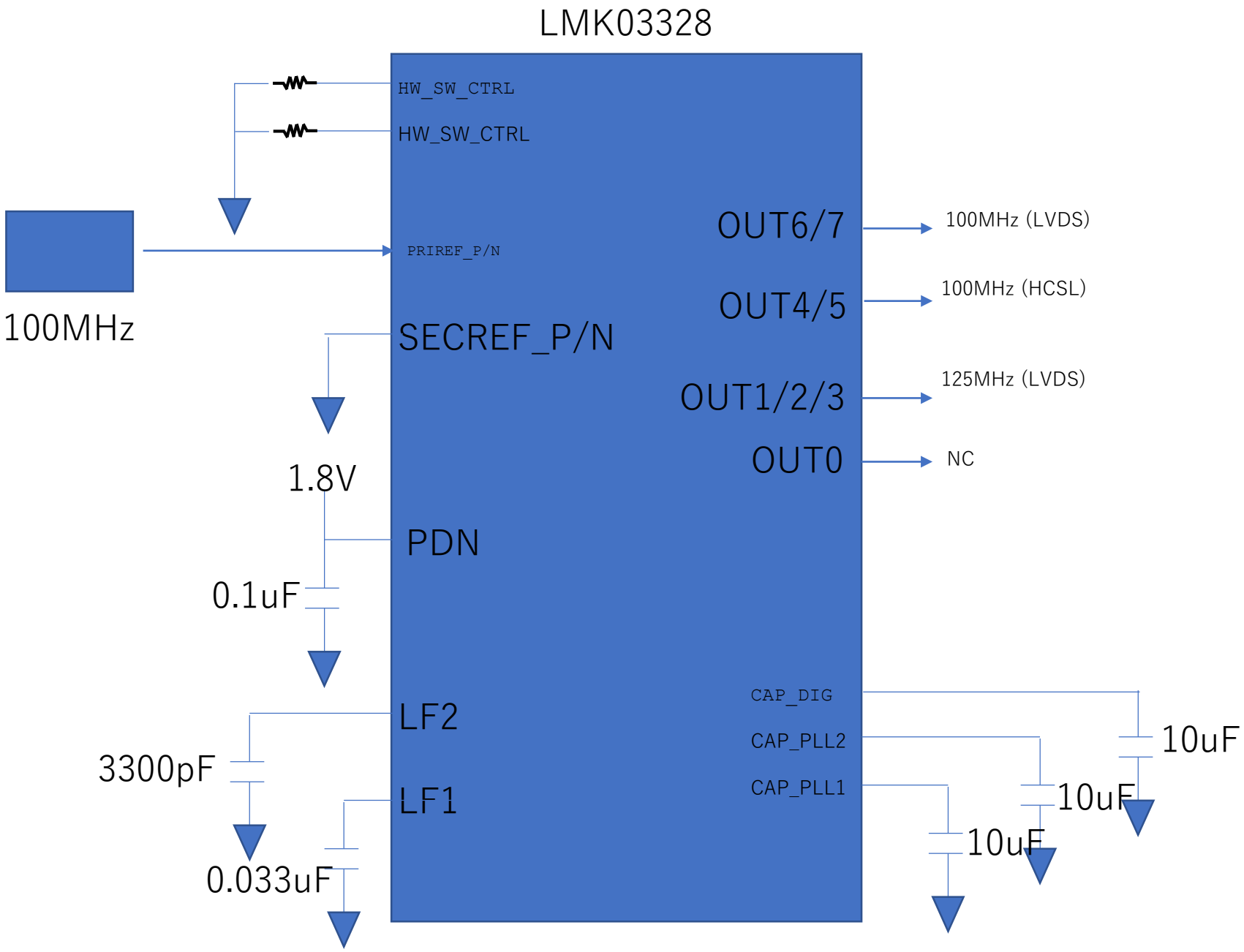
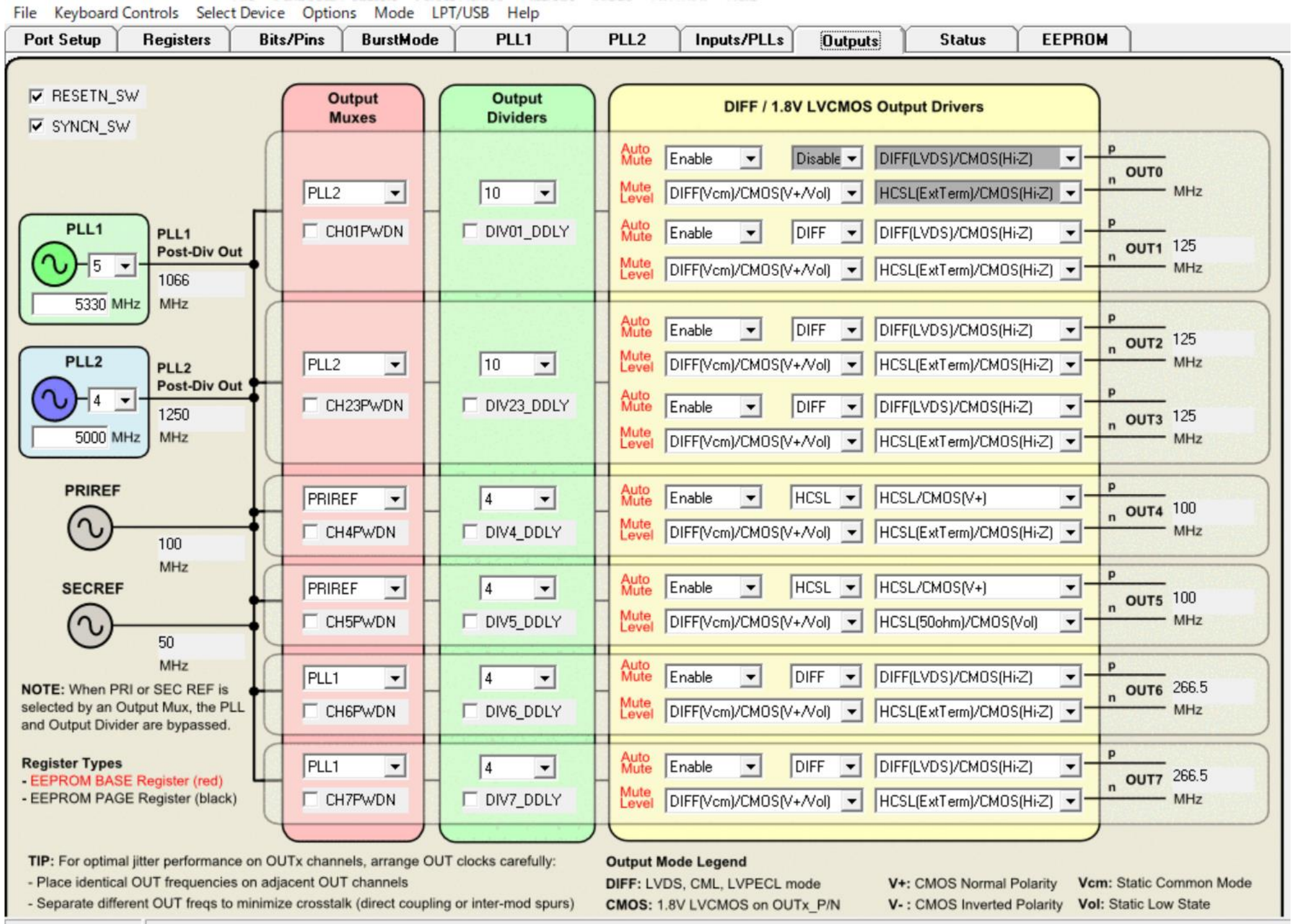
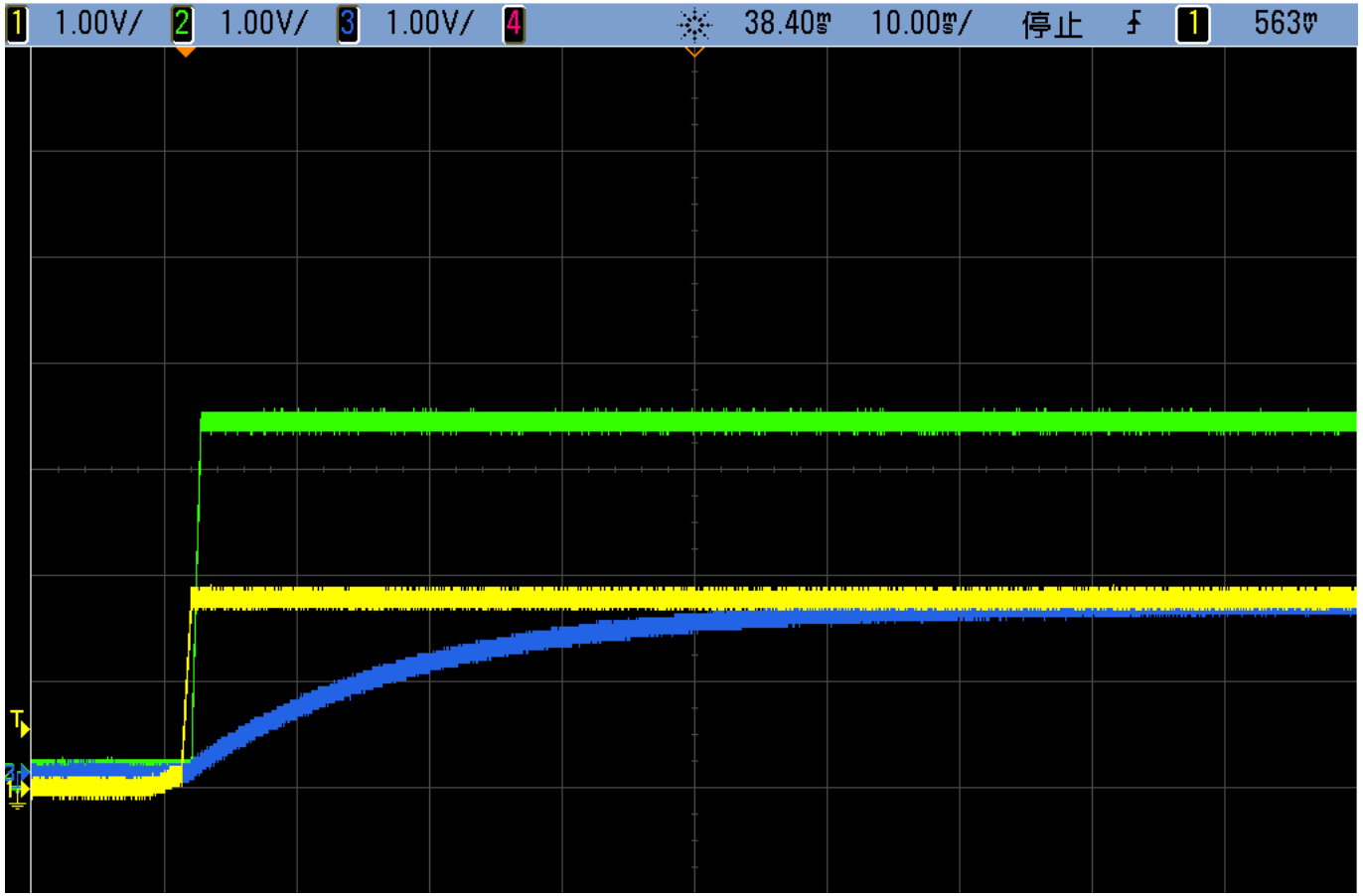


VDDO_x : 1.8V
VDD_PLLx: 3.3V
VDD_IN: 3.3V
VDD_DIG 3.3V


File Keyboard Controls Select Device Options Mode LPT/USB Help
Port Setup
Registers
Bits/Pins
BurstMode
PLL1
PLL2
Inputs/PLLs
Outputs
Status
EEPROM
RESETN_SW
SYNCN_SW
Output Muxes
Output Dividers
DIFF / 1.8V LVCMOS Output Drivers
PLL1
5
5330 MHz
PLL1 Post-Div Out
1066 MHz
PLL2
4
5000 MHz
PLL2 Post-Div Out
1250 MHz
PRIREF
100 MHz
SECREF
50 MHz
NOTE: When PRI or SEC REF is selected by an Output Mux, the PLL and Output Divider are bypassed.
Register Types
- EEPROM BASE Register (red)
- EEPROM PAGE Register (black)
PLL2
10
CH01PWDN
DIV01_DDLY
Auto Mute
Enable
Disable
DIFF(LVDS)/CMOS(Hi-Z)
Mute Level
DIFF(Vcm)/CMOS(V+/Vol)
HCSL(ExtTerm)/CMOS(Hi-Z)
DIFF
OUT0
OUT1 125 MHz
PLL2
10
CH23PWDN
DIV23_DDLY
OUT2 125 MHz
OUT3 125 MHz
PRIREF
4
CH4PWDN
DIV4_DDLY
HCSL
HCSL/CMOS(V+)
OUT4 100 MHz
PRIREF
4
CH5PWDN
DIV5_DDLY
HCSL(50ohm)/CMOS(Vol)
OUT5 100 MHz
PLL1
4
CH6PWDN
DIV6_DDLY
OUT6 266.5 MHz
PLL1
4
CH7PWDN
DIV7_DDLY
OUT7 266.5 MHz
TIP: For optimal jitter performance on OUTx channels, arrange OUT clocks carefully:
- Place identical OUT frequencies on adjacent OUT channels
- Separate different OUT freqs to minimize crosstalk (direct coupling or inter-mod spurs)
Output Mode Legend
DIFF: LVDS, CML, LVPECL mode
CMOS: 1.8V LVCMOS on OUTx_P/N
V+: CMOS Normal Polarity
V- : CMOS Inverted Polarity
Vcm: Static Common Mode
Vol: Static Low State

Power-up sequence



Green: 3.3V

Yellow: 1.8V

Blue: 1.8V(PDN)

PDN is delayed with
External 0.1uF.
200kΩ(internal) x 0.1uF
=20ms(63% charged)