Datasheet P22

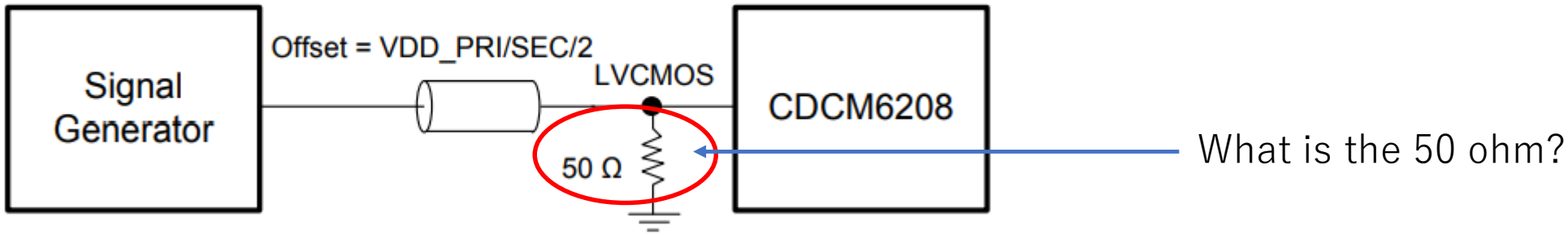


Figure.15 LVCMOS Input DC Configuration During Device Test

Datasheet P82

Replace to 0 ohm resister.

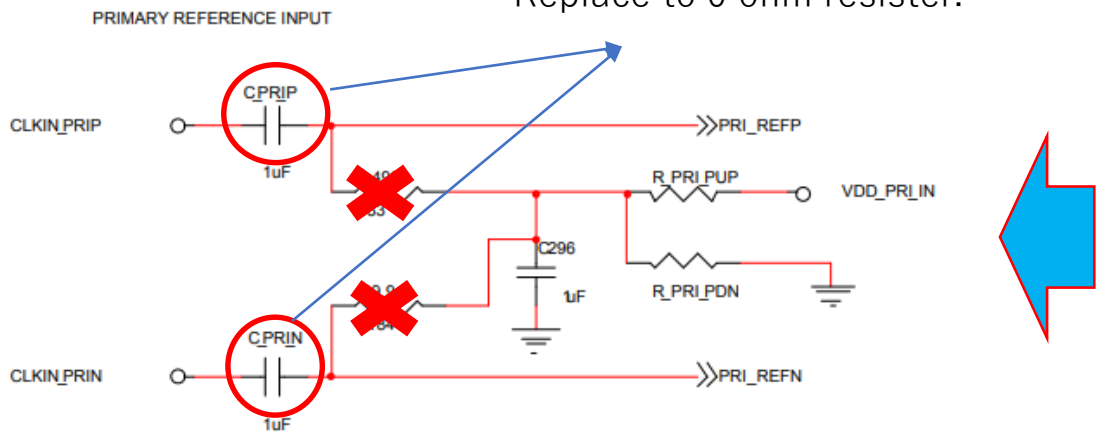
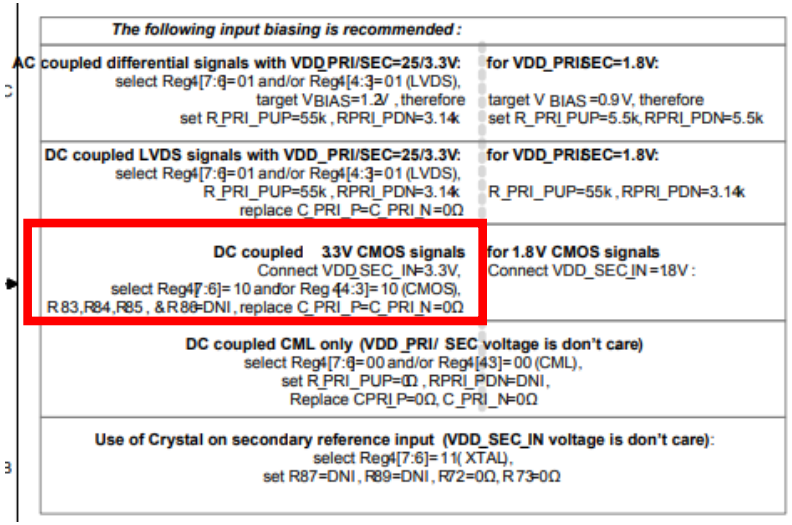


Figure 67. Schematic Page 2(PRIMARY REFERENCE INPUT)



The following input biasing is recommended :	
AC coupled differential signals with VDD_PRI/SEC=25/3.3V: select Reg4[7:6]=01 and/or Reg4[4:3]=01 (LVDS), target VBIAS=1.2V , therefore set R_PRI_PUP=55k , RPRI_PDN=3.14k	**for VDD_PRI/SEC=1.8V:** target V BIAS =0.9 V, therefore set R_PRI_PUP=5.5k, RPRI_PDN=5.5k
DC coupled LVDS signals with VDD_PRI/SEC=25/3.3V: select Reg4[7:6]=01 and/or Reg4[4:3]=01 (LVDS), R_PRI_PUP=55k , RPRI_PDN=3.14k replace C_PRI_P=C_PRI_N=0Ω	**for VDD_PRI/SEC=1.8V:** R_PRI_PUP=55k , RPRI_PDN=3.14k
DC coupled 3.3V CMOS signals Connect VDD_SEC_IN=3.3V, select Reg4[7:6]= 10 and/or Reg 4[4:3]= 10 (CMOS), R 83,R84,R85 , & R86=DNI , replace C_PRI_P=C_PRI_N=0Ω	**for 1.8 V CMOS signals** Connect VDD_SEC_IN = 1.8V :
DC coupled CML only (VDD_PRI/ SEC voltage is don't care) select Reg4[7:6]=00 and/or Reg4[4:3]= 00 (CML), set R_PRI_PUP=0Ω , RPRI_PDN=DNI , Replace CPRI_P=0Ω, C_PRI_N=0Ω	
Use of Crystal on secondary reference input (VDD_SEC_IN voltage is don't care): select Reg4[7:6]= 11(XTAL), set R87=DNI , R89=DNI , R72=0Ω, R 73=0Ω	