

Flat top, seen on eval board and on own board



Non flat top, having hit <rt> in Code Loader. Have not been able to get this to work yet on own board



Screen grab of Code Loader

LMX2492

File Keyboard Controls Select Device Options Mode LPT/USB Help

Port Setup Registers Bits/Pins BurstMode PLL Ramp Calculator

Update All For effect, must enable FlexScript before pressing update all button. If not enabled, click Options --> Enable Flex Scripts.

Controls on grey background/box such as this message are not for user input

MSB -->

VCO Output Limit

High 10000 MHz
Low 1000 MHz

Valid In Ramps 0 1 2 3 4 5 6 7

CMP0 9400 MHz
CMP1 9800 MHz

OSCin Frequency 100 MHz Must enter to match PLL Fpd 100 MHz

VCO Start Frequency 9600 MHz Accumulator Start 1610612736

Sign	Decimal Value	2s complement (programmed register) [32:31]	RAMP_LIMIT_x[30:0]
High 0	67108864	0	67108864
Low 1	1442840576	3	704643072

Sign	Decimal Value	[32:31]	RAMP_CMPx[30:0]
CMP0 1	33554432	3	2113929216
CMP1 0	33554432	0	33554432

PLL_R	PLL_NUM
1	0

PLL_N	PLL_DEN
96	16777216

Ramps Ramp Enable

Ramp Number	Actual Start Frequency (MHz)	Desired End Frequency (MHz)	Actual End Frequency (MHz)	Duration (us)	Dly	Next Ramp	Start next ramp after	RST	FL	Flags	Length	Increment (dec)
0	9600	9700	9700.001692771	25	1	TOC Timeout		<input checked="" type="checkbox"/>	<input type="checkbox"/>	Disabled	2500	6711
1	9700.001692771	9600	9599.999403953	4	0	TOC Timeout		<input type="checkbox"/>	<input type="checkbox"/>	Disabled	400	-41944
2	-1	9750	-1	100	0	TOC Timeout		<input type="checkbox"/>	<input type="checkbox"/>	Disabled	10000	16778
3	-1	9550	-1	1	0	TOC Timeout		<input type="checkbox"/>	<input type="checkbox"/>	Disabled	100	-1342208
4	-1	9600	-1	256	0	TOC Timeout		<input type="checkbox"/>	<input type="checkbox"/>	Disabled	25600	203162
5	-1	9450	-1	1	0	TOC Timeout		<input type="checkbox"/>	<input type="checkbox"/>	Disabled	100	-1006735
6	-1	9800	-1	256	0	TOC Timeout		<input type="checkbox"/>	<input type="checkbox"/>	Disabled	25600	208404
7	-1	10600	-1	100	0	TOC Timeout		<input type="checkbox"/>	<input type="checkbox"/>	Disabled	10000	53688

Ramp Count 0 Ramp Auto RAMP_AUTO Ramp In Source Ramp Transition

Increment (2s complement) Programmed Register

0	6711	4	0
1	1073699880	5	0
2	0	6	0
3	0	7	0

Trigger Source A Disabled
Trigger Source B Disabled
Trigger Source C Disabled

FSK Trigger Disabled
FSK Deviation 0
Phase Mod. En RAMP_PM_EN

Dump of registers from Code Loader in both states, there is no change in the register values, see difference column:

flat top			none flat top			Difference	
R141	0x008D00	0	R141	0x008D00	0	0	RAMP7
R140	0x008C27	39	R140	0x008C27	39	0	RAMP7
R139	0x008B10	16	R139	0x008B10	16	0	RAMP7
R138	0x008A00	0	R138	0x008A00	0	0	RAMP7
R137	0x008900	0	R137	0x008900	0	0	RAMP7
R136	0x008800	0	R136	0x008800	0	0	RAMP7
R135	0x008700	0	R135	0x008700	0	0	RAMP7
R134	0x008600	0	R134	0x008600	0	0	RAMP6
R133	0x008564	100	R133	0x008564	100	0	RAMP6
R132	0x008400	0	R132	0x008400	0	0	RAMP6
R131	0x008300	0	R131	0x008300	0	0	RAMP6
R130	0x008200	0	R130	0x008200	0	0	RAMP6
R129	0x008100	0	R129	0x008100	0	0	RAMP6
R128	0x008000	0	R128	0x008000	0	0	RAMP6
R127	0x007F00	0	R127	0x007F00	0	0	RAMP5
R126	0x007E00	0	R126	0x007E00	0	0	RAMP5
R125	0x007D64	100	R125	0x007D64	100	0	RAMP5
R124	0x007C00	0	R124	0x007C00	0	0	RAMP5
R123	0x007B00	0	R123	0x007B00	0	0	RAMP5
R122	0x007A00	0	R122	0x007A00	0	0	RAMP5
R121	0x007900	0	R121	0x007900	0	0	RAMP5
R120	0x007800	0	R120	0x007800	0	0	RAMP4
R119	0x007764	100	R119	0x007764	100	0	RAMP4
R118	0x007600	0	R118	0x007600	0	0	RAMP4
R117	0x007500	0	R117	0x007500	0	0	RAMP4
R116	0x007400	0	R116	0x007400	0	0	RAMP4
R115	0x007300	0	R115	0x007300	0	0	RAMP4
R114	0x007200	0	R114	0x007200	0	0	RAMP4
R113	0x007100	0	R113	0x007100	0	0	RAMP3
R112	0x007000	0	R112	0x007000	0	0	RAMP3
R111	0x006F64	100	R111	0x006F64	100	0	RAMP3
R110	0x006E00	0	R110	0x006E00	0	0	RAMP3
R109	0x006D00	0	R109	0x006D00	0	0	RAMP3
R108	0x006C00	0	R108	0x006C00	0	0	RAMP3
R107	0x006B00	0	R107	0x006B00	0	0	RAMP3
R106	0x006A00	0	R106	0x006A00	0	0	RAMP2
R105	0x006927	39	R105	0x006927	39	0	RAMP2
R104	0x006810	16	R104	0x006810	16	0	RAMP2
R103	0x006700	0	R103	0x006700	0	0	RAMP2
R102	0x006600	0	R102	0x006600	0	0	RAMP2
R101	0x006500	0	R101	0x006500	0	0	RAMP2
R100	0x006400	0	R100	0x006400	0	0	RAMP2

R99	0x006300	0	R99	0x006300	0	0	RAMP1
R98	0x006201	1	R98	0x006201	1	0	RAMP1
R97	0x006190	144	R97	0x006190	144	0	RAMP1
R96	0x00603F	63	R96	0x00603F	63	0	RAMP1
R95	0x005FFF	255	R95	0x005FFF	255	0	RAMP1
R94	0x005E5C	92	R94	0x005E5C	92	0	RAMP1
R93	0x005D28	40	R93	0x005D28	40	0	RAMP1
							RAMP0 other bits, like next which is s
R92	0x005C24	36	R92	0x005C24	36	0	one
R91	0x005B09	9	R91	0x005B09	9	0	RAMP0_LEN[18:8]
R90	0x005AC4	196	R90	0x005AC4	196	0	RAMP0_LEN[7:0]
R89	0x005900	0	R89	0x005900	0	0	RAMP0_INC[29:24]
R88	0x005800	0	R88	0x005800	0	0	RAMP0_INC[23:16]
R87	0x00571A	26	R87	0x00571A	26	0	RAMP0_INC[15:8]
R86	0x005637	55	R86	0x005637	55	0	RAMP0_INC[7:0]
R85	0x005500	0	R85	0x005500	0	0	Reserved
R84	0x005400	0	R84	0x005400	0	0	Ramp count
R83	0x005300	0	R83	0x005300	0	0	Ramp count
R82	0x005204	4	R82	0x005204	4	0	Ramp limit high
R81	0x005100	0	R81	0x005100	0	0	Ramp limit high
R80	0x005000	0	R80	0x005000	0	0	Ramp limit high
R79	0x004F00	0	R79	0x004F00	0	0	Ramp limit high
R78	0x004EAA	170	R78	0x004EAA	170	0	Ramp limit low
R77	0x004D00	0	R77	0x004D00	0	0	Ramp limit low
R76	0x004C00	0	R76	0x004C00	0	0	Ramp limit low
R75	0x004B00	0	R75	0x004B00	0	0	Ramp limit low
R74	0x004A00	0	R74	0x004A00	0	0	FSK_DEV
R73	0x004900	0	R73	0x004900	0	0	FSK_DEV
R72	0x004800	0	R72	0x004800	0	0	FSK_DEV
R71	0x004700	0	R71	0x004700	0	0	FSK_DEV
R70	0x004609	9	R70	0x004609	9	0	Ramp bitns
R69	0x004500	0	R69	0x004500	0	0	RAMP_CMP1
R68	0x004402	2	R68	0x004402	2	0	RAMP_CMP1
R67	0x004300	0	R67	0x004300	0	0	RAMP_CMP1
R66	0x004200	0	R66	0x004200	0	0	RAMP_CMP1
R65	0x004100	0	R65	0x004100	0	0	RAMP_CMP1
R64	0x004000	0	R64	0x004000	0	0	RAMP_CMP0
R63	0x003FFE	254	R63	0x003FFE	254	0	RAMP_CMP0
R62	0x003E00	0	R62	0x003E00	0	0	RAMP_CMP0
R61	0x003D00	0	R61	0x003D00	0	0	RAMP_CMP0
R60	0x003C00	0	R60	0x003C00	0	0	RAMP_CMP0
R59	0x003B00	0	R59	0x003B00	0	0	RAMP TRIG
R58	0x003A01	1	R58	0x003A01	1	0	RAMP TRIG, LSB is ramp enable
R57	0x003900	0	R57	0x003900	0	0	Reserved
R56	0x00380F	15	R56	0x00380F	15	0	Reserved
R55	0x00376F	111	R55	0x00376F	111	0	Reserved

R54	0x00366F	111	R54	0x00366F	111	0	Reserved
R53	0x00350F	15	R53	0x00350F	15	0	Reserved
R52	0x00348F	143	R52	0x00348F	143	0	Reserved
R51	0x00330F	15	R51	0x00330F	15	0	Reserved
R50	0x00320F	15	R50	0x00320F	15	0	Reserved
R49	0x0031AF	175	R49	0x0031AF	175	0	Reserved
R48	0x00300F	15	R48	0x00300F	15	0	Reserved
R47	0x002F4F	79	R47	0x002F4F	79	0	Reserved
R46	0x002E30	48	R46	0x002E30	48	0	Reserved
R45	0x002D00	0	R45	0x002D00	0	0	Reserved
R44	0x002C00	0	R44	0x002C00	0	0	Reserved
R43	0x002B00	0	R43	0x002B00	0	0	Reserved
R42	0x002A00	0	R42	0x002A00	0	0	Reserved
R41	0x002900	0	R41	0x002900	0	0	Reserved
R40	0x002800	0	R40	0x002800	0	0	Reserved
R39	0x002752	82	R39	0x002752	82	0	MUX
R38	0x002618	24	R38	0x002618	24	0	MUX
R37	0x002510	16	R37	0x002510	16	0	MUX
R36	0x002408	8	R36	0x002408	8	0	MUX
R35	0x002341	65	R35	0x002341	65	0	MUX
R34	0x002204	4	R34	0x002204	4	0	DLD
R33	0x002120	32	R33	0x002120	32	0	DLD
R32	0x002000	0	R32	0x002000	0	0	FL_TOC
R31	0x001F2E	46	R31	0x001F2E	46	0	CMP
R30	0x001E04	4	R30	0x001E04	4	0	CPM
R29	0x001D00	0	R29	0x001D00	0	0	FL_TOC
R28	0x001C1F	31	R28	0x001C1F	31	0	CPG
R27	0x001B08	8	R27	0x001B08	8	0	Various
R26	0x001A00	0	R26	0x001A00	0	0	PLL_R
R25	0x001901	1	R25	0x001901	1	0	PLL_R
R24	0x001800	0	R24	0x001800	0	0	FRAC_DEN
R23	0x001703	3	R23	0x001703	3	0	FRAC_DEN
R22	0x0016E8	232	R22	0x0016E8	232	0	FRAC_DEN
R21	0x001500	0	R21	0x001500	0	0	FRAC_NUM
R20	0x001400	0	R20	0x001400	0	0	FRAC_NUM
R19	0x001300	0	R19	0x001300	0	0	FRAC_NUM
R18	0x00122C	44	R18	0x00122C	44	0	FRAC and PLL[17:16]
R17	0x001100	0	R17	0x001100	0	0	PLL_N[15:8]
R16	0x001060	96	R16	0x001060	96	0	PLL_N[7:0]
R15	0x000F00	0	R15	0x000F00	0	0	Reserved
R14	0x000E00	0	R14	0x000E00	0	0	Reserved
R13	0x000D00	0	R13	0x000D00	0	0	Reserved
R12	0x000C00	0	R12	0x000C00	0	0	Reserved
R11	0x000B00	0	R11	0x000B00	0	0	Reserved
R10	0x000A00	0	R10	0x000A00	0	0	Reserved
R9	0x000900	0	R9	0x000900	0	0	Reserved

R8	0x000800	0	R8	0x000800	0	0	Reserved
R7	0x000700	0	R7	0x000700	0	0	Reserved
R6	0x000600	0	R6	0x000600	0	0	Reserved
R5	0x000500	0	R5	0x000500	0	0	Reserved
R4	0x000400	0	R4	0x000400	0	0	Reserved
R3	0x000300	0	R3	0x000300	0	0	Reserved
R2	0x000201	1	R2	0x000201	1	0	Control
R1	0x000100	0	R1	0x000100	0	0	Reserved
R0	0x000018	24	R0	0x000018	24	0	