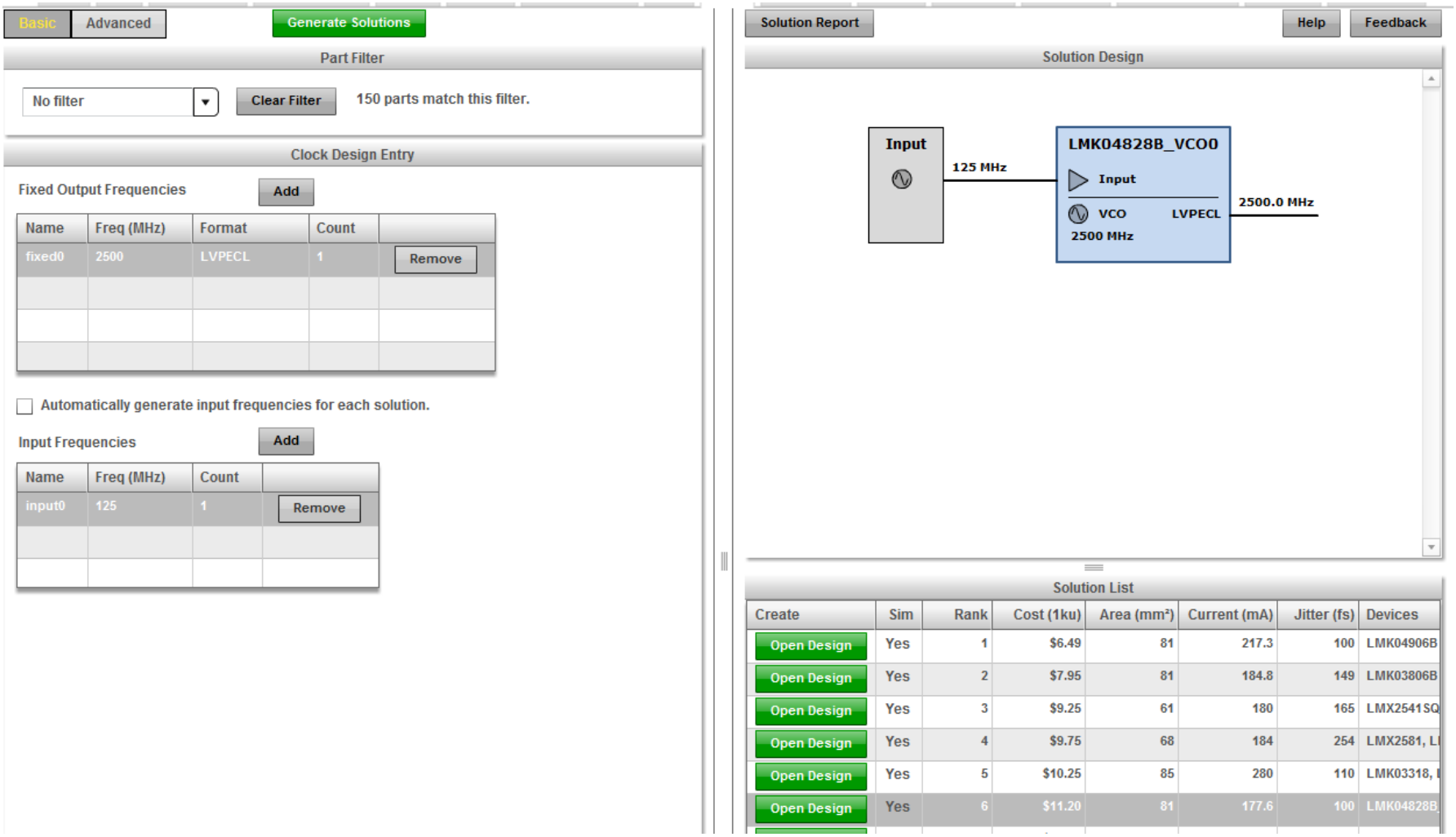
Using Clock Architect as of 2017-03-21 with dual loop devices

This document shows the process of simulating dual loop PLLs in Clock Architect and the design that's necessary to achieve best performance. In this document a design showing 119.6 fs rms can be **improved to 84.1 fs rms. Best performance is achieved when only LMK0482x is contributing to final phase noise/jitter.**

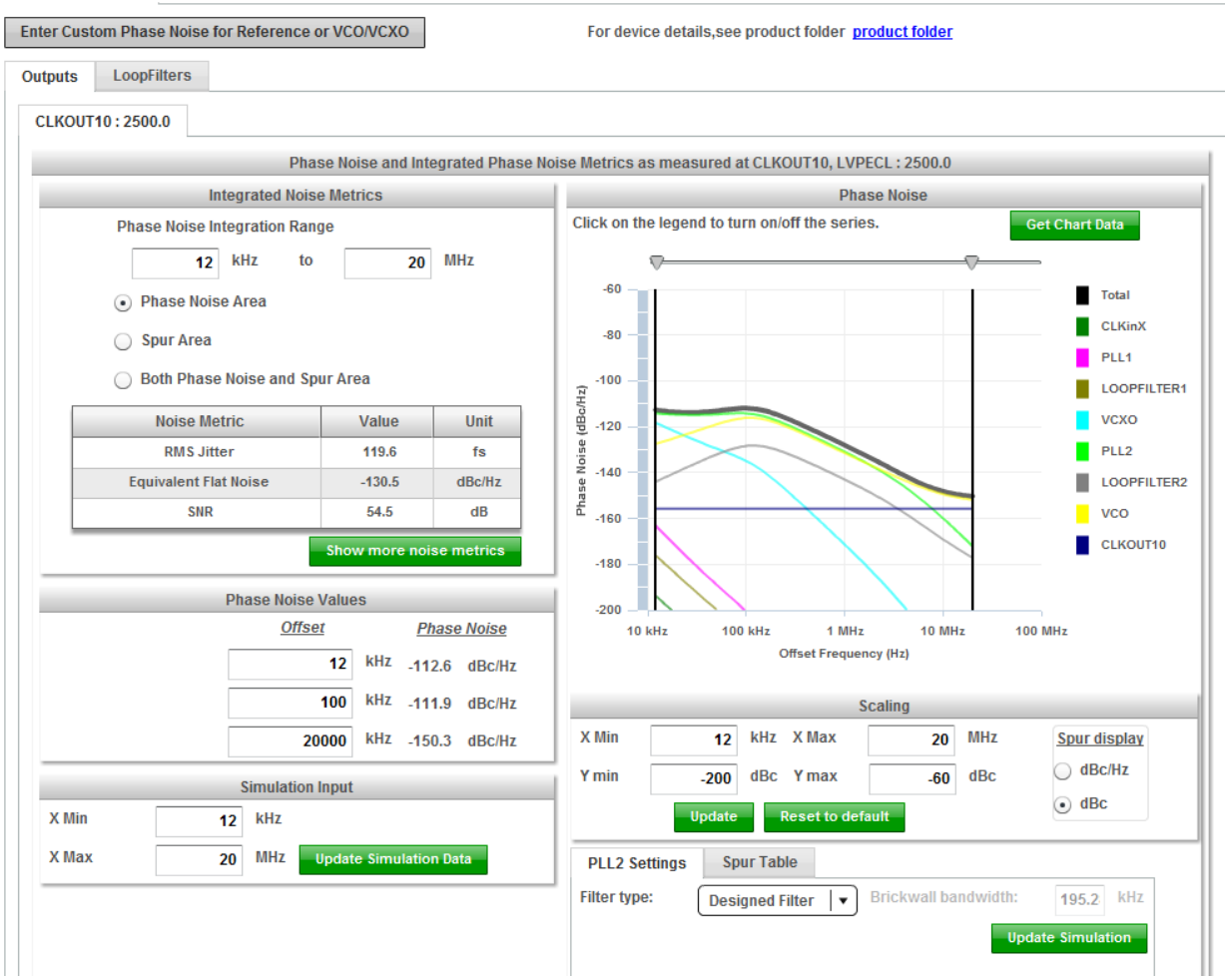
See last slide on using Clock Architect with LMK0482x for single loop devices.

Enter conditions, then open design.



Initial sim results

- Need to set jitter integration range to needed range for application.
- Need to update VCXO information
  - Frequency
  - Phase Noise
  - Loop filter
- Need to update PLL2 loop filter based on updated VCXO.



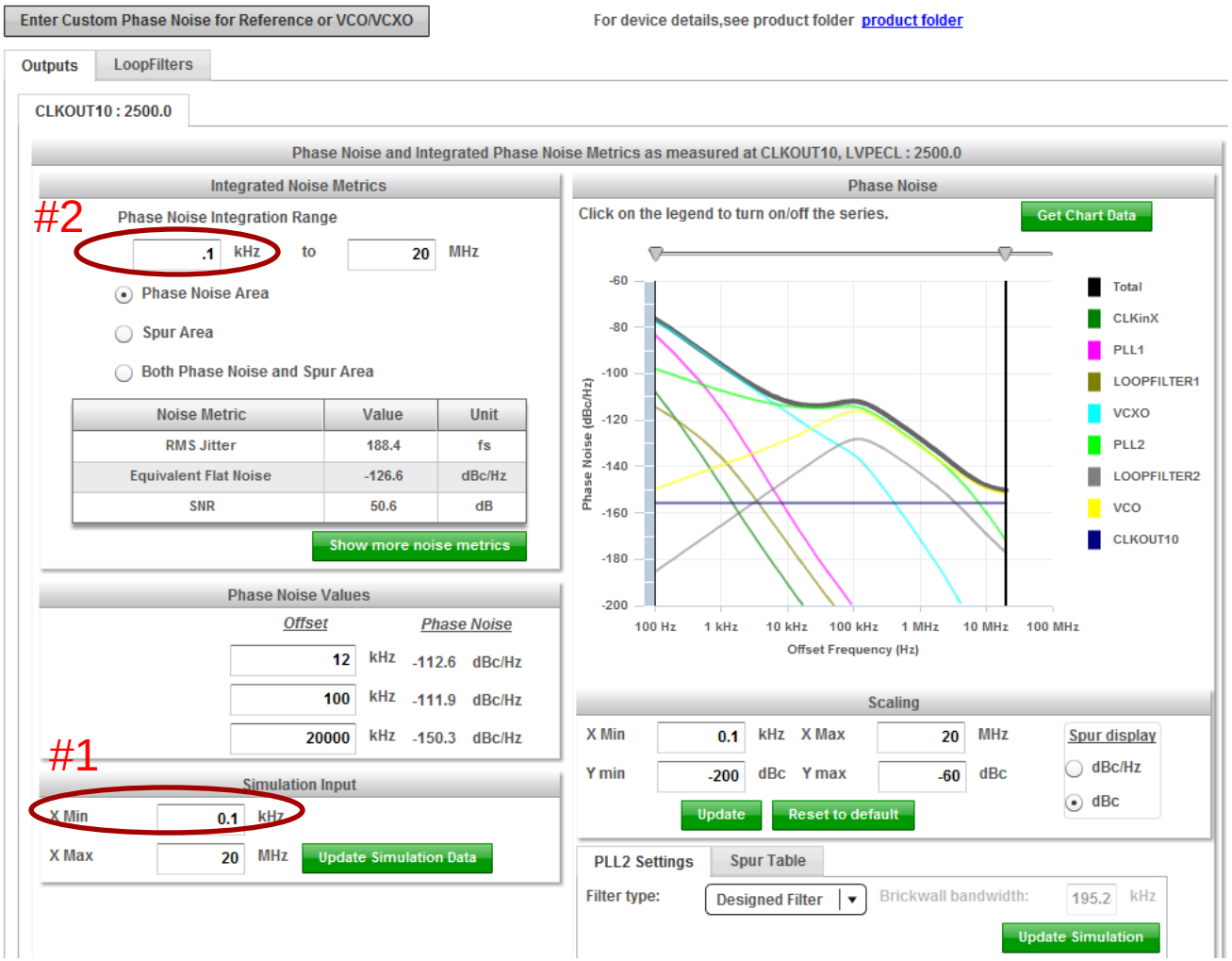
Note 12 kHz to 20 MHz integration = 119.6 fs rms

Our requirements

- Using a VCXO of 125 MHz
  - VCXO with phase noise profile as below
    - 10 Hz -76 dBc/Hz
    - 100 Hz -109 dBc/Hz
    - 1 kHz -137 dBc/Hz
    - 10 kHz -152 dBc/Hz
    - 100 kHz -160 dBc/Hz
    - 1 MHz -164 dBc/Hz

Updating range of data to analyze

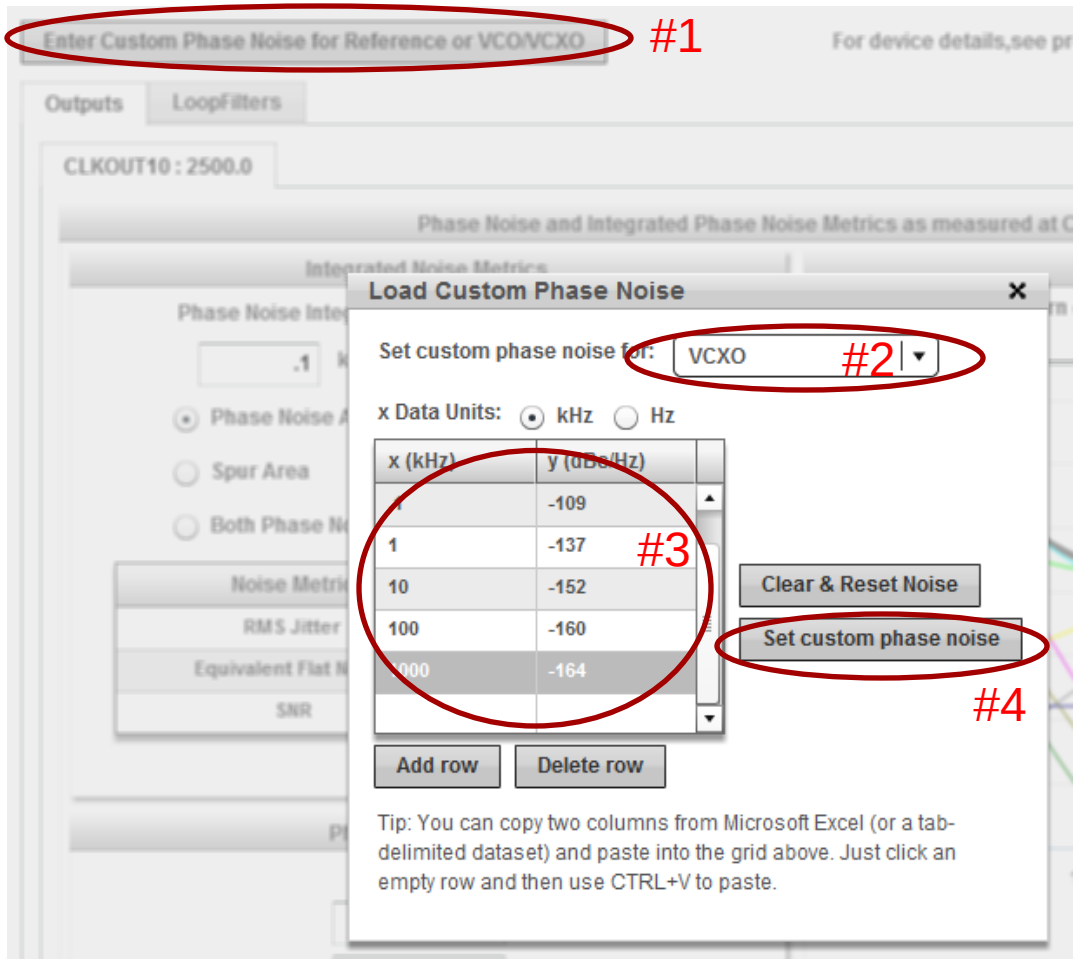
- #1) Changing simulation input to 0.1 kHz to increase amount of data to analyze
  - Setting 100 Hz
- #2) Update integration range to 100 Hz
- Note that VCXO noise dominates below 10 kHz and is impacting our jitter result.



Note 12 kHz to 20 MHz integration = 188.4 fs rms

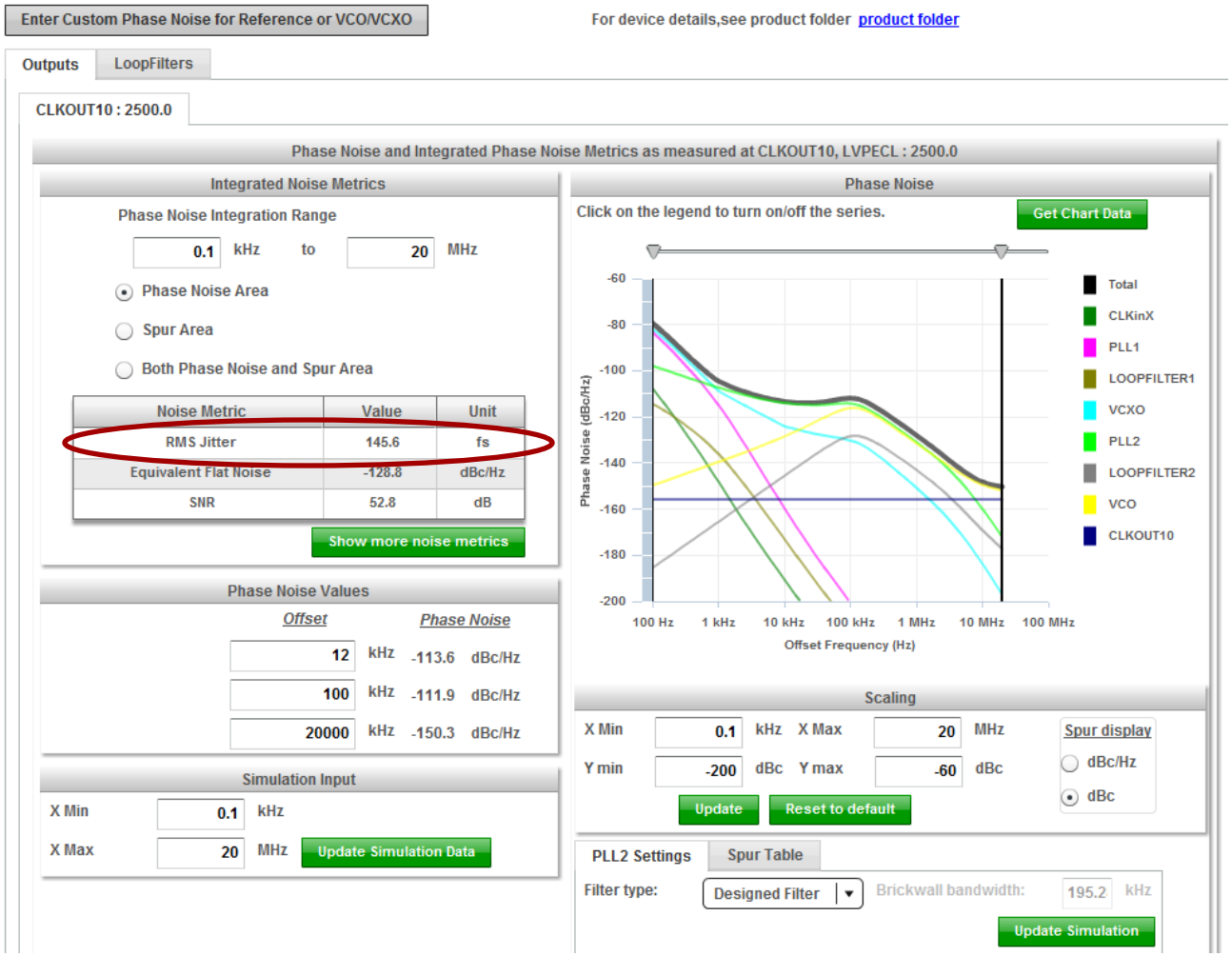
Update VCXO performance

- #1) Click the “Enter Custom Phase Noise for Reference of VCO/VCXO”
- #2) Select “VCXO”
- #3) Enter tabulated data
  - Note that it is possible to past measured data into this window. Be sure the x Data units above are as required.
- #4) Set custom phase noise.
- Now you are returned to an updated simulation.



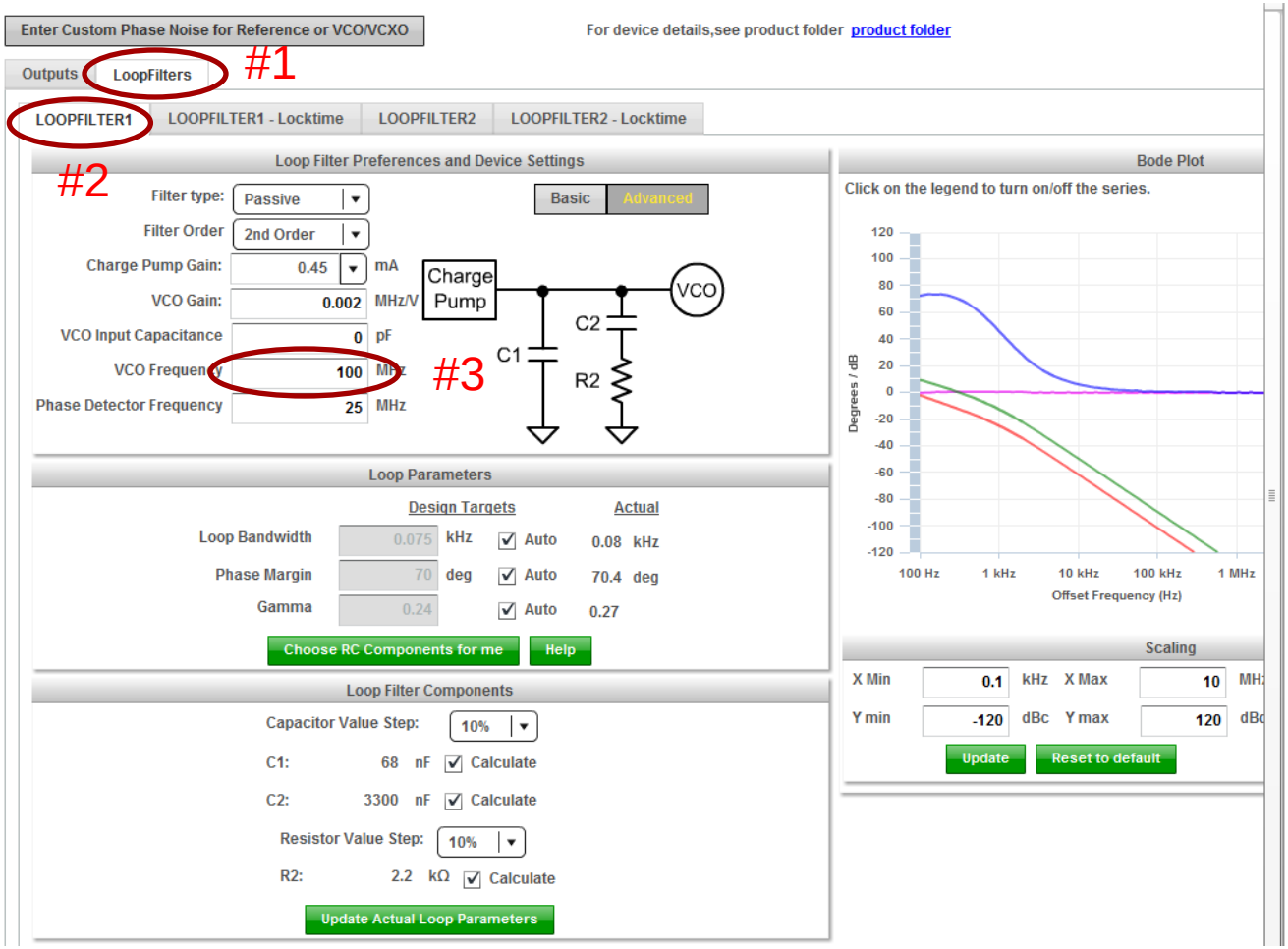
Sim result with new phase noise

- Updated jitter result is 145.6 fs rms.
- It is noted that the VCXO noise profile is much lower below 10 kHz. However still most significant contributor at 100 Hz.
- However, **must confirm VCXO frequency used by Clock Architect and PLL2 phase detector frequency.**



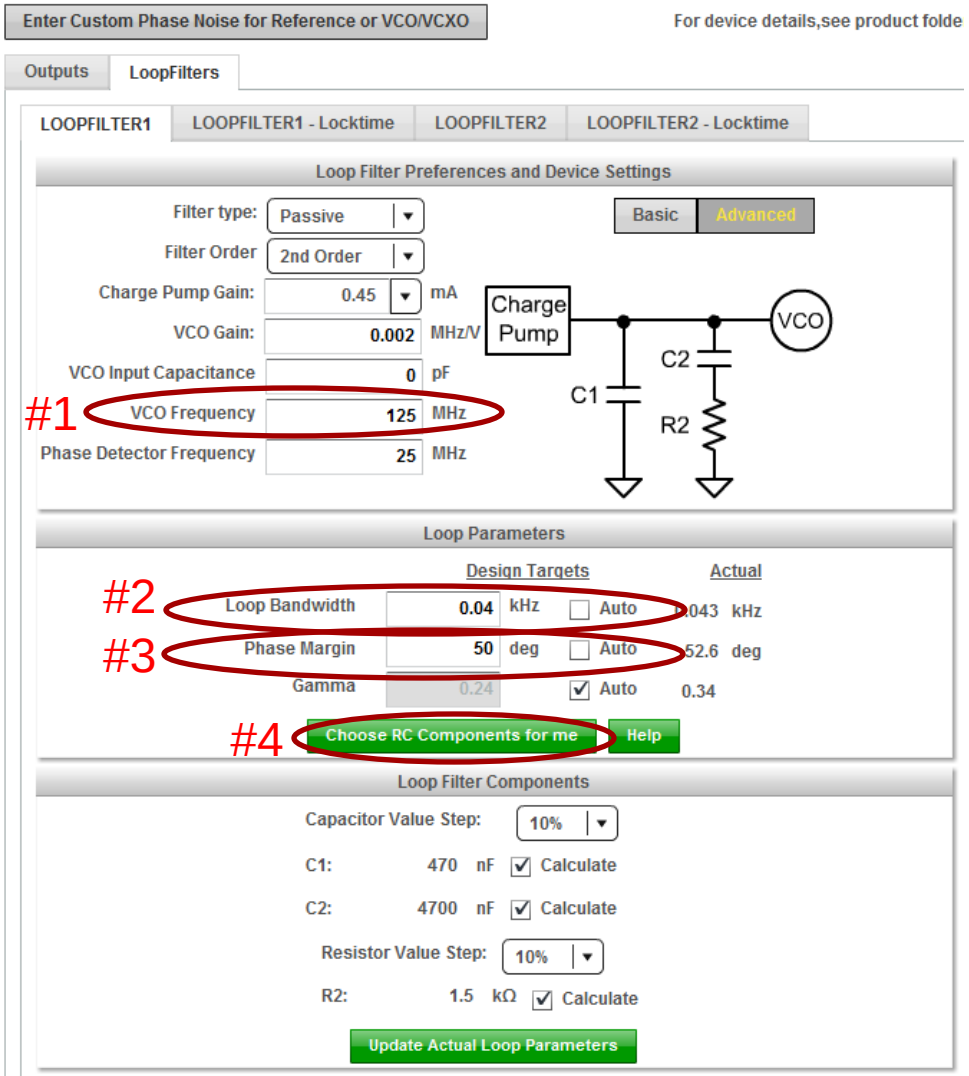
Default PLL1 Loop Filter

- Current state is 100 MHz VCXO. The VCXO we are considering is 125 MHz.
- For proper loop filter, VCO Gain must be entered for your specific VCXO, we will assume 2 kHz/V is correct.
- Note the phase detector is 25 MHz, this may be reduced to help reduce capacitor sizes by increasing PLL1 N.
- Charge Pump gain may also be altered to impact loop performance. After making change, clock 'Choose RC Components for me'



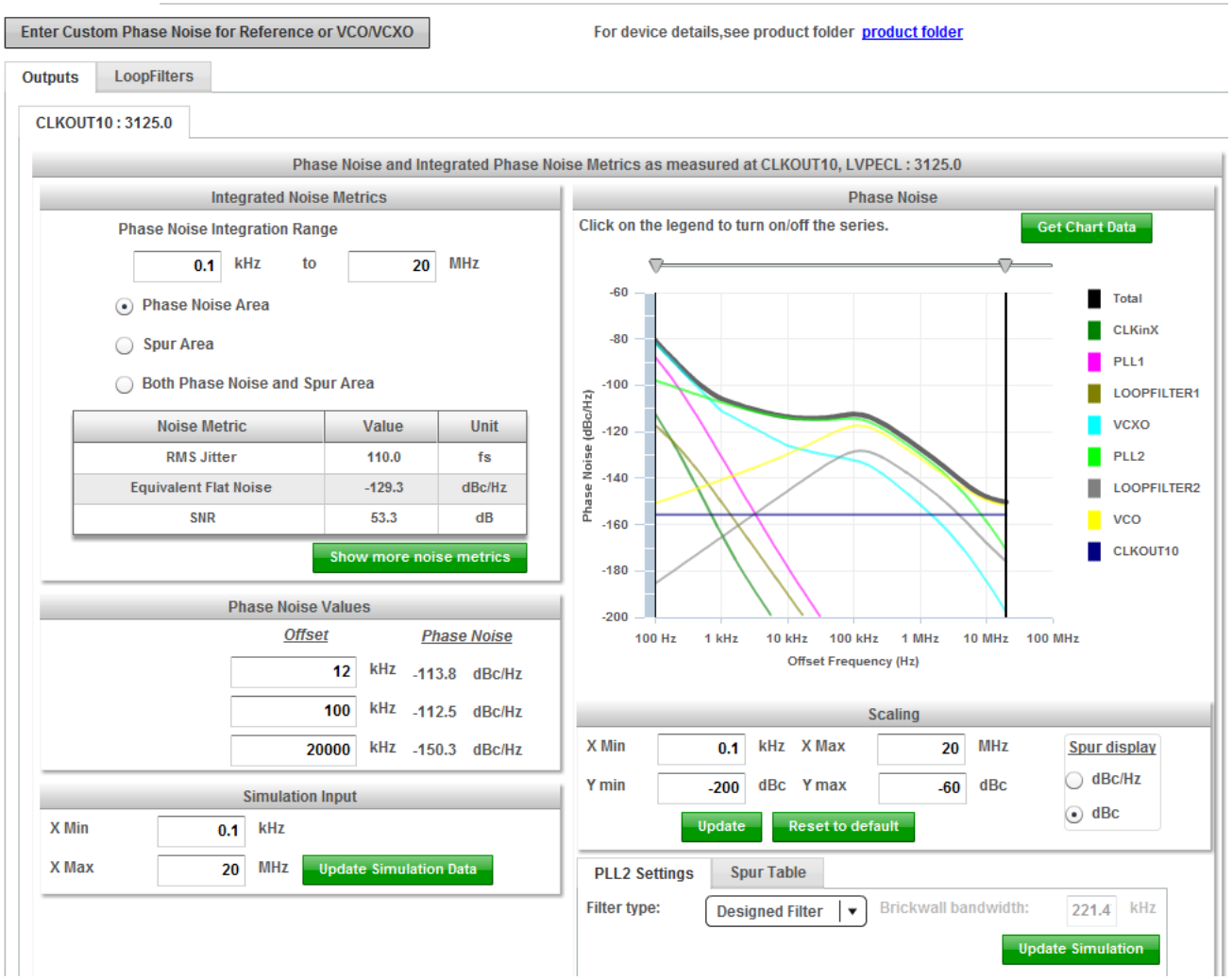
Update PLL1 Loop Filter / VCXO Frequency

- #1) Updated VCO Frequency to 125 MHz.
- Changed Loop Bandwidth to
  - #2) Force Loop Bandwidth of 40 Hz (default 75 Hz)
    - Lower loop bandwidth provides more filtering of CLKin (PLL1 reference) and PLL1 noise.
  - #3) Force Phase Margin of 50° (default 70 °)
    - Lower phase margin causes the filter to peak more at loop bandwidth, but 'cut' better. Some peaking at loop bandwidth for loop filters with bandwidth less than lower integration typically doesn't negatively impact jitter. Keep phase margin > 45 degrees.
- #4) Update the Loop Filter



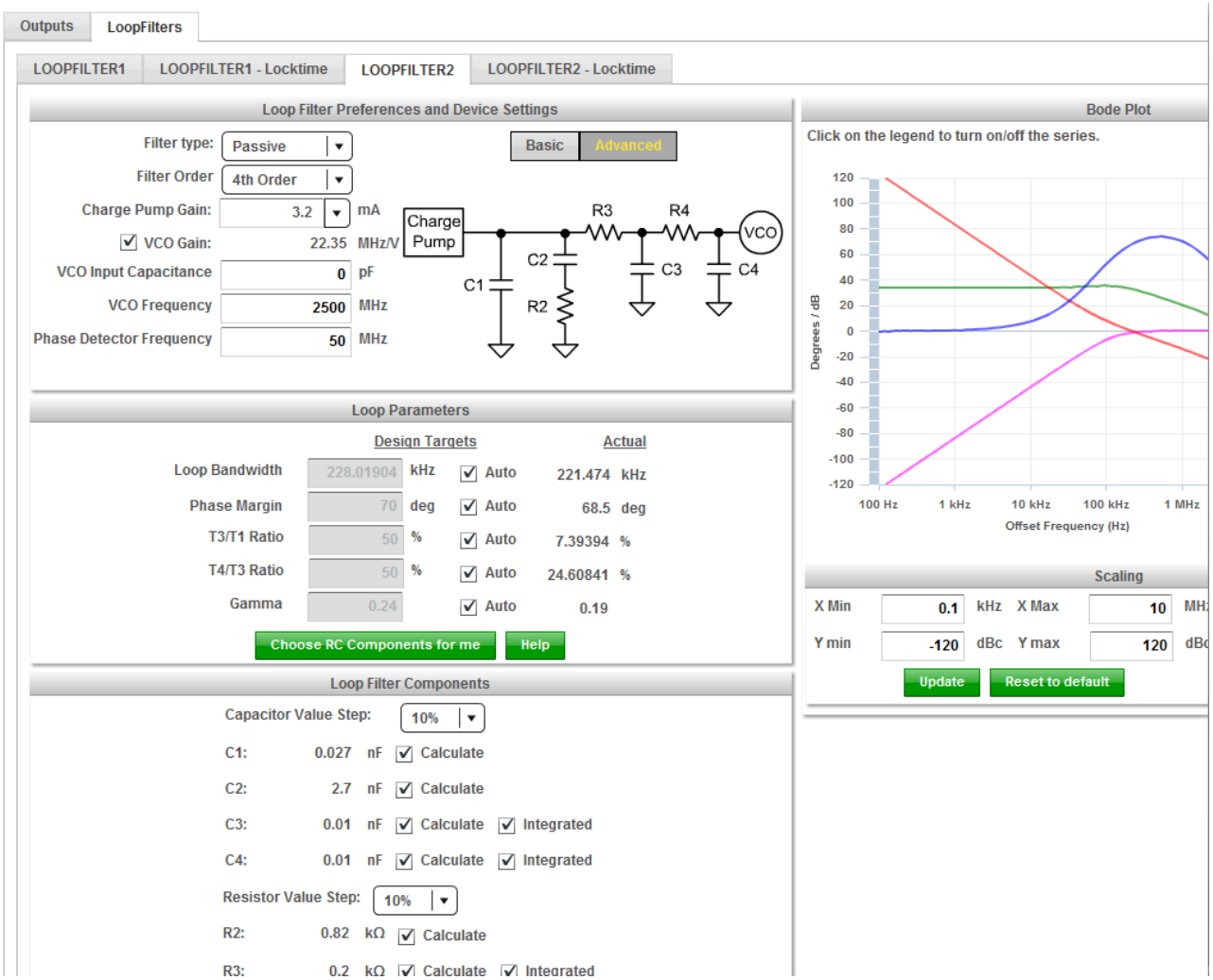
Results of updating PLL1 Loop Filter

- Note that because we narrowed the loop bandwidth of PLL1, the gap between PLL1 noise and VCXO noise at 100 Hz is larger, this is because the VCXO is filtering the PLL + Reference noise more at 100 Hz.
  - This shows a VCO (VCXO) dominant type loop filter for PLL1.
- Because we changed our VCXO frequency, the clock output frequency has also increased to 3125 MHz, we must update PLL2 loop filter.



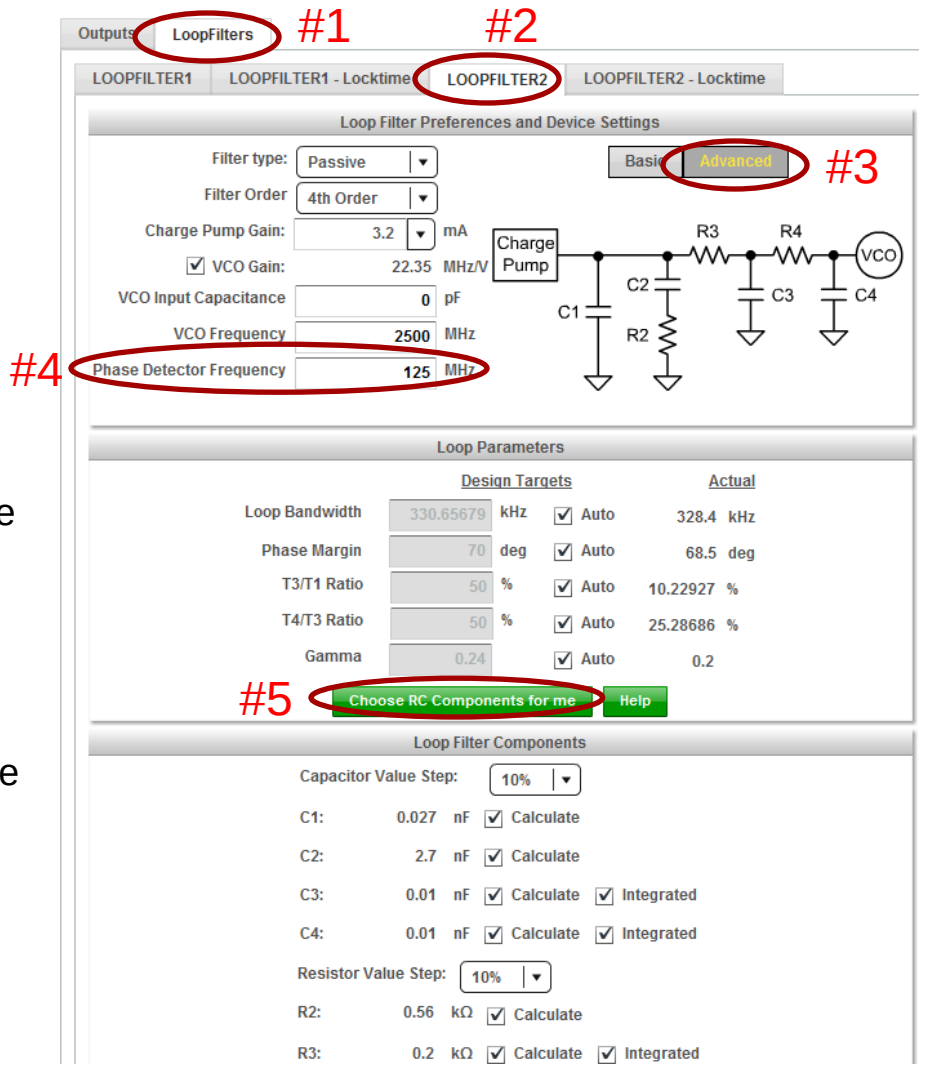
Default PLL2 Loop Filter for this design

- Note from initial simulation, the phase detector was set to 50 MHz, this is sub-optimal and was reducing our jitter performance, the maximum possible phase detector frequency should normally be used for PLL2 when presented with a clean reference.
  - LMK0482x can accept up to 155 MHz PDF.



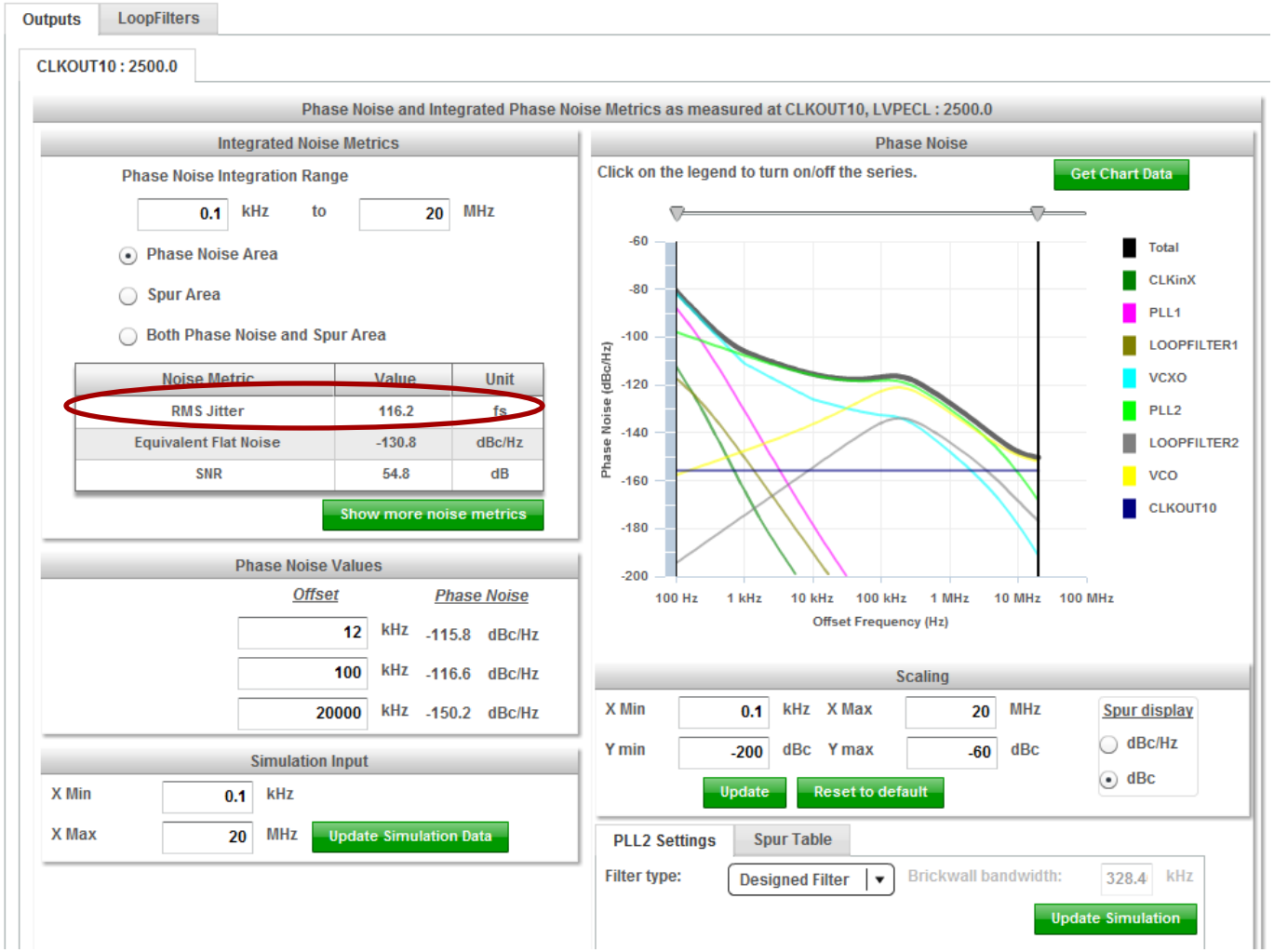
Updating PLL2 Loop Filter

- #1) Select Loop Filters tab
- #2) Select LOOPFILTER2
- #3) Select Advanced Mode
- #4) Update the phase detector frequency to be the same as VCXO frequency for PLL R = 1.
  - Note if your VCXO is less than 77.5 MHz, you could enter twice the VCXO frequency to simulate the effect of the PLL2 Reference Doubler, for example 61.44 MHz VCXO could have a PDF = 122.88 MHz.
- #5) Calculate updated loop filter.
  - We stick with the auto here, because this tends to design the optimum loop filter. One possibility for tweaking is trying higher phase margins like 75, 80, or 85 degrees.



Final simulation results using LMK04828 VCO0.

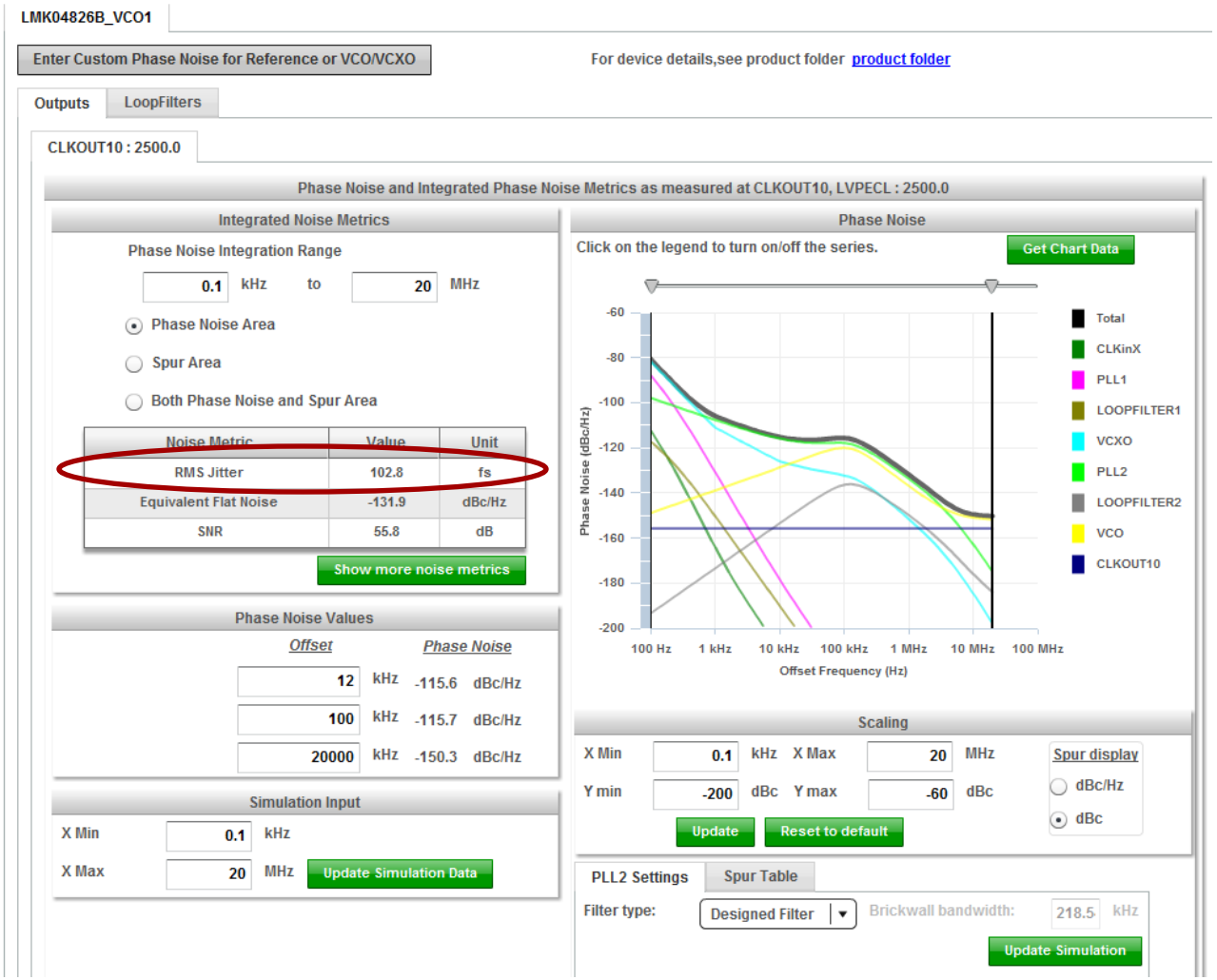
- Here is a link to the shared project.



Note 12 kHz to 20 MHz integration = 116.2 fs rms

Final simulation results using LMK04826 VCO1.

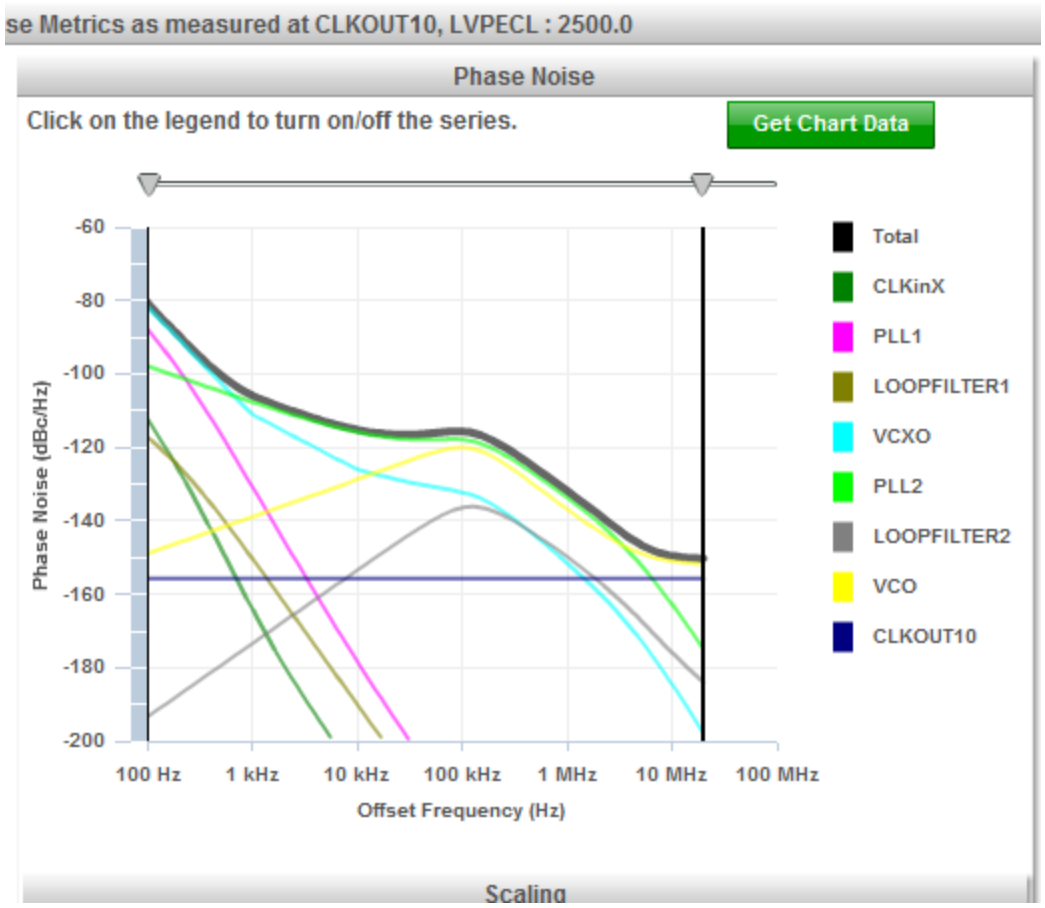
- In the LMK0482x family, the VCO1 has better open loop performance. Accordingly I've re-created the previous project, but with LMK04826. To return an LMK04826 result, in the search I set a filter for LMK04826.
- With LMK04826 VCO1 at 2500 MHz, **the simulated integrated jitter is 102.8 fs rms.**
- Please find this link to this shared project.



Note 12 kHz to 20 MHz integration = **102.8 fs rms**

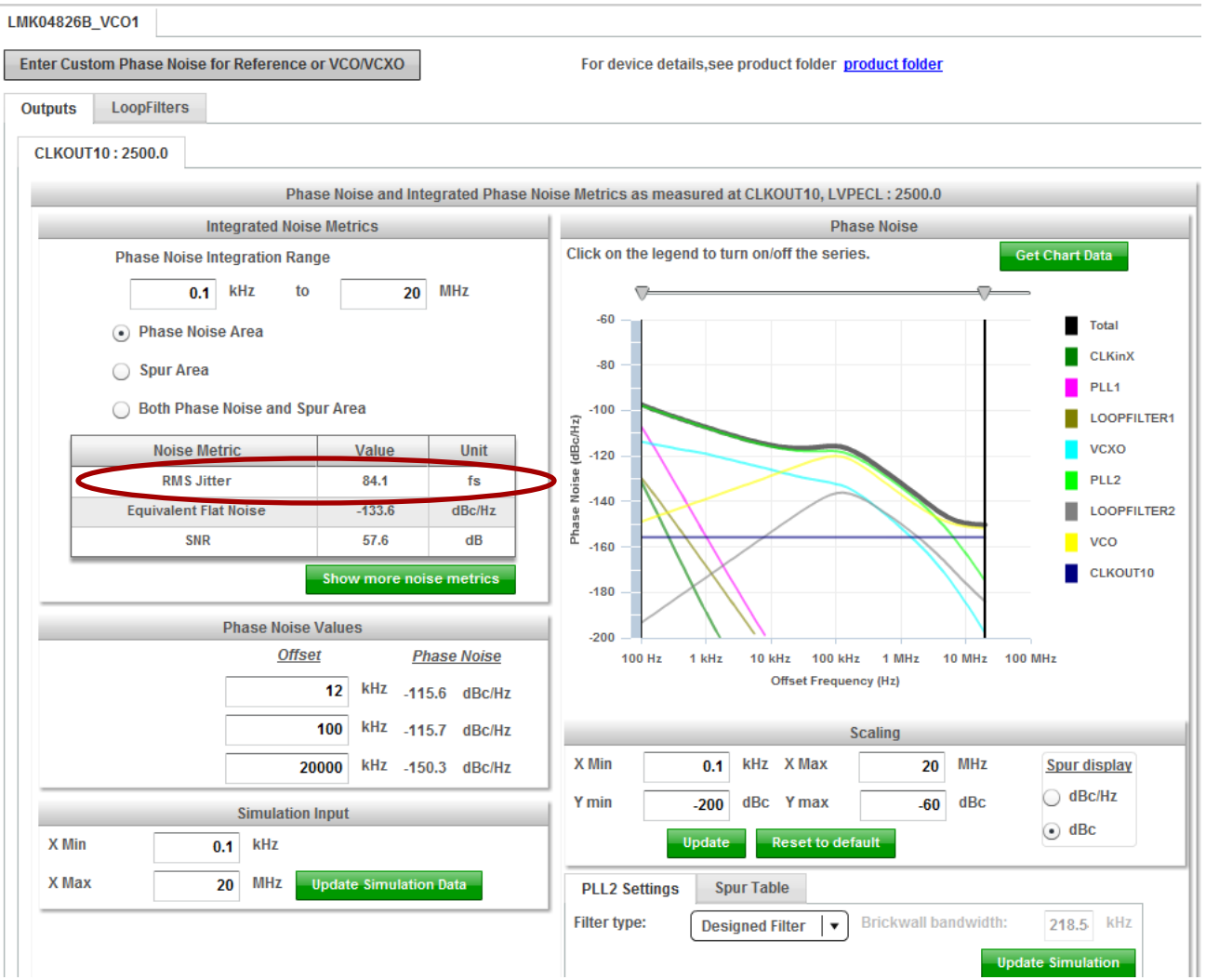
Final note

- The VCXO in this design is still limiting performance, as illustrated by the cyan line. VCXO is impacting below 1 kHz.
- Also PLL1 would be limiting performance below 1 kHz. Increase charge pump current to improve PLL1 noise or decreasing PLL1 loop bandwidth (more effective) will filter this noise out.
  - Updating from 40 Hz to 10 Hz loop bandwidth places PLL1 noise about 10 dB below PLL2 noise.



LMK0482x phase noise show case

- With a VCXO that doesn't limit phase noise performance and a loop filter designed such that PLL1 noise does not impact final output, jitter performance is improved in the 100 Hz to 20 MHz integration range. By simulation best case performance is:
  - **84.1 fs rms**



Other Notes

- LMK0482x simulations do not include support for the SYSREF divider. So entering low SYSREF frequencies into the design will cause the LMK0482x to not show as a solution.

A Note About Single Loop Simulations

2017-03-21

Simulating for a Single Loop

- **A Dual Loop simulation can be valid for a single loop. <u>The VCXO becomes your reference.</u>**
- In the example above, set the VCXO for the frequency of your single loop reference.
- Set your reference noise as VCXO noise
- Design the PLL1 loop bandwidth to be narrow, say 0.001 kHz with 50 degrees phase margin. Now the VCXO will be dominant most likely at offsets of 10 Hz and above (if not lower).
- If necessary, CLKin noise is somehow impacting your plot… override CLKin noise with a very low value like:
  - 1 kHz = -200 dBc/Hz
  - 10 kHz = -200 dBc/Hz