

Texas Instruments Qualification Summary

Quality and reliability are built into TI's culture, with the goal of providing customers high quality products. TI's semiconductor technologies are developed with a minimum goal of fewer than 50 Failures in Time (FIT) at 100,000 Power-On-Hours at 105C junction temperature. TI builds simulations, accelerated testing, and robustness evaluations into the product development process. During the product development process, TI carefully assesses silicon process reliability, package reliability, and silicon/package interaction.

TI also evaluates manufacturability of the device to verify a robust silicon and assembly flow to enable continuity of supply to customers. Non-Automotive devices are qualified with industry standard test methodologies performed primarily to the intent of the Joint Electron Devices Engineering Council (JEDEC). TI qualifies new devices, significant changes, and product families based on JEDEC JESD47. The data shown is representative of the material sets, processes, and manufacturing sites used by the device family.

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Qualification summary for:	CDC6C025000ADLFRQ1
Report date:	04/02/2026

Type	AEC Q100 test #	Test spec	Min lot qty	SS / lot	Test name	Condition	Result	Notes
Test group A - accelerated environment stress test								
THB/HAST	A2	JESD22-A101/J ESD22-A110	3	77	Biased HAST	130C/85%RH 96 hours	Pass	Or equivalent Q1 00 condition
AC/UHAST	A3	JESD22-A102/J ESD22-A118	3	77	Unbiased HAST	130C/85%RH fo r 96 hours	Pass	Or equivalent Q1 00 condition
TC	A4	JESD22-A104	3	77	Temperature cy cle	Per grade requir ements. See dat a sheet.	Pass	
TC-WBP	A4	MIL-STD883 me thod 2011	1	30	Post temp cycle bond pull	Per requirement s	Pass	As applicable pe r die configuratio n
HTSL	A6	JESD22-A103	1	45	High temp storag e bake	Per grade requir ements. See dat a sheet.	Pass	

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Type	AEC Q100 test #	Test spec	Min lot qty	SS / lot	Test name	Condition	Result	Notes
Test group B - accelerated lifetime simulation test								
HTOL	B1	JESD22-A108	3	77	High temperature operating life	Per grade requirements. See data sheet.	Pass	
ELFR	B2	AEC Q100-008	3	800	Early life failure rate	Per grade requirements. See data sheet.	Pass	
Test group C - package assembly integrity tests								
WBS	C1	AEC Q100-001	1	30	Wire bond shear	Cpk > 1.67	Pass	As applicable per die configuration
WBP	C2	MIL-STD883 method 2011	1	30	Wire bond pull	Cpk > 1.67	Pass	As applicable per die configuration
SD	C3	JEDEC J-STD-020	1	15	Solderability	>95% lead coverage	Pass	
PD	C4	JESD22-B100 and B108	3	10	Physical dimensions	Cpk > 1.67	Pass	
SBS	C5	AEC Q100-010	3	5 balls from 10 devices	Solder Ball Shear	Cpk > 1.67	Pass	As applicable per die configuration

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Test group D - die fabrication reliability tests								
EM	D1	—	—	—	Electromigration	Per technology requirements	Pass	
Tddb	D2	—	—	—	Time dependent dielectric breakdown	Per technology requirements	Pass	
HCI	D3	—	—	—	Hot carrier injection	Per technology requirements	Pass	
BTI	D4	—	—	—	Bias temperature instability	Per technology requirements	Pass	
SM	D5	—	—	—	Stress Migration	Per technology requirements	Pass	
Test group E - electrical verification								
HBM	E2	AEC Q100-002	1	3	Electrostatic discharge - human body model	Per AEC Q100-002	See data sheet	
CDM	E3	AEC Q100-011	1	3	Electrostatic discharge - charged device model	Per AEC Q100-011	See data sheet	
LU	E4	AEC Q100-004	1	3	Latch-up	Per AEC Q100-004	Pass	As applicable per Q100-004

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ED	E5	AEC Q100-009	3	30	Electrical distributions	Per AEC Q100-009	Pass	

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