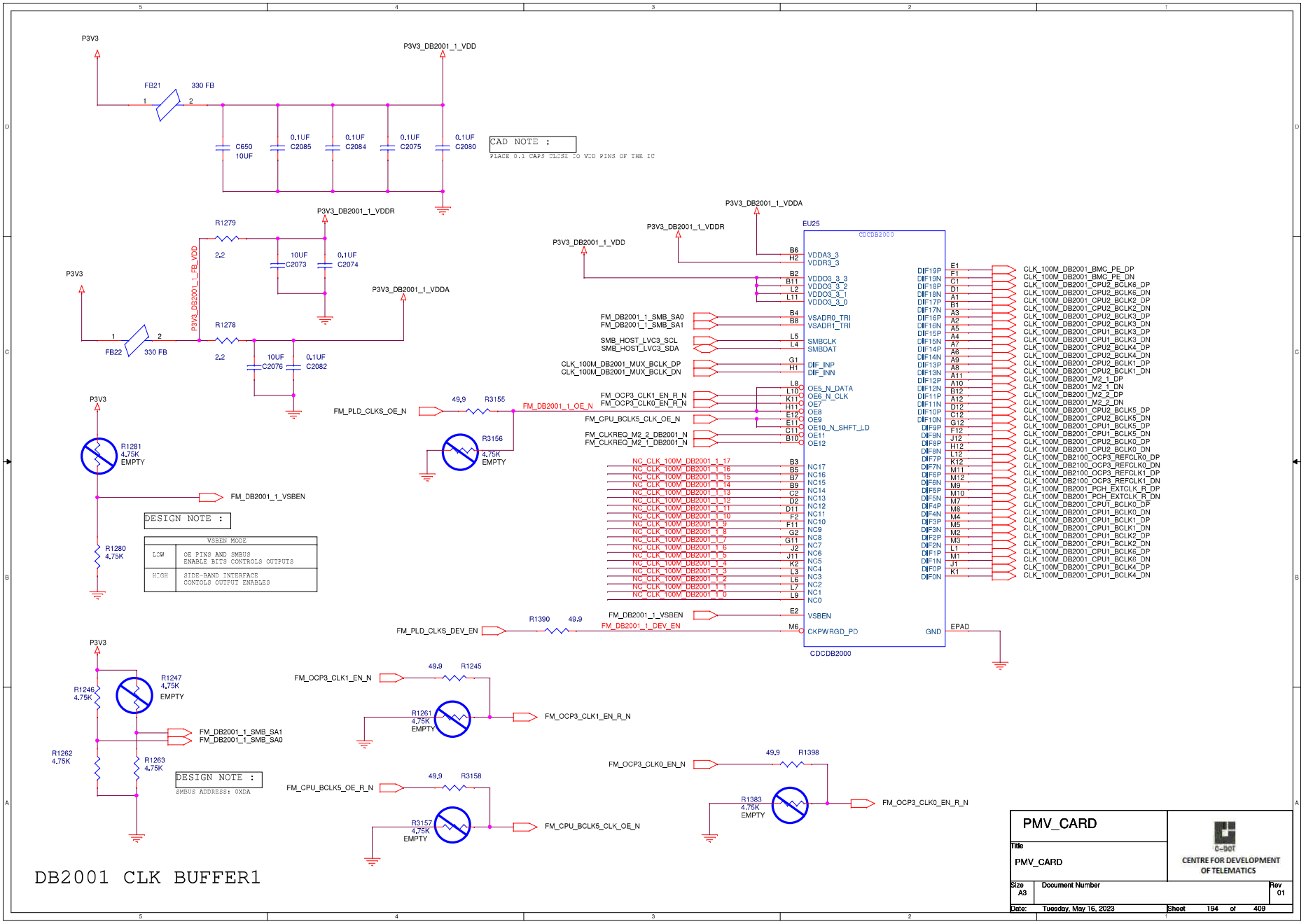
P3V3
P3V3_DB2001_1_VDD
FB21
330 FB
C650
10UF
0.1UF
C2085
0.1UF
C2084
0.1UF
C2075
0.1UF
C2080
CAD NOTE :
PLACE 0.1 CAPS CLOSE TO VDD PINS OF THE IC
P3V3_DB2001_1_VDDR
R1279
2.2
10UF
C2073
0.1UF
C2074
P3V3_DB2001_1_FB_VDD
P3V3
FB22
330 FB
R1278
2.2
10UF
C2076
0.1UF
C2082
P3V3_DB2001_1_VDDA
P3V3_DB2001_1_VDDA
P3V3_DB2001_1_VDDR
P3V3_DB2001_1_VDD
EU25
CDCDB2000
VDDA3_3
VDDR3_3
VDDO3_3_3
VDDO3_3_2
VDDO3_3_1
VDDO3_3_0
FM_DB2001_1_SMB_SA0
FM_DB2001_1_SMB_SA1
VSADR0_TRI
VSADR1_TRI
SMB_HOST_LVC3_SCL
SMB_HOST_LVC3_SDA
SMBCLK
SMBDAT
CLK_100M_DB2001_MUX_BCLK_DP
CLK_100M_DB2001_MUX_BCLK_DN
DIF_INP
DIF_INN
FM_OCP3_CLK1_EN_R_N
FM_OCP3_CLK0_EN_R_N
OE5_N_DATA
OE6_N_CLK
OE7
OE8
FM_CPU_BCLK5_CLK_OE_N
OE9
OE10_N_SHFT_LD
FM_CLKREQ_M2_2_DB2001_N
FM_CLKREQ_M2_1_DB2001_N
OE11
OE12
NC_CLK_100M_DB2001_1_17
NC_CLK_100M_DB2001_1_16
NC_CLK_100M_DB2001_1_15
NC_CLK_100M_DB2001_1_14
NC_CLK_100M_DB2001_1_13
NC_CLK_100M_DB2001_1_12
NC_CLK_100M_DB2001_1_11
NC_CLK_100M_DB2001_1_10
NC_CLK_100M_DB2001_1_9
NC_CLK_100M_DB2001_1_8
NC_CLK_100M_DB2001_1_7
NC_CLK_100M_DB2001_1_6
NC_CLK_100M_DB2001_1_5
NC_CLK_100M_DB2001_1_4
NC_CLK_100M_DB2001_1_3
NC_CLK_100M_DB2001_1_2
NC_CLK_100M_DB2001_1_1
NC_CLK_100M_DB2001_1_0
NC17
NC16
NC15
NC14
NC13
NC12
NC11
NC10
NC9
NC8
NC7
NC6
NC5
NC4
NC3
NC2
NC1
NC0
FM_DB2001_1_VSBEN
VSBEN
FM_PLD_CLKS_DEV_EN
FM_DB2001_1_DEV_EN
CKPWRGD_PD
GND
EPAD
DIF19P
DIF19N
DIF18P
DIF18N
DIF17P
DIF17N
DIF16P
DIF16N
DIF15P
DIF15N
DIF14P
DIF14N
DIF13P
DIF13N
DIF12P
DIF12N
DIF11P
DIF11N
DIF10P
DIF10N
DIF9P
DIF9N
DIF8P
DIF8N
DIF7P
DIF7N
DIF6P
DIF6N
DIF5P
DIF5N
DIF4P
DIF4N
DIF3P
DIF3N
DIF2P
DIF2N
DIF1P
DIF1N
DIF0P
DIF0N
CLK_100M_DB2001_BMC_PE_DP
CLK_100M_DB2001_BMC_PE_DN
CLK_100M_DB2001_CPU2_BCLK6_DP
CLK_100M_DB2001_CPU2_BCLK6_DN
CLK_100M_DB2001_CPU2_BCLK2_DP
CLK_100M_DB2001_CPU2_BCLK2_DN
CLK_100M_DB2001_CPU2_BCLK3_DP
CLK_100M_DB2001_CPU2_BCLK3_DN
CLK_100M_DB2001_CPU1_BCLK3_DP
CLK_100M_DB2001_CPU1_BCLK3_DN
CLK_100M_DB2001_CPU2_BCLK4_DP
CLK_100M_DB2001_CPU2_BCLK4_DN
CLK_100M_DB2001_CPU2_BCLK1_DP
CLK_100M_DB2001_CPU2_BCLK1_DN
CLK_100M_DB2001_M2_1_DP
CLK_100M_DB2001_M2_1_DN
CLK_100M_DB2001_M2_2_DP
CLK_100M_DB2001_M2_2_DN
CLK_100M_DB2001_CPU2_BCLK5_DP
CLK_100M_DB2001_CPU2_BCLK5_DN
CLK_100M_DB2001_CPU1_BCLK5_DP
CLK_100M_DB2001_CPU1_BCLK5_DN
CLK_100M_DB2001_CPU2_BCLK0_DP
CLK_100M_DB2001_CPU2_BCLK0_DN
CLK_100M_DB2100_OCP3_REFCLK0_DP
CLK_100M_DB2100_OCP3_REFCLK0_DN
CLK_100M_DB2100_OCP3_REFCLK1_DP
CLK_100M_DB2100_OCP3_REFCLK1_DN
CLK_100M_DB2001_PCH_EXTCLK_R_DP
CLK_100M_DB2001_PCH_EXTCLK_R_DN
CLK_100M_DB2001_CPU1_BCLK0_DP
CLK_100M_DB2001_CPU1_BCLK0_DN
CLK_100M_DB2001_CPU1_BCLK1_DP
CLK_100M_DB2001_CPU1_BCLK1_DN
CLK_100M_DB2001_CPU1_BCLK2_DP
CLK_100M_DB2001_CPU1_BCLK2_DN
CLK_100M_DB2001_CPU1_BCLK6_DP
CLK_100M_DB2001_CPU1_BCLK6_DN
CLK_100M_DB2001_CPU1_BCLK4_DP
CLK_100M_DB2001_CPU1_BCLK4_DN
CDCDB2000
P3V3
R1281
4.75K
EMPTY
FM_DB2001_1_VSBEN
R1280
4.75K
DESIGN NOTE :
VSBEN MODE
LOW
OE PINS AND SMBUS ENABLE BITS CONTROLS OUTPUTS
HIGH
SIDE-BAND INTERFACE CONTOLS OUTPUT ENABLES
FM_PLD_CLKS_OE_N
49.9
R3155
FM_DB2001_1_OE_N
R3156
4.75K
EMPTY
R1390
49.9
P3V3
R1246
4.75K
R1247
4.75K
EMPTY
FM_DB2001_1_SMB_SA1
FM_DB2001_1_SMB_SA0
R1262
4.75K
R1263
4.75K
DESIGN NOTE :
SMBUS ADDRESS: 0XDA
FM_OCP3_CLK1_EN_N
49.9
R1245
R1261
4.75K
EMPTY
FM_OCP3_CLK1_EN_R_N
FM_CPU_BCLK5_OE_R_N
49.9
R3158
R3157
4.75K
EMPTY
FM_CPU_BCLK5_CLK_OE_N
FM_OCP3_CLK0_EN_N
49.9
R1398
R1383
4.75K
EMPTY
FM_OCP3_CLK0_EN_R_N
DB2001 CLK BUFFER1
PMV_CARD
Title
PMV_CARD
C-DOT
CENTRE FOR DEVELOPMENT OF TELEMATICS
Size
A3
Document Number
Rev
01
Date:
Tuesday, May 16, 2023
Sheet
194
of
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