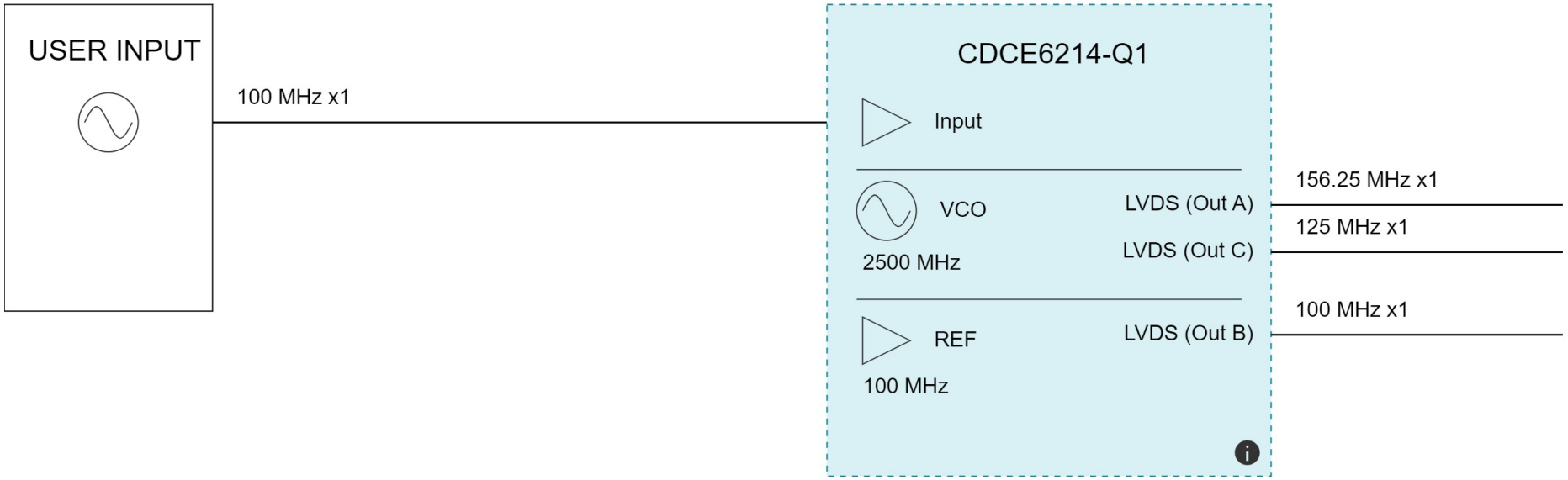
Clock tree architect design report

1. Selected solution details:

1.a. Block diagram:



https://webench.ti.com/clock-tree-architect

1.b. Solution details:

Devices	Area (mm²)	BOM price estimate ($)	Jitter (fs rms)	Power (mW)
CDCE6214-Q1	16.00	3.080	350 Out A: 350 Out C: 350 Out B: 179	172

1.c. Device details:

Devices	Area (mm²)	BOM price estimate ($)	Current (mA)	Power (mW)
CDCE6214-Q1	16.00	3.080	52	172

1.d. Output details:

Devices	Output	Frequency	Format	Clock count	Jitter (fs rms)	Noise floor (dBc/Hz)	Deterministic phase
CDCE6214-Q1	Out A: GTH Clock-SFP	156.25 MHz	LVDS	1	350	-152	Yes [1]
	Out C: PCIE_125	125 MHz	LVDS	1	350	-152	Yes [1]
	Out B: PCIE_100	100 MHz	LVDS	1	179	-152	Yes [1]

[1] Requires some settings at device level. Kindly, refer the datasheet.

2. Required system specifications and parameters:

2.a. Required output details:

Name	Format	Frequency	Clock count	Jitter (fs rms)	Noise floor (dBc/Hz)	Additional specs
Out A: GTH Clock-SFP	LVDS	156.25 MHz	1	1000	-50	-
Out B: PCIE_100	LVDS	100 MHz	1	1000	-50	-
Out C: PCIE_125	LVDS	125 MHz	1	1000	-50	-

2.b. Input details:

One or more of the below inputs or TI oscillators may be used.

Name	Frequency	Clock count	Jitter (fs rms)	Noise floor (dBc/Hz)	Additional specs
Input- 25MHz Crystal	25 MHz	1	-	-	-
Input A- 100MHz PCIE	100 MHz	1	-	-	-

2.c. System configuration options:

Application: Medical
Jitter integration bandwidth: 12 kHz to 20 MHz
Max. number of stages: 5
Solution scoring:
Jitter: Important, Power: Important, Price: Important, Area: Important

2.d. External VCO and VCXO computation parameters:

VCO attribute	Value	VCXO attribute	Value
Price ($)	30	Price ($)	20
Area (mm²)	140	Area (mm²)	180
Current (mA)	15	Current (mA)	15
Noise floor (dBc/Hz)	-156	Noise floor (dBc/Hz)	-168
Jitter (fs rms)	50	Jitter (fs rms)	50
Min frequency (MHz)	1	Frequency (MHz)	500
Max frequency (MHz)	10000	Auto pick VCXO frequency	true

2.e. User preferred devices:

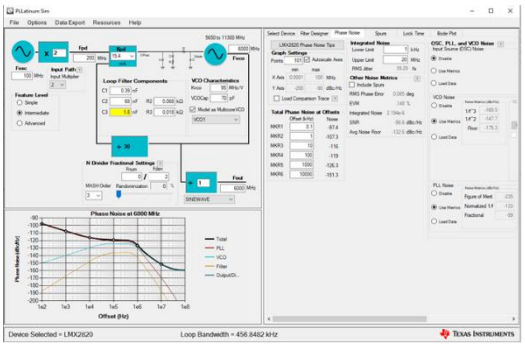
Filtration criteria: OR
Filter values: CDCE6214-Q1

Featured clocks & timing tools

Clock tree architect design tool helps you select the right clocks & timing products to design a clock tree based on user entered output, input and system specifications. Along with the clock tree structure – it provides an approximate metric for power, area, jitter and other system parameters. Users are recommended to use the below tools to help with more accurate in-depth simulations, device programming, loop filter design and configuration.

PLLatinum Simulator Tool (PLLATINUMSIM-SW)

The PLLATINUMSIM-SW simulator tool lets you create detailed designs and simulations of our PLLATINUM™ integrated circuits which include the LMX series of PLLs and synthesizers. Users can design active and passive filters, do detailed simulations of phase noise, purs, lock time and bode plots.



TICS Pro Software (TICSPRO-SW)

The TICS Pro software is used to program the evaluation modules (EVMs) for device numbers with these prefixes: CDC, LMK and LMX. These devices include PLLs and voltage-controlled oscillators (PLL+VCO), synthesizers and clocking devices. Users can program EVMs through USB2ANY interface adaptor or onboard USB interface and export the programming configurations for use in end application. Even without an EVM, TICS Pro is very useful tool in determining and validating register configurations and how to set up the device.

Clocks & timing product portfolio and additional resources

Visit Clocks & timing home page to explore the full product portfolio and additional resources to help you with your designs. Also, checkout TI Precision Labs - Clocks and timing videos to learn more about clocks and timing basics, phase lock loop fundamentals, noise, network synchronizers and design tips.

Technical support

TI E2E™ support forums

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Get answers now

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