Hi dear,

Hope you are feeling great.

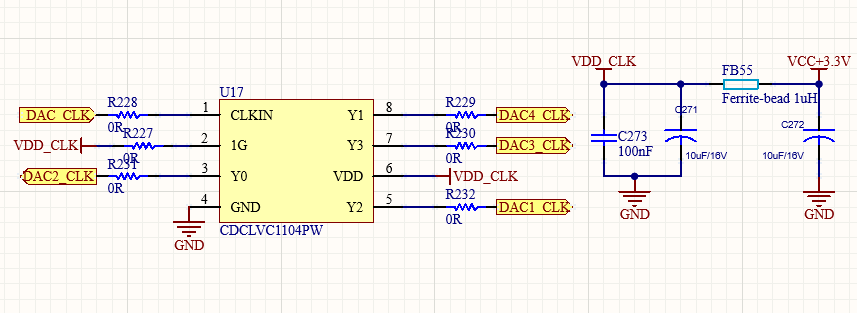
I’m sorry for missing the last case. I’m going to add the required waveform in the last response of the expired case and ask the question again.

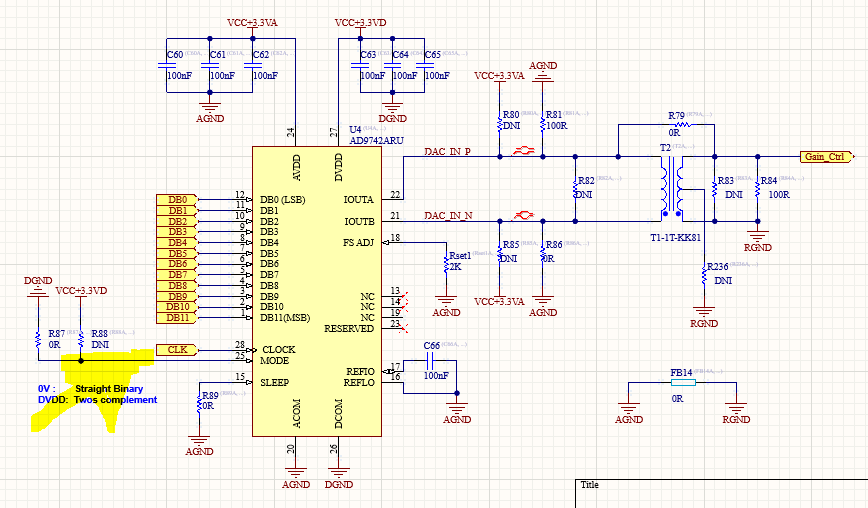
I’m using CDCLVC1104PW in order to buffer the incoming clock (100MHz-200MHz) from the FPGA (Spartan6) and apply them to four Digital-to-Analog Converters (AD9742ARU). All layout recommendations in the TI datasheet have tried to meet. However, the output values of CDCLVC1104PW are the same and around 60 mv (seems all changes of the input clock are ignored). In addition, supply voltage and high level of input CLK are 3.3V, and an input CLK meets the VHL and VLH correctly.

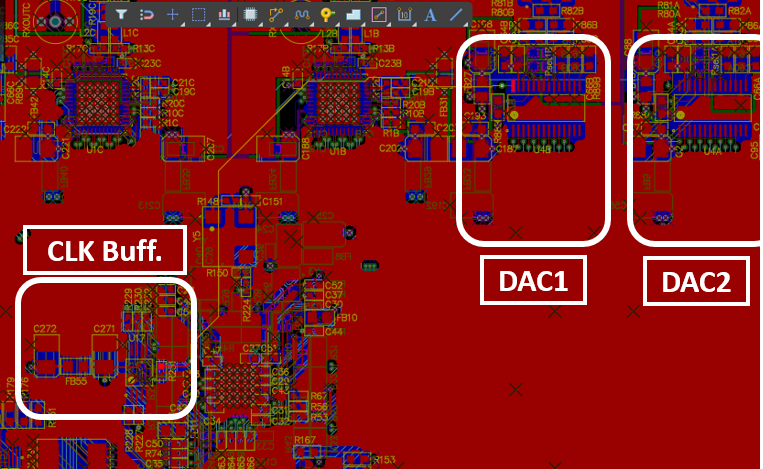
All output signals of the “clock buffer IC” have the same problem (there is no change in the output pins related to the change in the input signal). In addition, I have tried different input CLK with freq. of 10MHZ, 50MHz, 200MHz, and even I’ve applied 3.3V directly to the input pin (as well as GND) but the output pins are always equal to ‘0’.

The situation does not change even by separating of output pin from the rest of my circuit.

Please let me know if there is any problem or solution to solve the issue.

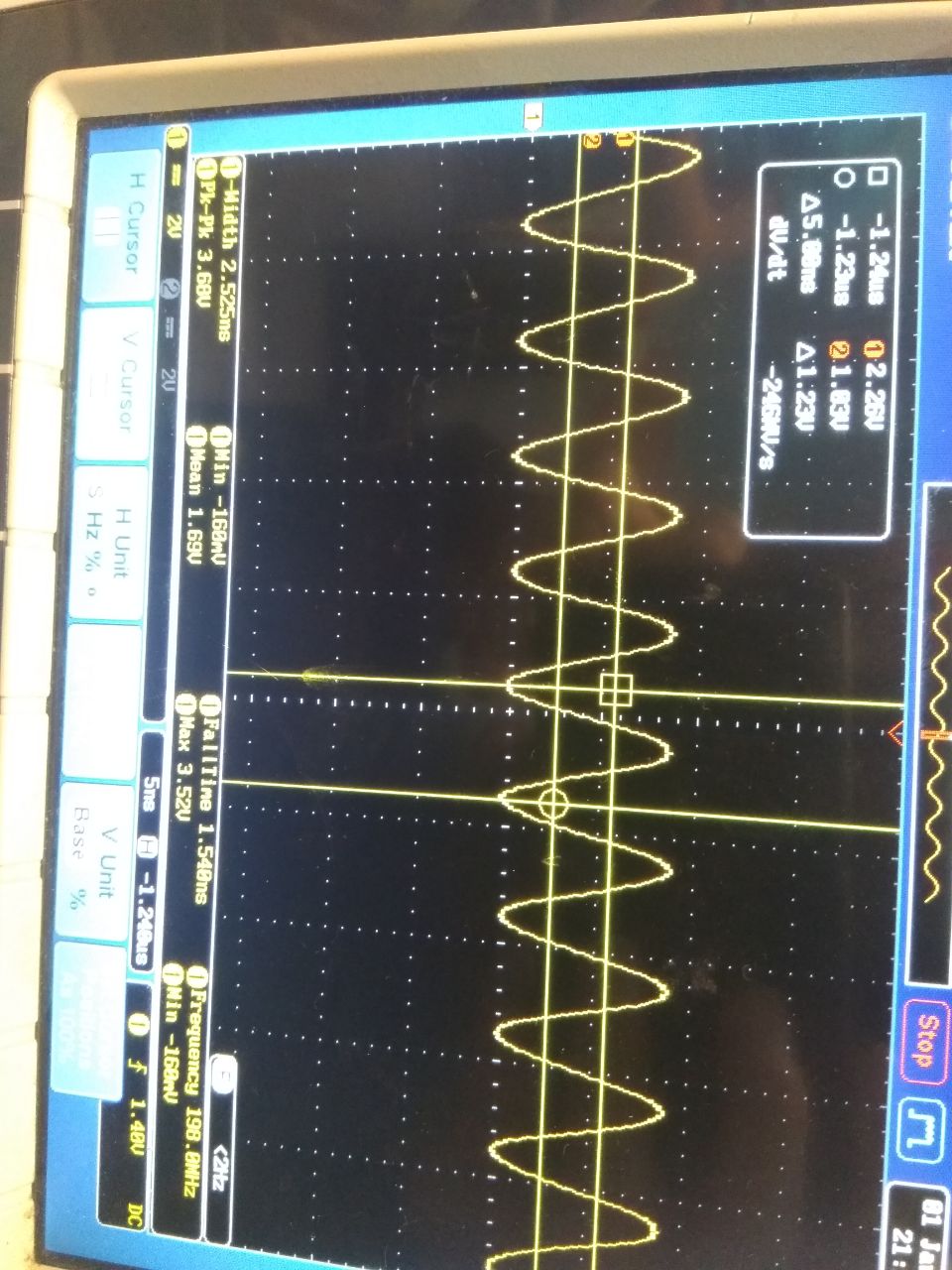
Some pictures of PCB layout, schematic, Input clock, VCC, and output are shown in the following (attached file):



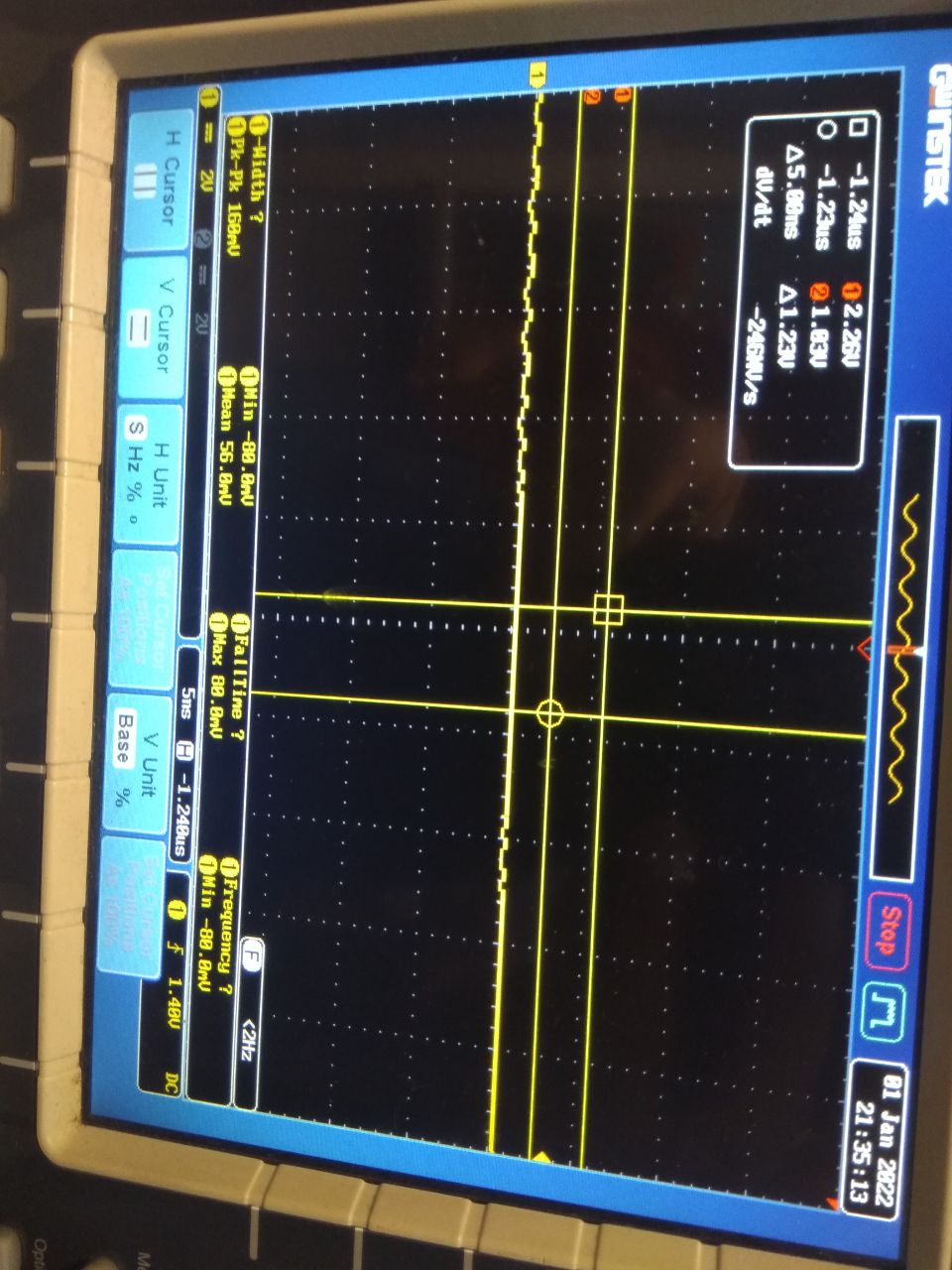




VCC



Input CLK



Output (all pins are the same)