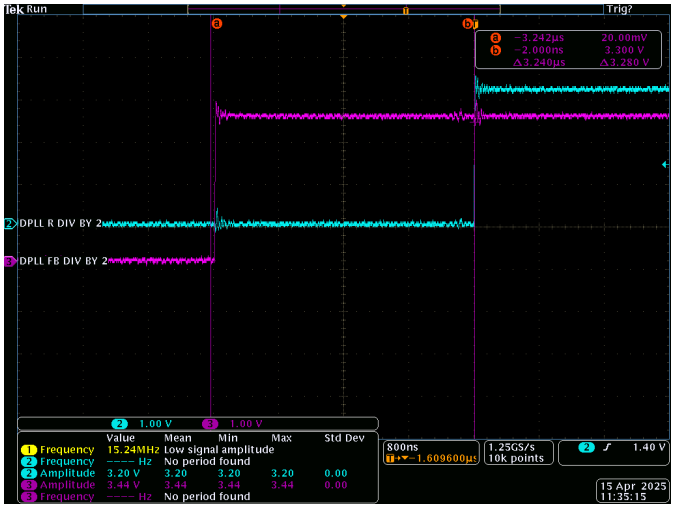
DPLL R and DPLL FB Divide By 2 Debug - DPLLs

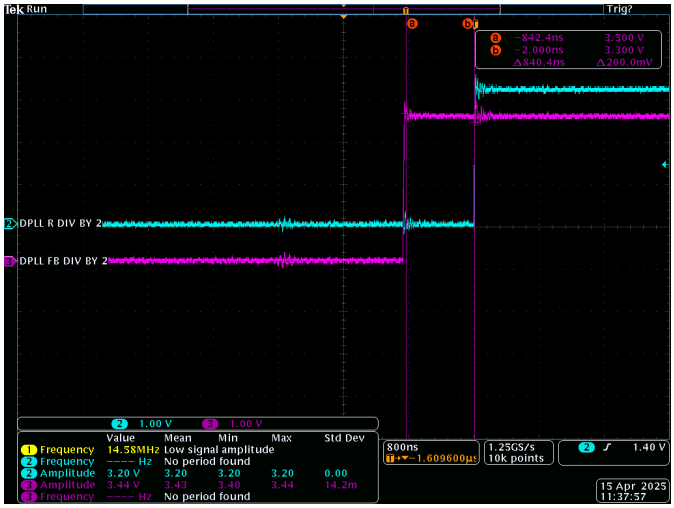
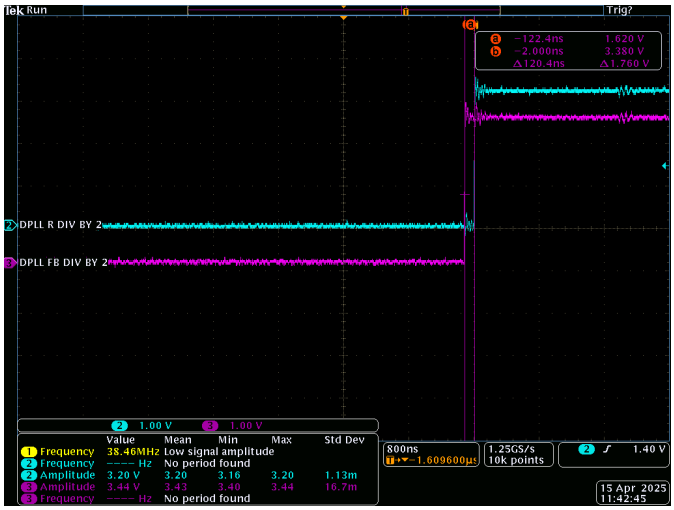
Use the DPLL R and DPLL FB Divide by 2 status signals (on STATUSx or GPIOx) to view the inputs to the TDC.

When the DPLL is locked, the two status signals are phase aligned and the scope can trigger.
If the DPLL is unlocked, the two status signals are drifting from each other and the scope cannot trigger.

Example:

- LMK05318B
- PRIREF = 1PPS
- XO = 24 MHz +/- 2.5 ppm
- DPLL LBW = 0.1 Hz

Timestamp	Error between DPLL R and DPLL FB DIV BY 2 Status	Behavior / Scope Shot
0 s	-	Toggle SWRST
10 s	-	HLDOVER = 0 LOFL = 1 LOPL = 1
25 s	-	HLDOVER = 0 LOFL = 0 LOPL = 1
45 s	3000 ns	

Timestamp	Error between DPLL R and DPLL FB DIV BY 2 Status	Behavior / Scope Shot
3 min 30 sec	840 ns	
8 min 30 s	120 ns	

Timestamp	Error between DPLL R and DPLL FB DIV BY 2 Status	Behavior / Scope Shot
10 min	56 ns	Zoom in, change in time scale DPLL FB fluctuates as the DPLL tracks the REF phase and makes corrections to the DPLL numerator. DPLL FB stays around the same phase (the difference in phase between two signal stays about the same) DPLL is near 0ppm error from REF.