

LMK05318B I2C Address:
Range: 11001xxb
As Configured (float GPIO1): 1100101b

See page 40 in LMK datasheet for status output table.
Note: STATUS0 and STATUS1 can be measured via test points. Host connection to STATUS0 and STATUS1 is quite complicated, it requires the nets to be set to 0.8V at startup, then they will operate at a 3.3V voltage level (while the GPIO in/out operates at 1.8V voltage level).

OLD MATH, DO NOT USE:
Warning: AD90364_CLK may only accept a maximum V_{p-p} of 1.3V.
 $REF_CLK_VDD_{pp} \sim 2.5V \rightarrow AD90364_CLK$
(MAX $V_{p-p} = 1.3V$)
 $V_{out} = V_{in} * (C1 + C2)$
The V_{out} = 1.2V for example
 $1.2 = 2.5 * (C1 / (C1 + C2))$

For improved signal integrity on the 40MHz RFIC clock, make the following changes:

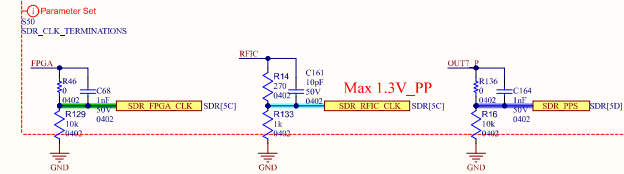
R133: Remove

R14: Replace with 5.1k Ohm

C161: Replace with ~20pF

SDR CLOCK SIGNAL TERMINATIONS

Place near SDR pins



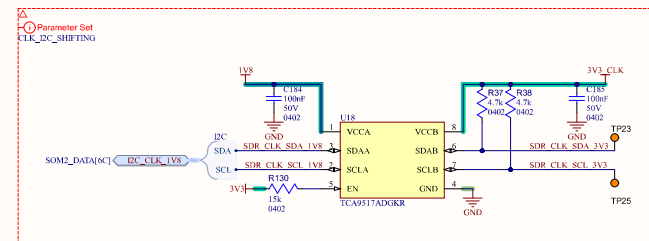
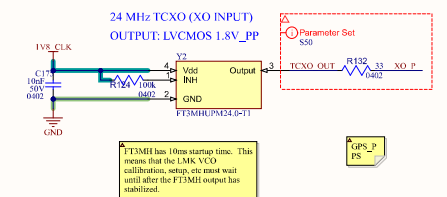
ETH PHY CLOCK SIGNAL TERMINATIONS

Place near ETH PHY



CLK_TCXO

24 MHz TCXO (XO INPUT)
OUTPUT: LVCNOS 1.8V_PP



Caution: XO_P is only 2.5V_PP compliant. Use the following values for R1 and R2 (in red):
VDD Net (found [R47])
3.3V 125/375
2.5V 1 open
1.8V 0 open
(LMK datasheet page 30)

Min recommended slew rate for all input clocks is 0.5V/ns. Especially true for single-ended clocks. Phase noise performance will begin to degrade as the clock input slew rate is reduced.

Parameter Set S50
GPS_PPS
GPS_PPS = 2.5V_PP

Parameter Set S50
PRIME_P MAX 3.4V_PP
PRIME_P = 3.4V_PP

Parameter Set S50
SECRET_P MAX 3.4V_PP
SECRET_P = 3.4V_PP

Parameter Set S50
XO_P MAX 2.5V_PP
XO_P = 2.5V_PP

Parameter Set S50
STATUS0
STATUS0 = 0.8V

Parameter Set S50
STATUS1
STATUS1 = 0.8V

Parameter Set S50
GPIO0
GPIO0 = 0.8V

Parameter Set S50
GPIO1/SCS
GPIO1/SCS = 0.8V

Parameter Set S50
GPIO2/SDO/FINC
GPIO2/SDO/FINC = 0.8V

Parameter Set S50
HW_SW_CTRL
HW_SW_CTRL = 0.8V

Parameter Set S50
SDR_CLK_SDA_3V3
SDR_CLK_SDA_3V3 = 3V3

Parameter Set S50
SDR_CLK_SCL_3V3
SDR_CLK_SCL_3V3 = 3V3

Parameter Set S50
SDR_CLK_STATUS0
SDR_CLK_STATUS0 = 0.8V

Parameter Set S50
SDR_CLK_STATUS1
SDR_CLK_STATUS1 = 0.8V

Parameter Set S50
GPIO0
GPIO0 = 0.8V

Parameter Set S50
GPIO1/SCS
GPIO1/SCS = 0.8V

Parameter Set S50
GPIO2/SDO/FINC
GPIO2/SDO/FINC = 0.8V

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HW_SW_CTRL
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SDR_CLK_SDA_3V3
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SDR_CLK_SCL_3V3
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SDR_CLK_STATUS1
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SDR_CLK_STATUS1
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GPIO1/SCS
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GPIO2/SDO/FINC
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SDR_CLK_STATUS1
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GPIO1/SCS
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