Driving the clock inputs of LMK00301 with single-ended topology

The LMK00301 has two universal inputs (CLKin0/CLKin0* and CLKin1/CLKin1*) which can accept AC or DC coupled 3.3V/2.5V LVPECL, LVDS, CML, SSTL, and other differential and single-ended signals. As long as the input signal satisfies the input requirements specified in data sheet, there is no risk in operation.

A differential signal input is better than single-ended input circuit because it typically provides higher slew rate and common-mode-rejection which help to achieve a batter phase noise and jitter performance. While it is recommended to drive the CLKin/CLKin* pair with a differential signal input, it is possible to drive it with a single-ended clock provided it conforms to the Single-Ended Input specifications for CLKin pins listed in the Electrical Characteristics.

V_{IH}	Single-Ended Input High Voltage	CLKinX driven single-ended (AC or DC coupled), CLKinX* AC coupled to GND or externally biased within V_{CM} range		Vcc	V
V_{IL}	Single-Ended Input Low Voltage		GND		V
V_{I_SE}	Single-Ended Input Voltage Swing[6][7]		0.3	2	Vpp
V_{CM}	Single-Ended Input Common Mode Voltage		0.25	Vcc - 1.2	V

Figure 1. Single-Ended Input specifications for CLKin pins

AC coupled input circuit:

For DC-balanced signals, an AC coupling circuit may appropriate to shift the input signal to within the VCM range. For large single-ended input signals, such as 3.3V or 2.5V LVCMOS, a 50 Ω load resistor should be placed near the input pin to attenuation the signal to prevent input overdrive as well as for line termination to minimize reflections. The load resistor can be put either before or after the capacitor. The CLKin input has an internal bias voltage of about 1.4 V, so the input can be AC coupled as shown in Figure 2. The output impedance of the CMOS driver plus Rs should be close to 50 Ω to match the characteristic impedance of the transmission line.

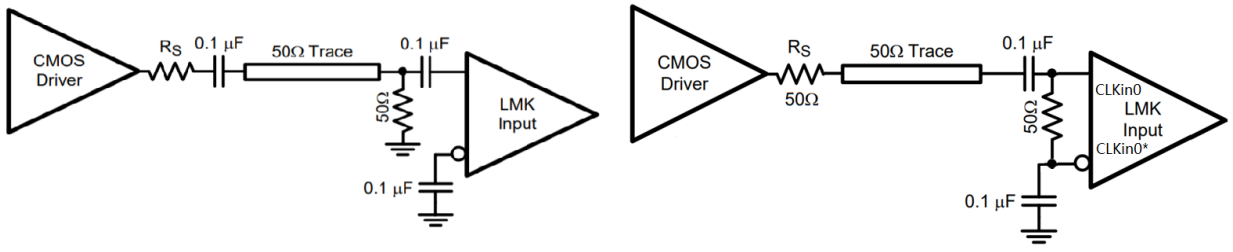

Figure 2. Single-Ended LVCMOS Input, AC Coupling

The potential risk for put the load resistor after the capacitor is oscillations when input is floating or in High Z mode. The 50 ohm resistance across the LMK inputs essentially makes the built in DC offset on the CLK inputs zero and thereby resulting in oscillations when input is floating or High Z mode. It is recommend to put the 50 ohm resistance before the capacitor.

DC coupled input circuit:

A single-ended clock may also be DC coupled to CLKin pin as shown in Figure 3. A 50-Ω load resistor should be placed near the CLKin input for signal attenuation and line termination. The external bias voltage should be within the specified input common voltage (VCM) range. This can be achieved using external biasing resistors in the kΩ range (RB1 and RB2) or another low-noise voltage reference. Another way is to using a thevenin termination. Both pull−up and pull−down resistors are used to provide the DC bios as well as the line termination.

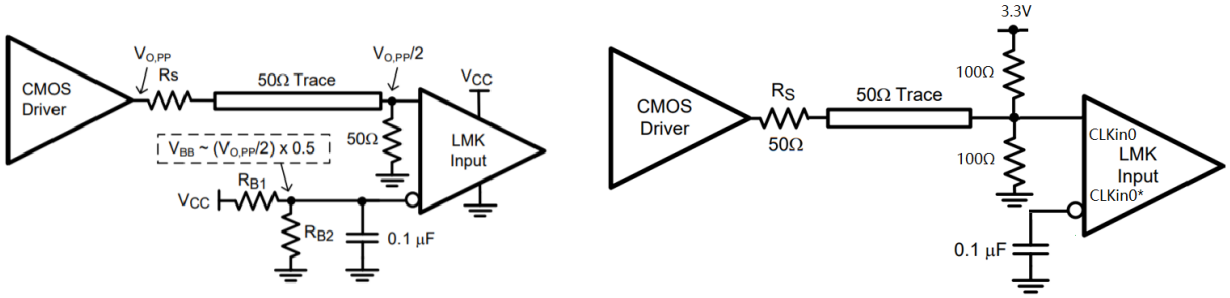

Figure 3. Single-Ended LVCMOS Input, DC Coupling with Common Mode Biasing

Although the bios voltage of the termination circuit may be different from the internal bios voltage(1.4V). There is no risk in operation or long-term reliability since the LMK device has internal AC coupling. Input stage is ac-coupled internally and there is a weak DC bias set on the input, this DC bias has an offset between the CLKIN pins which is designed to prevent oscillations when the inputs are floating/High Z. A high-level block diagram of input pin is shown in the Figure 4.

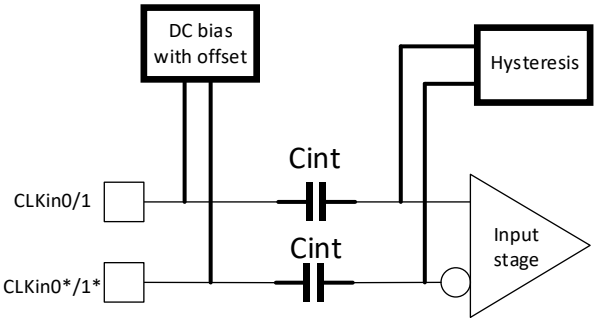

Figure 4. High-level block diagram of input pin