

Fast frequency switching using the “full assist” mode

Multicore VCO integrated PLL+VCO tend to suffer in frequency switching speed with important calibration time required for each frequency selected. LMX2594 provides a feature to fully calibrate for each frequency before active duty and switch between the available frequencies without calibration reducing the switching time by more than 45 usec. Please find below the frequency switching example using full assistance available on LMX2594.

3 frequencies are selected that are fairly close together on the output for test measurement reasons yet require large tuning capability for the LMX2594 because it has to switch VCO/capcode and amplitude settings. I followed the procedure in red below:

- 1. Calibrate offline all required frequencies at one convenient temperature**
Since LMX2594 support 125C temperature drift, The actual temperature where calibration is performed is not critical.
- 2. Readback all calibration data for each desired frequency. Save all data with your ASIC.**
*R110[7:5]: VCO core (rb_VCO_SEL)
R111[7:0]: Cap code (rb_VCO_CAPCTRL)
R112[8:0]: VCO amplitude (rb_VCO_DACISET)*
- 3. Place VCO configuration in FORCE mode once in active duty**
*R8[14]=1: VCO amplitude (VCO_DACISET_FORCE)
R8[11]=1: Cap code (VCO_CAPCTRL_FORCE)
R20[10]=1: VCO core (VCO_SEL_FORCE)*
- 4. Write all PLL and VCO data on the SPI interface**
*PLL: N, R, fraction, etc.
VCO: R20[13:11]=VCO_SEL, R19[7:0]=VCO_CAPCTRL, R16[8:0]=VCO_DACISET.
LMX2594 lock dynamically without calibration*

We pre calibrated 3 frequencies:

F= {1.4, 1.6 ,2.0} GHz.

In order to generate these frequencies the following configuration was used:

- 100 MHz reference with a200 MHz PFD using the input doubler to reduce inband noise on the PLL.
- CP current set to max at 15 mA.

Each frequency is generated with the following VCO/output divider configuration:

1.4 GHz => 11.2 GHz VCO with a divider by 8 on the output. VCO #4 is used for this.
1.6 GHz => 9.6 GHz VCO with a divider by 6 on the output. VCO #2 is used for this.
2.0 GHz => 8.0 GHz VCO with a divider by 4 on the output. VCO #1 is used for this.

We also needed to change the PFD delay settings for each frequency. In total, we need to change 6 registers for each frequency (including the 3 registers required for the VCO configuration) and no

calibration was needed at run time. We used a data generator to create the SPI transactions and used the maximum speed of LMX2594 with 75 MHz serial clock. Each register is now latched in in 320 nsec...so our six registers can be written in less than 2 usec.

The register sequence was made such that the PLL is able acquire lock as fast as possible so the sequence was:

- Select VCO
- Select cap_code
- Select N...PLL can now "start working toward lock"
- Select D
- Select VCO amplitude
- Select PFD delay

The register sequence for this device is summarized in the table below. They would likely be different for a different device...as you readback calibration data:

	1.6 GHz [hex]	2.0 GHz[hex]	1.4 GHz[hex]
VCO	14D448	14CC48	14E448
Cap code	13271C	13274B	13274A
N	240030	240028	240038
D	4B0880	4B0840	4B08C0
VCO amplitude	100113	100120	10015A
PFD delay	250304	250304	250404

We used a E5052 in modulation domain analysis to show the frequency as a function of time.

The pictures below shows the E5052 screenshot while the LMX2594 switches between these 3 frequencies. The second scrsreen shot shows a zoomed in function. The time between each marker is approximately the register time for a transaction. You can see dynamic lock engaged and started in less than 2 usec. More time would be needed in fractional mode for example as you would need to write more registers for the required configuration.

