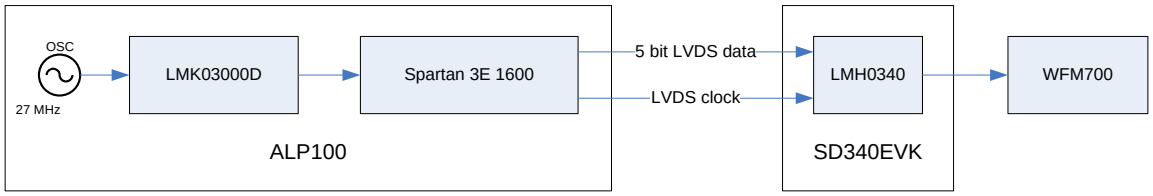
HD SDI Output Jitter of LMH0340 using LMK03000D as Clock Source for Xilinx FPGA

Purpose

To demonstrate the LMK03000D can be used to clock a data serializer and meet SMPTE 292M specifications. The serializer in this case is an LMH0340 plus a Xilinx Spartan 3E FPGA with National IP.

Test Setup



Test information:

- Measurements made with WFM700
- 27 MHz crystal oscillator reference
- 75% SMPTE Color Bars
- ALP100 Board with LMK03000D as clock source

Measurements

1080p30:

Lower Edge	Peak to peak jitter	Unit Interval	SMPTE 292M Specification
10 Hz	132 ps	0.195 UI	1 UI
100 kHz	79 ps	0.117 UI	0.2 UI

1080i30/M (M = 1.001):

Lower Edge	Peak to peak jitter	Unit Interval	SMPTE 292M Specification
10 Hz	138 ps	0.205 UI	1 UI
100 kHz	79 ps	0.117 UI	0.2 UI

Conclusion

The result shows that the LMK03000D clocking the data serializer of an LMH0340 plus a Xilinx Spartan 3E FPGA with National IP will meet the jitter performance specifications of SMPTE 292M.

Appendix A - LMK03000D Programming / Loop Filter

Programming information for frequency: 74.25/1.001

OSCin = 27 MHz
R = 91
N = 2000
VCO DIV = 2
CLK divider = 8 (program 4)
VCO Frequency = 1188/1.001 MHz
Charge Pump = 3.2 mA
Loop Filter BW = 16.5 kHz

While the programming information below for 74.25 MHz will set the output frequency to 74.25 MHz, it is possible to keep these 74.25/1.001 divider values and change only N = 2002 to achieve 74.25 MHz. This will keep the loop filter BW = 16.5 kHz and phase margin = 70 degrees and therefore jitter constant.

Programming information for frequency: 74.25 MHz

OSCin = 27 MHz
R = 45
N = 990
VCO DIV = 2
CLK divider = 8 (program 4)
VCO Frequency = 1188 MHz
Charge Pump = 3.2 mA
Loop Filter BW = 31.8 kHz

Decreasing the phase detector frequency from ~297 kHz (Total N = 2000*2) to 600 kHz (Total N = 990*2) results in the loop filter bandwidth widening to ~31.8 kHz and increases phase margin to 73.7 degrees. This increased loop bandwidth results in slightly lower jitter for 74.25 MHz.

Loop filter:

R2 = 18 k (external part)
R3 = 0.6 k (integrated, default in datasheet)
R4 = 0.2 k (integrated, default in datasheet)
C1 = 27 pF (external part)
C2 = 1.8 nF (external part)
C3 = 0 pF (integrated, default in datasheet)
C4 = 10 pF (integrated, default in datasheet)