HiTech Global ZYNQ UltraScale+™ RFSoC Development Platform

HTG-ZRF8 User Manual

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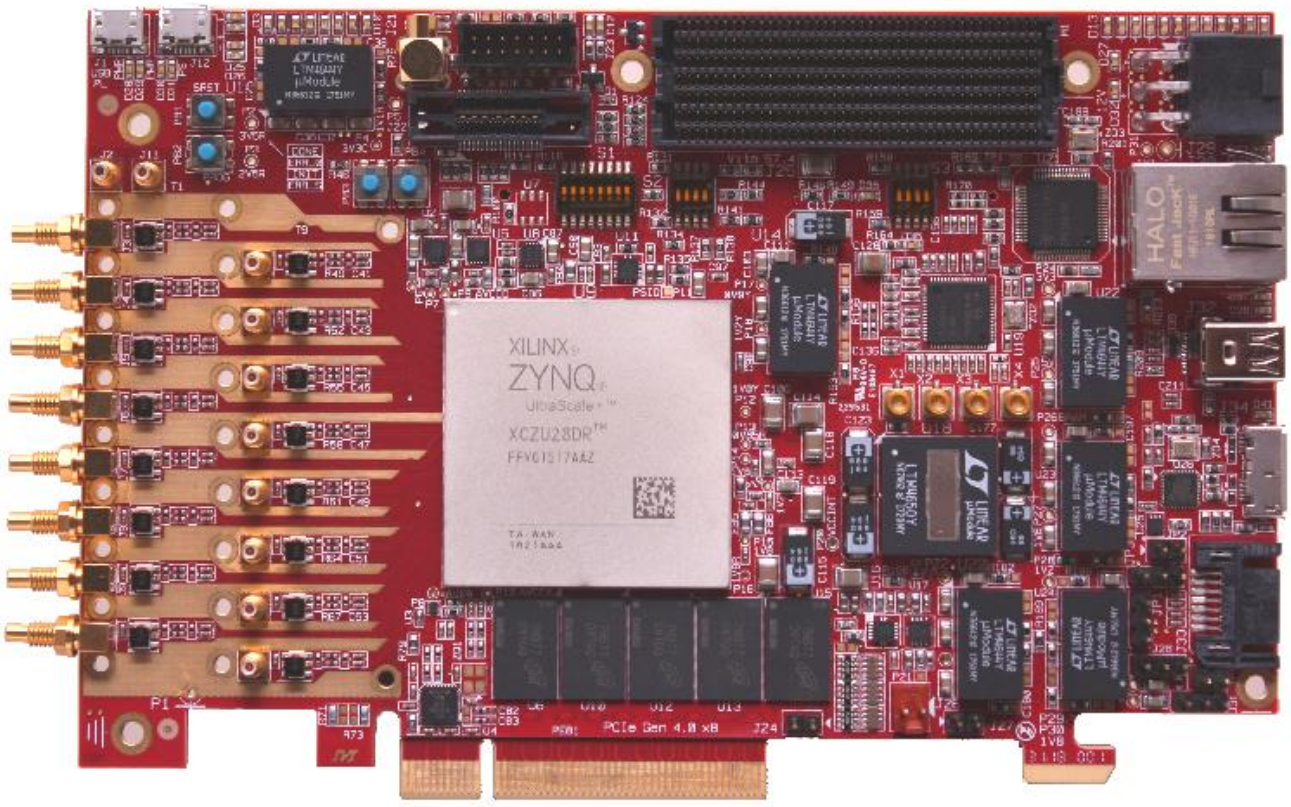

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Revision History

Date	Version	Notes
8/15/2017	1.0	

Table Of Contents

Tables & Figures

1.0) Overview

Populated with one Xilinx ZYNQ **UltraScale+ RFSoC** ZU25DR, ZU27DR, or **ZU28DR**, the HTG-ZRF8 provides access to large FPGA gate densities, multiple ADC/DAC ports, expandable I/Os ports and DDR4 memory for variety of different programmable applications.

The HTG-ZRF8 is supported by eight 12-bit ADC (4GSPS) and eight 14-bit DAC (6.4GSPS) ports. The ADC and DAC ports are supported through high-performance front panel micro Rf connectors.

The HTG-ZRF8 architecture allows easy and versatile functional expansion through one Vita 57.4 compliant (FMC+) port. The HTG-ZRF8 can host wide range of Vita57.1 /Vita57.4 compliant daughter cards.

The HTG-ZRF8 is supported by one 72-bit ECC DDR4 SODIMM socket providing access to up to 16 GB of SDRAM memory. The processor's side is supported by up to 2GB of DDR4 memory.

The HTG-ZRF8 can be used in PCI Express and Standalone mode and powered through its 6-pin Molex PCIe connector.

Table (1) illustrates key features of the supported FPGAs by the HTG-ZRF8 platform.

		Device Name	ZU25DR	ZU27DR	ZU28DR
Processing System (PS)	Application Processor Unit	Processor Core	**Quad-core** ARM® Cortex™-A53 MPCore™ up to 1.5GHz		
		Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB		
	Real-Time Processor Unit	Processor Core	**Dual-core** ARM Cortex-R5 MPCore up to 533MHz		
		Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core		
	External Memory	Dynamic Memory Interface	x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 with ECC		
		Static Memory Interfaces	NAND, 2x Quad-SPI		
	Connectivity	High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet		
		General Connectivity	2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO		
	Integrated Block Functionality	Power Management	Full / Low / PL / Battery Power Domains		
		Security	RSA, AES, and SHA		
		AMS - System Monitor	10-bit, 1MS/s – Temperature and Voltage Monitor		
PS to PL Interface			12 x 32/64/128b AXI Ports		
Programmable Logic (PL)	RF Data Converter Subsystem	12-bit, 4GSPS RF-ADC w/DDC	8	8	8
		12-bit, 2GSPS RF-ADC w/DDC	0	0	0
		14-bit, 6.4GSPS RF-DAC w/DUC	8	8	8
		SD-FEC	0	0	8
	Programmable Functionality	System Logic Cells (K)	678	930	930
		CLB LUTs (K)	310	425	425
	Memory	Max. Distributed RAM (Mb)	9.6	13.0	13.0
		Total Block RAM (Mb)	27.8	38.0	38.0
		UltraRAM (Mb)	13.5	22.5	22.5
	Integrated IP	DSP Slices	3,145	4,272	4,272
		PCI Express® Gen 3x16 / Gen4x8	1	2	2
		150G Interlaken	1	1	1
		100G Ethernet MAC/PCS w/RS-FEC	1	2	2
		AMS - System Monitor	1	1	1

Table (1): Summary of supported ZYNQ RFSoc UltraScale+ FPGA Features

2.0) HTG-ZRF8 Platform's Features

►Xilinx Zynq UltraScale+ RFSoc ZU25DR, ZU27DR, or ZU28DR
►x8 ADC (12-bit , 4GSPS) ports (SMCC connectors)
►x8 DAC (14-bit, 6.4GSPS) ports (SMCC connectors)
►Programmable ADC/DAC Clock Generator
►x8 PCI Express end-point Gen4
►x1 Vita57.4 FPGA Mezzanine Connector (FMC+) with 68 single-ended I/Os and 8 GTY (32.75Gbps) Serial Transceivers
►Independent DDR4 memory for the FPGA (up to 16GB SODIMM) and the ARM Processors (2GB component)
► x2 QSPI Configuration Flash devices
►x1 10/100/1000 Ethernet (RJ45) port (Processor)
►x1 MicroSD (Processor)
►x1 SATA (Processor)
►x1 Display Port (Processor)
►x1 USB2.0 / USB 3.0 port (Processor)
►x2 USB/UART (FPGA and Processor)
►Programmable Clocks (with default frequencies but programmable through I2C bus)
► 1PPS port
►ARM Debug Header
►FPGA JTAG Header
►External Synchronous Clock port
►6.6" x 4.25"
►**Supports both PCI Express and Standalone operations**
- 12V/8A Power adapter for standalone operation

3.0) Banks Assignment, Block Diagram, Clocks Diagram & Mechanical Drawing

Figure (1) , (2), (3) and (4) illustrate FPGA I/O bank assignment, block diagram , clocks diagram, and mechanical dimensions of the HTG-ZRF8 platform.

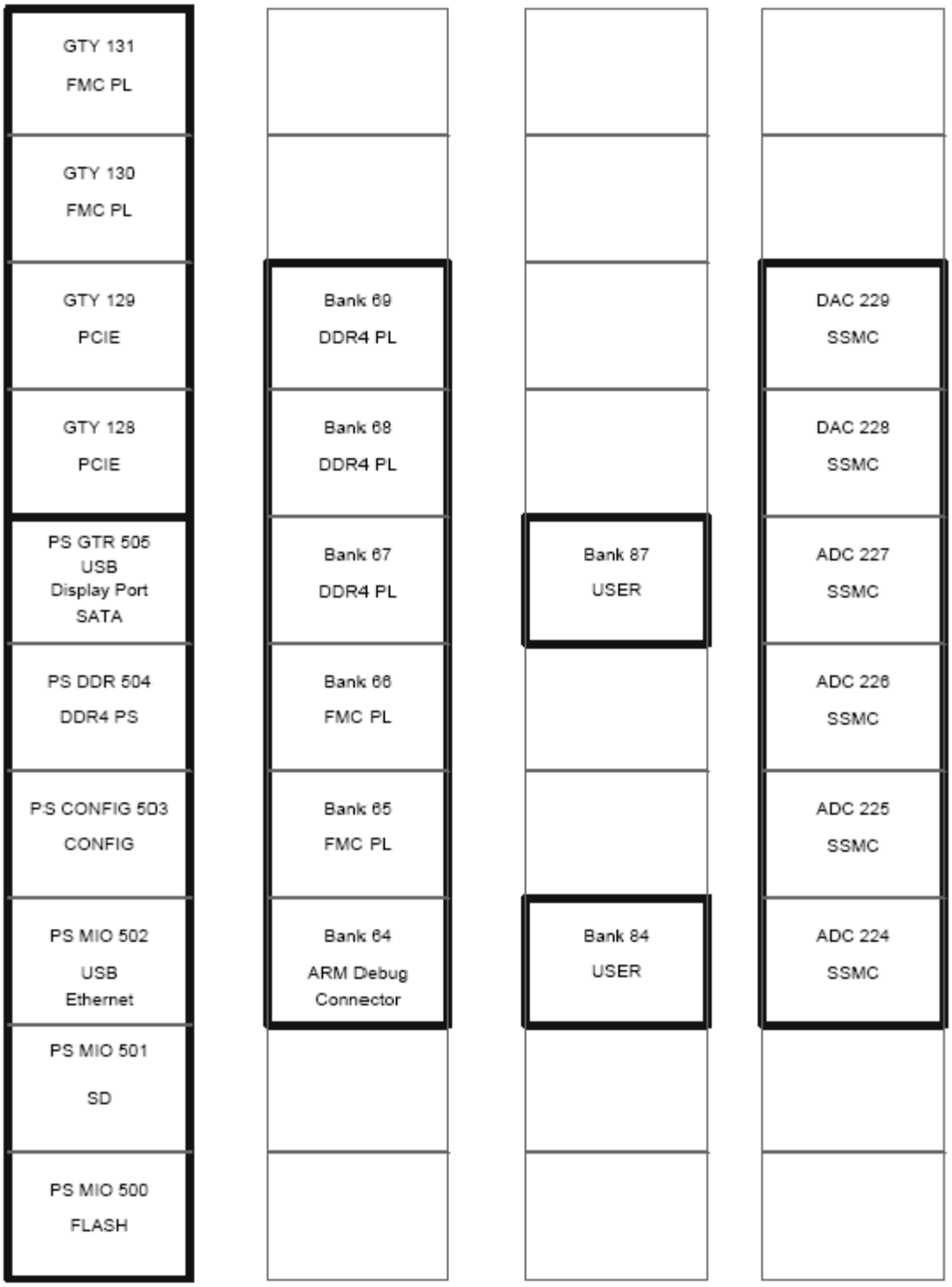


Figure (1): FPGA Bank Assignment

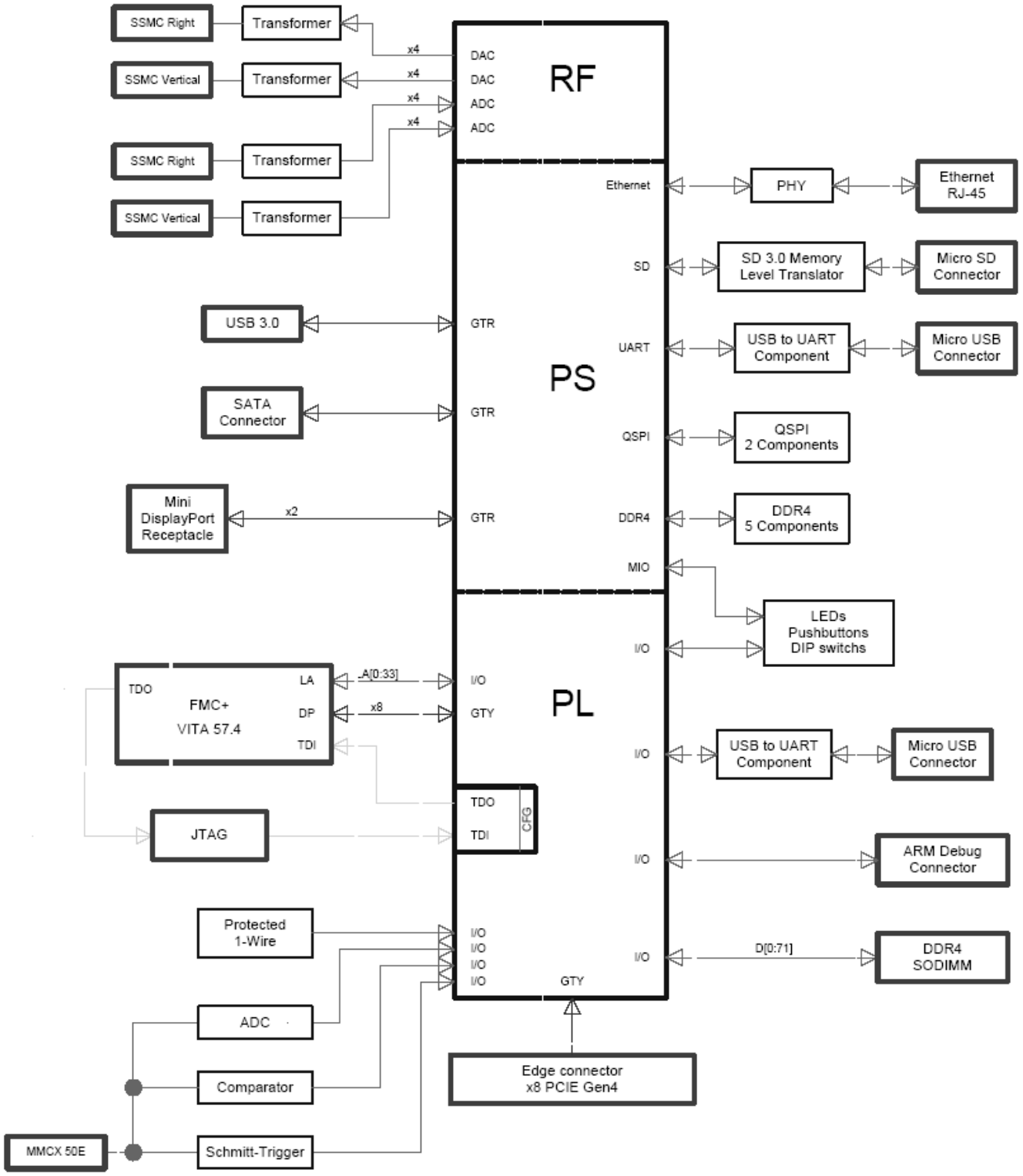


Figure (2): System Block Diagram

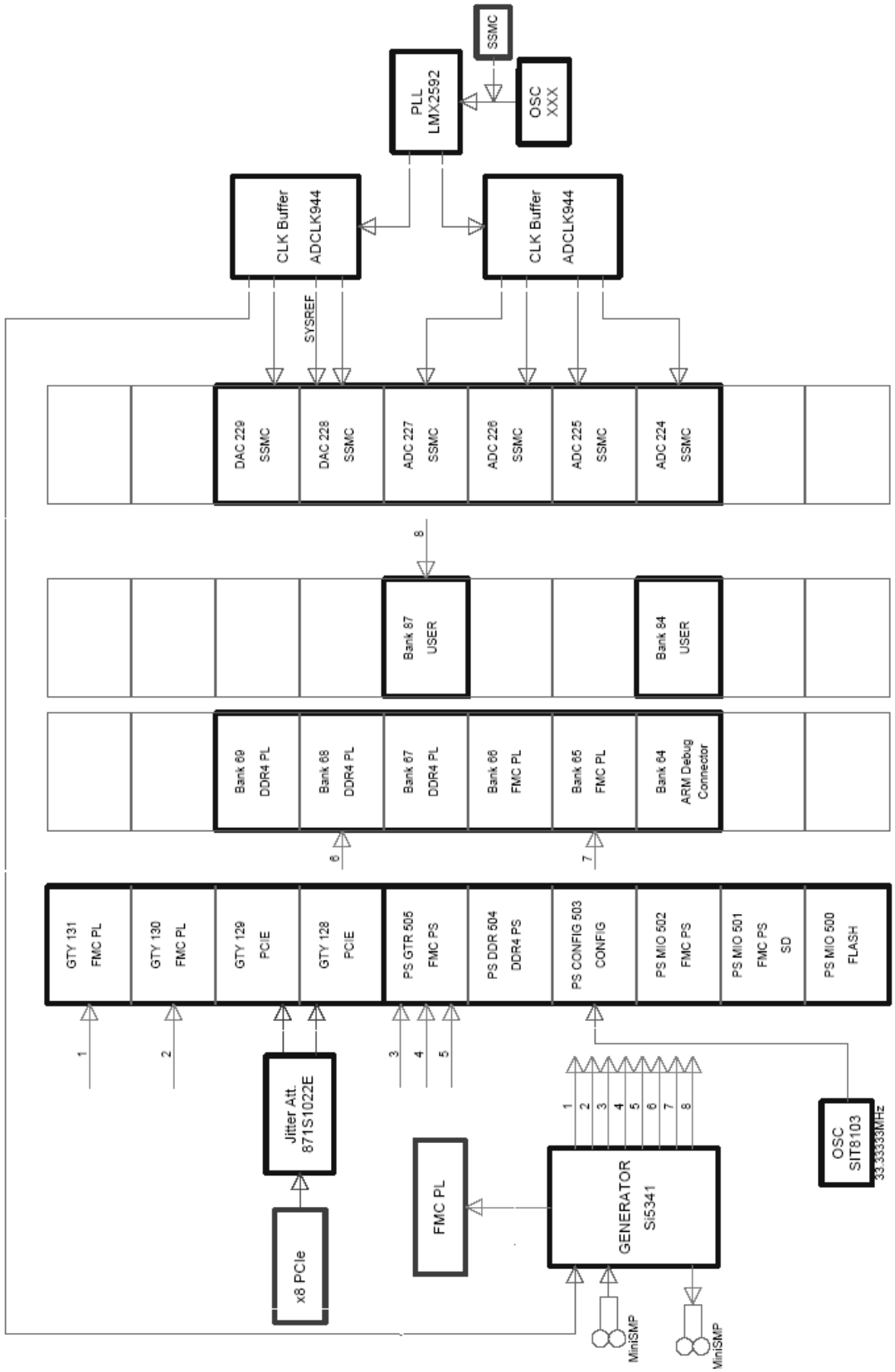


Figure (3): Clock Block Diagram

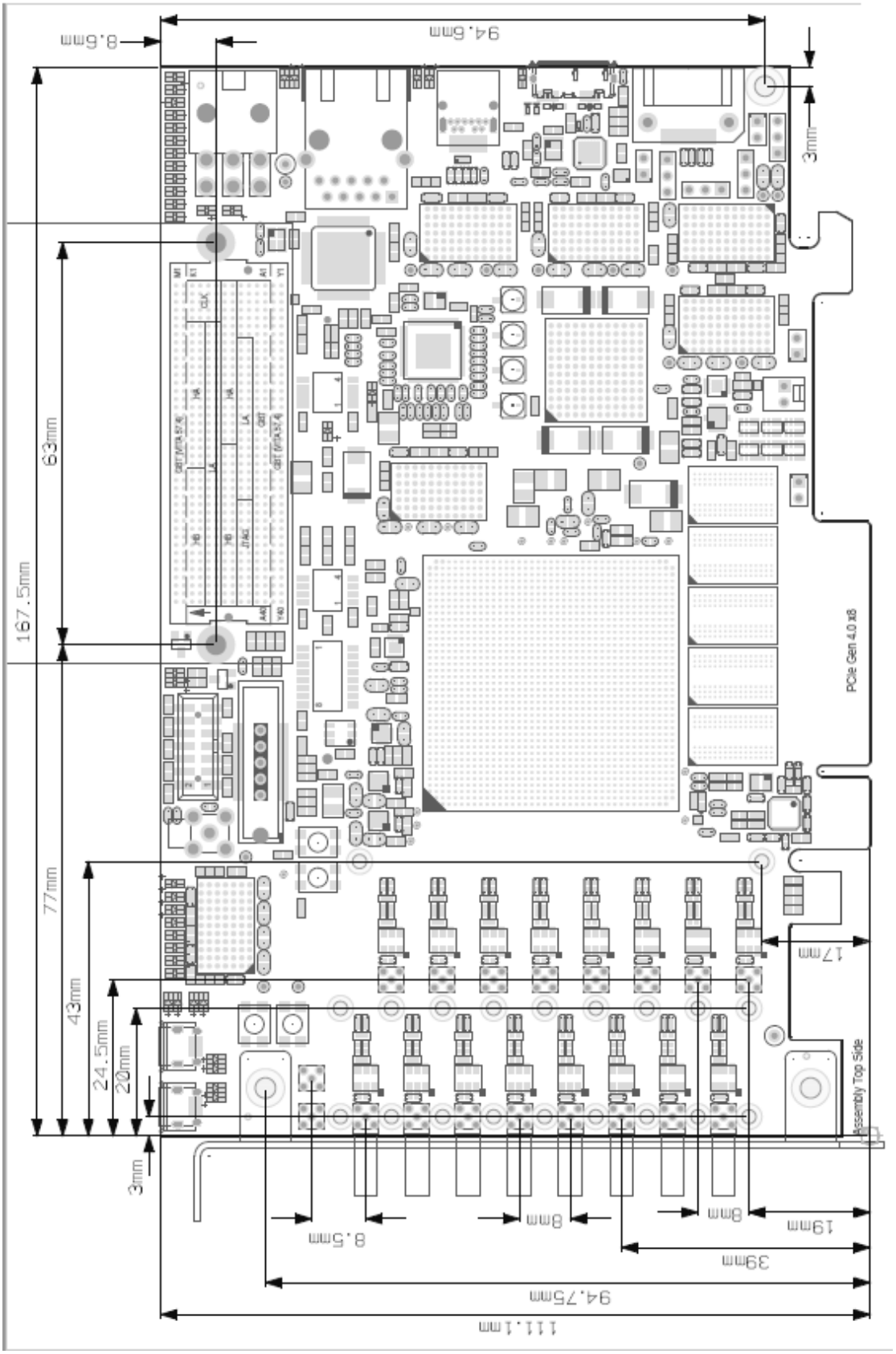


Figure (4): Mechanical Drawing

4.0) Clocks

The HTG-ZRF8 provides combination of fixed, programmable, and adjustable ultra-low-jitter clock sources for different interfaces as summarized by the table (2).

Source	Part Number (Manufacturer)	Default Value	Clock Function
U19	Si5341A	Programmable	User, DDR 4 , FMC+, Processor GTR & SMP
U40	SIT8103AC-23-18E-33.33333MHz	33.33 MHz	Processor
U4	871S1022EKLF (IDT)	100 MHz	PCI Express
U68	LMX2592RHA	Programmable	ADC & DAC
U69	VCC6-LAB-122M880000	122.88 MHz	ADC & DAC Input
ZQ1	7M-25.000MEEQ-T (not installed)	25 MHz	PCIe Standalone
ZQ2	7M48072002	48 MHz	U19 Main Reference
ZQ3	FA-238 25.0000MB	25 MHz	Ethernet
ZQ4	FA-238 24.0000MB	24 MHz	USB2
ZQ5	9HT10-32.768KDZF-T	32.768 KHz	PS_PADI/PS_PADO RTC
X1/X2	Mini SMP	Variable	U19 Additional External Output
X3/X4	SSMC Connector	Variable	U19 Additional External Input

Table (2): Main Clocks

►*The ICS871S1022 (U4)is a PLL-based clock generator specifically designed for PCI Express Clock Generation applications. The device generates 100MHz, 125MHz, 250MHz or 500MHz from either a 25MHz fundamental mode crystal or a 100MHz recovered clock. The ICS871S1022 has two modes of operation: (1) high frequency jitter attenuator and (2) high performance clock synthesizer mode. When in jitter attenuator mode, the ICS871S1022 is able to both suppress high frequency noise components and function as a frequency translator. Designed to receive a jittery and noisy clock from an external source, the ICS871S1022 uses FemtoClock® technology to clean up the incoming clock and translate the frequency to one of the four common PCI Express frequencies. When in synthesizer mode, the device is able to generate high performance SSC and non-SSC clocks from a low cost external, 25MHz, fundamental mode crystal. The ICS871S1022 uses FemtoClock® technology to generate low noise clock outputs capable of providing the seed frequencies for the common PCI Express link rates.*

Additional product information is available at http://www.idt.com/products/clocks-timing/application-specific-clocks/pci-express-pcie-clocks/871s1022-differential-07v-differential-pci-express-jitter-attenuator

►*The any-frequency, any-output Si5341(U19) clock generator combines a wide-band PLL with proprietary MultiSynth fractional synthesizer technology to offer a versatile and high performance clock generator platform. This highly flexible architecture is capable of synthesizing a wide range of integer and no-integer related frequencies up to 712.5 MHz on 10 differential clock outputs while delivering sub-100 fs rms phase jitter performance with 0 ppm error. Each of the clock outputs can be assigned its own format and output voltage enabling the Si5341/40 to replace multiple clock ICs and oscillators with a single device making it a true "clock tree on a chip".*

The Si5341/40 can be quickly and easily configured using **ClockBuilder Pro** software. The device can be programmed in circuit via I2C and SPI serial interfaces or using Silicon Labs' dongle and the J28 header.

https://www.silabs.com/products/development-tools/software/clockbuilder-pro-software

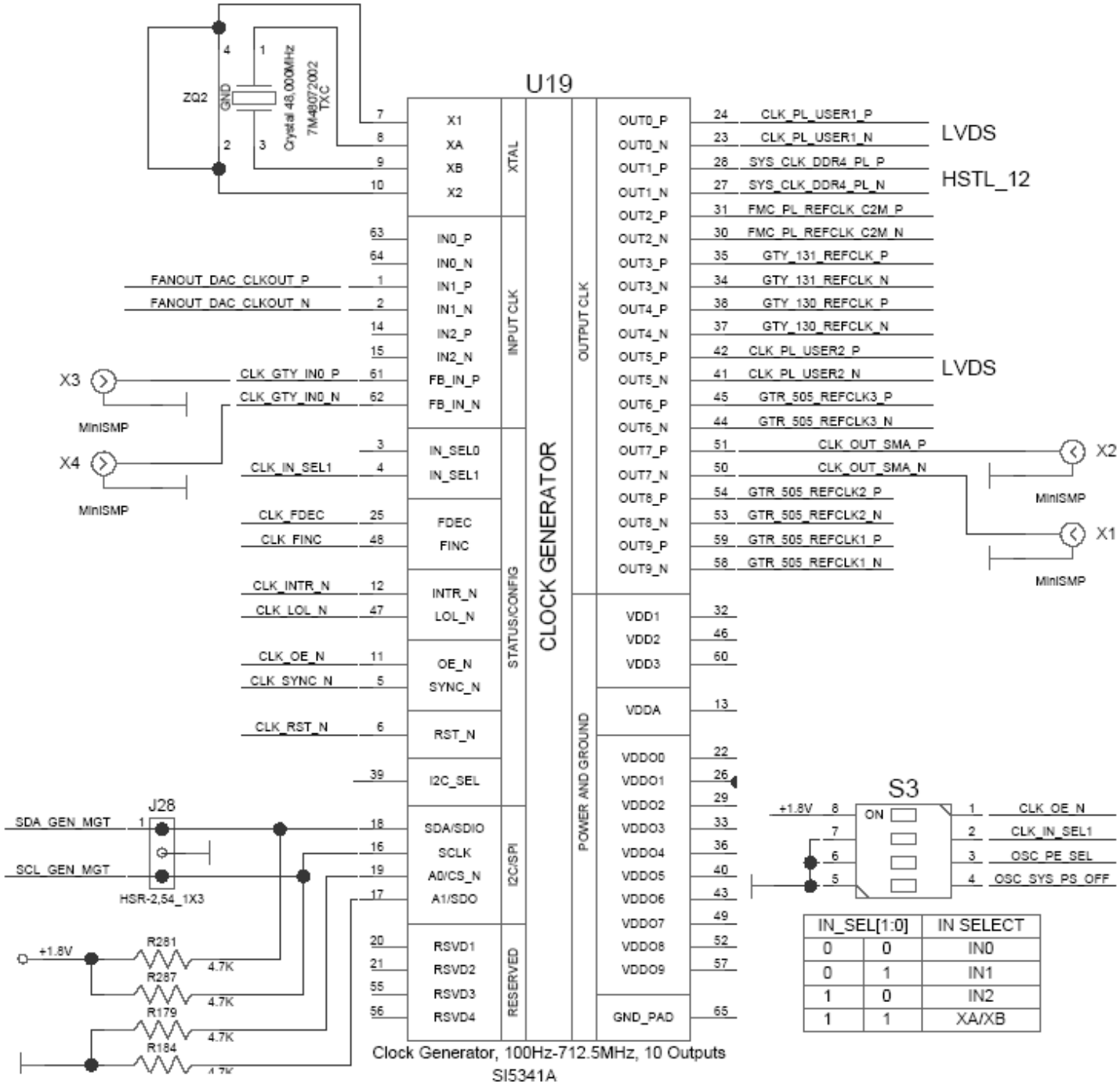


Figure (5): Si5341 Clock Generator Block Diagram

Table (3) provides summary of clock outputs of the Si5341 (U46) clock generator.

Output #	Signal Name	Destination	FPGA Pin Number
OUT0_P	CLK_PL_USER1_P	FPGA Bank 87 (User Clock)	C8
OUT0_N	CLK_PL_USER1_N		C7
OUT1_P	SYS_CLK_DDR4_PL_P	FPGA Bank67 (DDR4 SODIMM Clock)	G13
OUT1_N	SYS_CLK_DDR4_PL_N		G12
OUT2_P	FMC_PL_REFCLK_C2M_P	FMC + Connector (Carrier to Mezzanine Clock)	-
OUT2_N	FMC_PL_REFCLK_C2M_N		-
OUT3_P	GTY_131_REFCLK_P	FPGA GTY 131 (FMC+ DP4-DP7)	P31
OUT3_N	GTY_131_REFCLK_N		P32
OUT4_P	GTY_130_REFCLK_P	FPGA GTY 130 (FMC+ DP0-DP3)	U33
OUT4_N	GTY_130_REFCLK_N		U34
OUT5_P	CLK_PL_USER2_P	FPGA Bank 64 (User Clock)	AM15
OUT5_N	CLK_PL_USER2_N		AN15
OUT6_P	GTR_505_REFCLK3_P	FPGA GTR 505 (USB3/SATA/Display Port)	AC34
OUT6_N	GTR_505_REFCLK3_N		AC35
OUT7_P	CLK_OUT_SMA_P	X1 /X2 Mini SMP Connector (Output Clock)	-
OUT7_N	CLK_OUT_SMA_N		-
OUT8_P	GTR_505_REFCLK2_P	FPGA GTR 505 (USB3/SATA/Display Port)	AE34
OUT8_N	GTR_505_REFCLK2_N		AE35
OUT9_P	GTR_505_REFCLK1_P	FPGA GTR 505 (USB3/SATA/Display Port)	AG34
OUT9_N	GTR_505_REFCLK1_N		AG35

Table (3): Summary of the Si5341 (U46) Clock Outputs

►*The LMX2592 (U68) is a high performance wideband synthesizer (PLL with integrated VCO). The output frequency range is from 20 MHz to 5.5 GHz. The VCO core covers an octave from 3.55 to 7.1 GHz. The output channel divider covers the frequency range from 20 MHz to the low bound of the VCO core.*

The input signal frequency has a wide range from 5 to 1400 MHz. Following the input, there is an programmable OSCin doubler, a pre-R divider (previous to multiplier), a multiplier, and then a post-R divider (after multiplier) for flexible frequency planning between the input (OSCin) and the phase detector.

The phase detector (PFD) can take frequencies from 5 to 200 MHz, but also has extended modes down to 0.25 MHz and up to 400 MHz. The phase-lock loop (PLL) contains a Sigma-Delta modulator (1st to 4th order) for fractional N-divider values. The fractional denominator is programmable to 32-bit long, allowing a very fine resolution of frequency step. There is a phase adjust feature that allows shifting of the output phase in relation to the input (OSCin) by a fraction of the size of the fractional denominator.

The output power is programmable and can be designed for high power at a specific frequency by the pullup component at the output pin.

The digital logic is a standard 4-wire SPI or uWire interface and is 1.8-V and 3.3-V compatible.

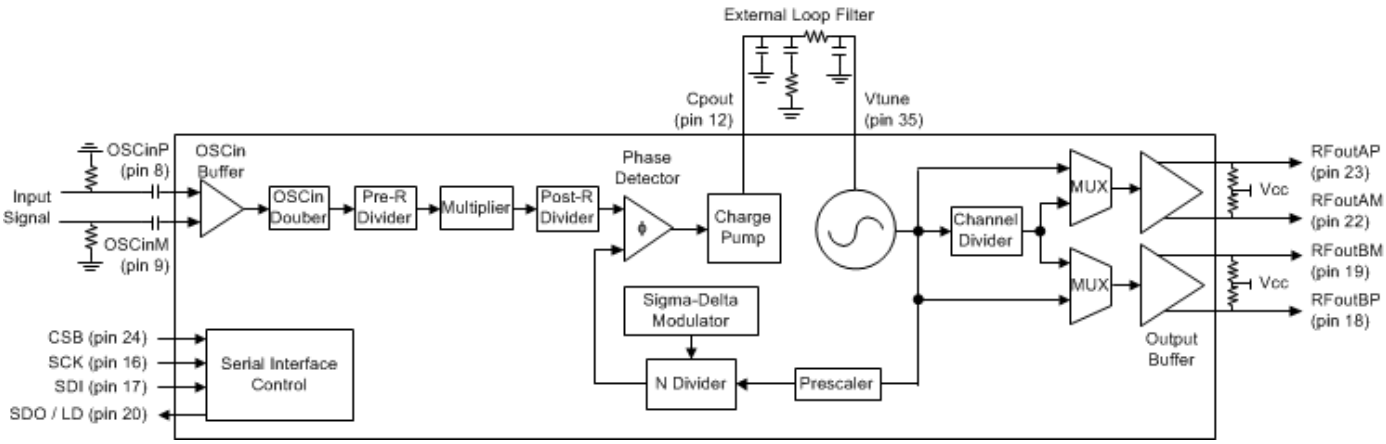


Figure (6): LMX2592 Block Diagram

5.0) PCI Express

The HTG-ZRF8 platform provides an 8-lane PCI Express Gen4 (8@16Gbps) end-point interface through integration of eight GTY serial transceivers (GTY 128 and 129) and one eight-lane hard-coded PCIe Link Layer Controller (X0Y0) of the FPGA.

Table (4) illustrates signal names and FPGA pin assignment for the PCI Express interface.

PCIe Signal Name	FPGA Signal Name	FPGA Pin Number
PCIE_CLK_N	PCIE_CLK0_MGT0_N	AA34
PCIE_CLK_P	PCIE_CLK0_MGT0_P	AA33
PCIE_CLK_N	PCIE_CLK0_MGT1_N	Y32
PCIE_CLK_P	PCIE_CLK0_MGT1_P	Y31
PCIE_CLK_N	PCIE_CLK1_MGT_N	W34
PCIE_CLK_P	PCIE_CLK1_MGT_P	W33
PERST	PCIE_PERST_N_F	AJ13
PETN0	PCIE_RX[0]_N	AA39
PETP0	PCIE_RX[0]_P	AA38
PETN1	PCIE_RX[1]_N	W39
PETP1	PCIE_RX[1]_P	W38
PETN2	PCIE_RX[2]_N	U39
PETP2	PCIE_RX[2]_P	U38
PETN3	PCIE_RX[3]_N	R39
PETP3	PCIE_RX[3]_P	R38
PETN4	PCIE_RX[4]_N	N39
PETP4	PCIE_RX[4]_P	N38

PETN5	PCIE_RX[5]_N	M37
PETP5	PCIE_RX[5]_P	M36
PETN6	PCIE_RX[6]_N	L39
PETP6	PCIE_RX[6]_P	L38
PETN7	PCIE_RX[7]_N	K37
PETP7	PCIE_RX[7]_P	K36
PERN0	PCIE_TX[0]_N	Y36
PERP0	PCIE_TX[0]_P	Y35
PERN1	PCIE_TX[1]_N	V36
PERP1	PCIE_TX[1]_P	V35
PERN2	PCIE_TX[2]_N	T36
PERP2	PCIE_TX[2]_P	T35
PERN3	PCIE_TX[3]_N	R34
PERP3	PCIE_TX[3]_P	R33
PERN4	PCIE_TX[4]_N	P36
PERP4	PCIE_TX[4]_P	P35
PERN5	PCIE_TX[5]_N	N34
PERP5	PCIE_TX[5]_P	N33
PERN6	PCIE_TX[6]_N	L34
PERP6	PCIE_TX[6]_P	L33
PERN7	PCIE_TX[7]_N	J34
PERP7	PCIE_TX[7]_P	J33
WAKE	PCIE_WAKE_N	E7

Table (4): PCI Express FPGA Pin Assignments

5.1) PCI Express Clock

The HTG-ZRF8 platform is supported by an auxiliary PCI Express jitter attenuator chip (871S1022EKLF) cleaning the 100MHz clock received by host PCs or servers. The jitter attenuator can also generate clock for the PCIe interface independent from host PCs or servers through its 25MHz (ZQ1) oscillator. This jitter attenuator circuit can be bypassed by uninstalling R104 and R105 resistors and installing C82 and C83 capacitors.

Figure (7) illustrates clock circuit of the PCI Express interface and Jitter Attenuator.

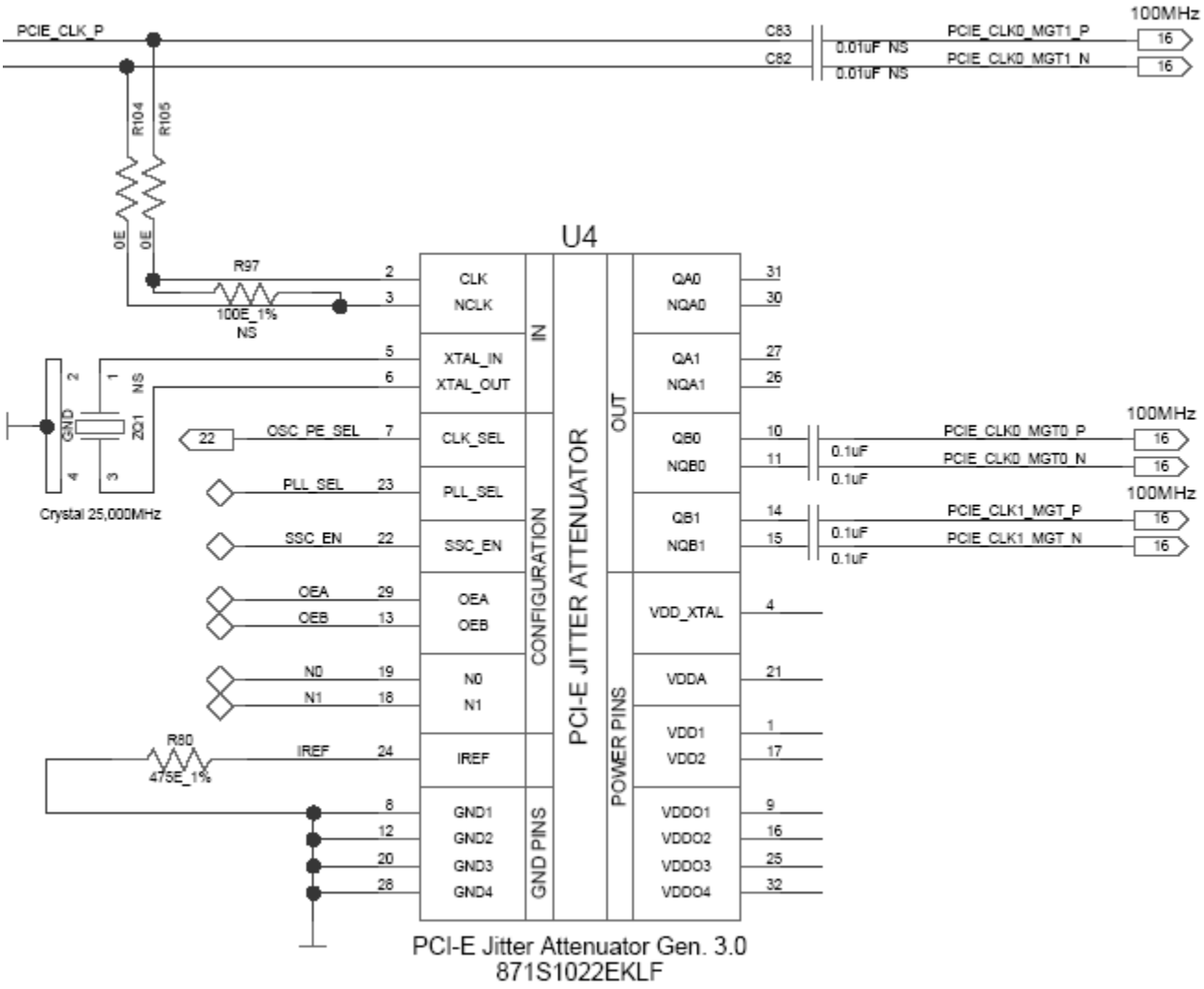


Figure (7): PCI Express Clock Circuit

PCI Express clock frequency value is set to 100 MHz by default. The output clock value can be adjusted by selecting N1:N0 attributes as shown by table (5) and figure (8).

INPUTS				OUTPUTS
CLK_SEL	IN (MHz)	N1:N0	N Divider	(MHz)
0	100	0 0	5	100
0	100	0 1	4	125
0	100	1 0	2	250
0	100	1 1	1	500
1	25	0 0	5	100
1	25	0 1	4	125
1	25	1 0	2	250
1	25	1 1	1	500

Table (5): PCI Express Clock Circuit

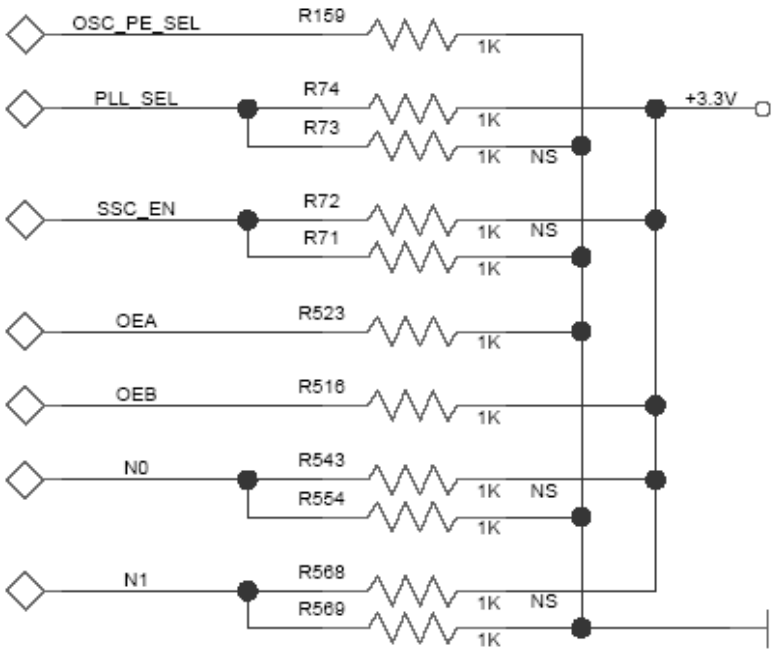


Figure (8): PCI Express Clock Enable Circuit

6.0) DDR-4 Memory

The HTG-ZRF8 platform supports one DDR4 SODIMM socket providing access to up to 16GB of memory through the FPGA programmable logic and five DDR4 components providing access to 2GB of memory through the processor's block of the FPGA.

Table (6) and (7) illustrate the FPGA bank assignment for the DDR4 SODIMM and Component interfaces.

DDR4 SODIMM Signal Name	FPGA Pin Number
DDR4_PL_A[0]	F11
DDR4_PL_A[1]	C13
DDR4_PL_A[2]	F14
DDR4_PL_A[3]	F10
DDR4_PL_A[4]	E11
DDR4_PL_A[5]	E13
DDR4_PL_A[6]	B13
DDR4_PL_A[7]	E12
DDR4_PL_A[8]	A11
DDR4_PL_A[9]	C12
DDR4_PL_A[10]	K13
DDR4_PL_A[11]	C15
DDR4_PL_A[12]	C11
DDR4_PL_A[13]	K10
DDR4_PL_A[14]	B14
DDR4_PL_A[15]	H12

DDR4_PL_A[16]	K12
DDR4_PL_ACT_N	B15
DDR4_PL_ALERT_N	D14
DDR4_PL_BA[0]	H13
DDR4_PL_BA[1]	A14
DDR4_PL_BG[0]	B12
DDR4_PL_BG[1]	D11
DDR4_PL_CK0_C	J10
DDR4_PL_CK0_T	J11
DDR4_PL_CK1_C	J13
DDR4_PL_CK1_T	J14
DDR4_PL_CKE0	A12
DDR4_PL_CKE1	A15
DDR4_PL_CS0_N	H10
DDR4_PL_CS1_N	E14
DDR4_PL_CS2_N	K11
DDR4_PL_CS3_N	F12
DDR4_PL_DM_DBI_N[0]	N14
DDR4_PL_DM_DBI_N[1]	J15
DDR4_PL_DM_DBI_N[2]	G17
DDR4_PL_DM_DBI_N[3]	D18
DDR4_PL_DM_DBI_N[4]	J23
DDR4_PL_DM_DBI_N[5]	F21
DDR4_PL_DM_DBI_N[6]	C23
DDR4_PL_DM_DBI_N[7]	N20
DDR4_PL_DM_DBI_N[8]	J8
DDR4_PL_DQ[0]	M12
DDR4_PL_DQ[1]	M13
DDR4_PL_DQ[2]	N15
DDR4_PL_DQ[3]	M17
DDR4_PL_DQ[4]	L12
DDR4_PL_DQ[5]	N13
DDR4_PL_DQ[6]	M15
DDR4_PL_DQ[7]	N17
DDR4_PL_DQ[8]	K17
DDR4_PL_DQ[9]	L17
DDR4_PL_DQ[10]	J19
DDR4_PL_DQ[11]	H16
DDR4_PL_DQ[12]	J16
DDR4_PL_DQ[13]	K16
DDR4_PL_DQ[14]	H17

DDR4_PL_DQ[15]	J18
DDR4_PL_DQ[16]	E16
DDR4_PL_DQ[17]	F15
DDR4_PL_DQ[18]	E17
DDR4_PL_DQ[19]	H18
DDR4_PL_DQ[20]	F16
DDR4_PL_DQ[21]	G15
DDR4_PL_DQ[22]	E18
DDR4_PL_DQ[23]	G18
DDR4_PL_DQ[24]	C16
DDR4_PL_DQ[25]	D15
DDR4_PL_DQ[26]	C17
DDR4_PL_DQ[27]	A19
DDR4_PL_DQ[28]	A16
DDR4_PL_DQ[29]	D16
DDR4_PL_DQ[30]	A17
DDR4_PL_DQ[31]	B19
DDR4_PL_DQ[32]	H23
DDR4_PL_DQ[33]	J21
DDR4_PL_DQ[34]	H22
DDR4_PL_DQ[35]	K24
DDR4_PL_DQ[36]	G23
DDR4_PL_DQ[37]	H21
DDR4_PL_DQ[38]	G22
DDR4_PL_DQ[39]	L24
DDR4_PL_DQ[40]	E21
DDR4_PL_DQ[41]	F20
DDR4_PL_DQ[42]	E23
DDR4_PL_DQ[43]	F24
DDR4_PL_DQ[44]	D21
DDR4_PL_DQ[45]	E22
DDR4_PL_DQ[46]	E24
DDR4_PL_DQ[47]	G20
DDR4_PL_DQ[48]	C20
DDR4_PL_DQ[49]	A20
DDR4_PL_DQ[50]	B24
DDR4_PL_DQ[51]	C21
DDR4_PL_DQ[52]	B20
DDR4_PL_DQ[53]	A21
DDR4_PL_DQ[54]	C22
DDR4_PL_DQ[55]	A24

DDR4_PL_DQ[56]	L19
DDR4_PL_DQ[57]	L21
DDR4_PL_DQ[58]	L23
DDR4_PL_DQ[59]	N19
DDR4_PL_DQ[60]	L20
DDR4_PL_DQ[61]	M19
DDR4_PL_DQ[62]	L22
DDR4_PL_DQ[63]	M20
DDR4_PL_DQ[64]	F9
DDR4_PL_DQ[65]	G7
DDR4_PL_DQ[66]	H6
DDR4_PL_DQ[67]	G6
DDR4_PL_DQ[68]	G9
DDR4_PL_DQ[69]	H7
DDR4_PL_DQ[70]	K9
DDR4_PL_DQ[71]	J9
DDR4_PL_DQS_C[0]	L14
DDR4_PL_DQS_C[1]	K18
DDR4_PL_DQS_C[2]	F19
DDR4_PL_DQS_C[3]	B17
DDR4_PL_DQS_C[4]	H20
DDR4_PL_DQS_C[5]	D24
DDR4_PL_DQS_C[6]	A22
DDR4_PL_DQS_C[7]	K22
DDR4_PL_DQS_C[8]	G8
DDR4_PL_DQS_T[0]	L15
DDR4_PL_DQS_T[1]	K19
DDR4_PL_DQS_T[2]	G19
DDR4_PL_DQS_T[3]	B18
DDR4_PL_DQS_T[4]	J20
DDR4_PL_DQS_T[5]	D23
DDR4_PL_DQS_T[6]	B22
DDR4_PL_DQS_T[7]	K21
DDR4_PL_DQS_T[8]	H8
DDR4_PL_EVENT_N	G14
DDR4_PL_ODT0	J7
DDR4_PL_ODT1	H11
DDR4_PL_PAR	G10
DDR4_PL_RST_N	D13

Table (6): DDR4 FPGA Pin Assignment (SODIMM-PL Side)

DDR4 Components Signal Name	FPGA Pin Number
DDR4_PS_A[0]	AV31
DDR4_PS_A[1]	AW28
DDR4_PS_A[2]	AV28
DDR4_PS_A[3]	AU29
DDR4_PS_A[4]	AW31
DDR4_PS_A[5]	AU28
DDR4_PS_A[6]	AL29
DDR4_PS_A[7]	AM30
DDR4_PS_A[8]	AM29
DDR4_PS_A[9]	AP29
DDR4_PS_A[10]	AT31
DDR4_PS_A[11]	AT32
DDR4_PS_A[12]	AT30
DDR4_PS_A[13]	AU32
DDR4_PS_A[14]	AR28
DDR4_PS_A[15]	AP30
DDR4_PS_A[16]	AP28
DDR4_PS_ACT_N	AL30
DDR4_PS_ALERT_N	AL32
DDR4_PS_BA[0]	AN30
DDR4_PS_BA[1]	AM32
DDR4_PS_BG[0]	AN32
DDR4_PS_CK_C	AV30
DDR4_PS_CK_T	AU30
DDR4_PS_CKE	AW30
DDR4_PS_CS_N	AW29
DDR4_PS_DM_DBI_N[0]	AU23
DDR4_PS_DM_DBI_N[1]	AT27
DDR4_PS_DM_DBI_N[2]	AL24
DDR4_PS_DM_DBI_N[3]	AM27
DDR4_PS_DM_DBI_N[4]	AV36
DDR4_PS_DM_DBI_N[5]	AT35
DDR4_PS_DM_DBI_N[6]	AM36
DDR4_PS_DM_DBI_N[7]	AJ32
DDR4_PS_DM_DBI_N[8]	AR38
DDR4_PS_DQ[0]	AW25
DDR4_PS_DQ[1]	AW24
DDR4_PS_DQ[2]	AV25
DDR4_PS_DQ[3]	AW23
DDR4_PS_DQ[4]	AV23

DDR4_PS_DQ[5]	AV22
DDR4_PS_DQ[6]	AR24
DDR4_PS_DQ[7]	AR23
DDR4_PS_DQ[8]	AT25
DDR4_PS_DQ[9]	AP26
DDR4_PS_DQ[10]	AU25
DDR4_PS_DQ[11]	AR27
DDR4_PS_DQ[12]	AU27
DDR4_PS_DQ[13]	AV26
DDR4_PS_DQ[14]	AV27
DDR4_PS_DQ[15]	AW26
DDR4_PS_DQ[16]	AP25
DDR4_PS_DQ[17]	AP24
DDR4_PS_DQ[18]	AP23
DDR4_PS_DQ[19]	AN25
DDR4_PS_DQ[20]	AM25
DDR4_PS_DQ[21]	AK24
DDR4_PS_DQ[22]	AN23
DDR4_PS_DQ[23]	AK23
DDR4_PS_DQ[24]	AK26
DDR4_PS_DQ[25]	AL25
DDR4_PS_DQ[26]	AK28
DDR4_PS_DQ[27]	AK27
DDR4_PS_DQ[28]	AN27
DDR4_PS_DQ[29]	AN26
DDR4_PS_DQ[30]	AN28
DDR4_PS_DQ[31]	AM28
DDR4_PS_DQ[32]	AU39
DDR4_PS_DQ[33]	AU38
DDR4_PS_DQ[34]	AU37
DDR4_PS_DQ[35]	AU35
DDR4_PS_DQ[36]	AV38
DDR4_PS_DQ[37]	AW36
DDR4_PS_DQ[38]	AV35
DDR4_PS_DQ[39]	AW35
DDR4_PS_DQ[40]	AU33
DDR4_PS_DQ[41]	AV33
DDR4_PS_DQ[42]	AW34
DDR4_PS_DQ[43]	AW33
DDR4_PS_DQ[44]	AR34
DDR4_PS_DQ[45]	AR33

DDR4_PS_DQ[46]	AP33
DDR4_PS_DQ[47]	AP34
DDR4_PS_DQ[48]	AL39
DDR4_PS_DQ[49]	AM38
DDR4_PS_DQ[50]	AM39
DDR4_PS_DQ[51]	AN38
DDR4_PS_DQ[52]	AM35
DDR4_PS_DQ[53]	AM34
DDR4_PS_DQ[54]	AN36
DDR4_PS_DQ[55]	AN35
DDR4_PS_DQ[56]	AK32
DDR4_PS_DQ[57]	AK31
DDR4_PS_DQ[58]	AJ31
DDR4_PS_DQ[59]	AJ30
DDR4_PS_DQ[60]	AH30
DDR4_PS_DQ[61]	AG32
DDR4_PS_DQ[62]	AF32
DDR4_PS_DQ[63]	AG30
DDR4_PS_DQ[64]	AT36
DDR4_PS_DQ[65]	AR36
DDR4_PS_DQ[66]	AT39
DDR4_PS_DQ[67]	AP35
DDR4_PS_DQ[68]	AR39
DDR4_PS_DQ[69]	AP38
DDR4_PS_DQ[70]	AP36
DDR4_PS_DQ[71]	AP39
DDR4_PS_DQS_C[0]	AU24
DDR4_PS_DQS_C[1]	AT26
DDR4_PS_DQS_C[2]	AM24
DDR4_PS_DQS_C[3]	AL27
DDR4_PS_DQS_C[4]	AW37
DDR4_PS_DQS_C[5]	AU34
DDR4_PS_DQS_C[6]	AN37
DDR4_PS_DQS_C[7]	AH32
DDR4_PS_DQS_C[8]	AT37
DDR4_PS_DQS_T[0]	AT24
DDR4_PS_DQS_T[1]	AR26
DDR4_PS_DQS_T[2]	AM23
DDR4_PS_DQS_T[3]	AL26
DDR4_PS_DQS_T[4]	AV37
DDR4_PS_DQS_T[5]	AT34

DDR4_PS_DQS_T[6]	AM37
DDR4_PS_DQS_T[7]	AH31
DDR4_PS_DQS_T[8]	AR37
DDR4_PS_ODT	AV32
DDR4_PS_PAR	AN31
DDR4_PS_RST_N	AM33
SYS_CLK_DDR4_PL_N	G12
SYS_CLK_DDR4_PL_P	G13

Table (7) DDR4 FPGA Pin Assignment (Components-PS Side)

6.1) DDR4 Clock

The DDR4 SODIMM clock is generated by programming OUT1 of the Si5341 clock generator.

7.0) FPGA Mezzanine Card (FMC+) Interface (Vita57.4)

The HTG-ZRF8 platform is populated with one Vita57.4 compliant FMC+ connector with 68 single-ended I/Os and 8 GTY (32.75Gbps) Serial Transceivers. This expansion port hosts Vita57.1 or Vita57.4 compliant daughter cards. HiTech Global offers wide range of add-on FMC and FMC+ modules as shown on http://www.hitechglobal.com/Accessories/FMC_Modules.htm .

Figure (9) illustrates carrier card FMC+ connector's grid labeling

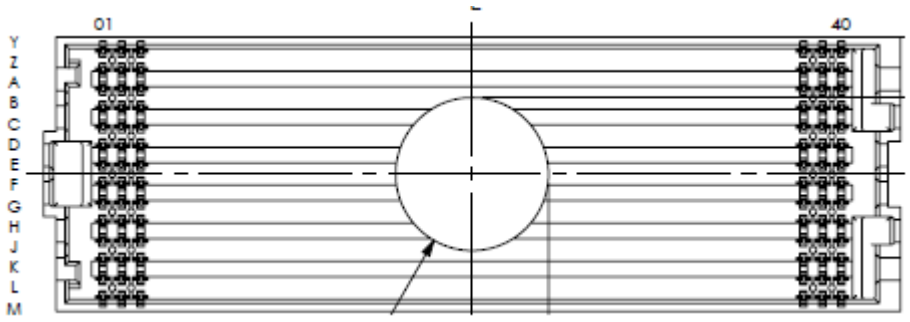
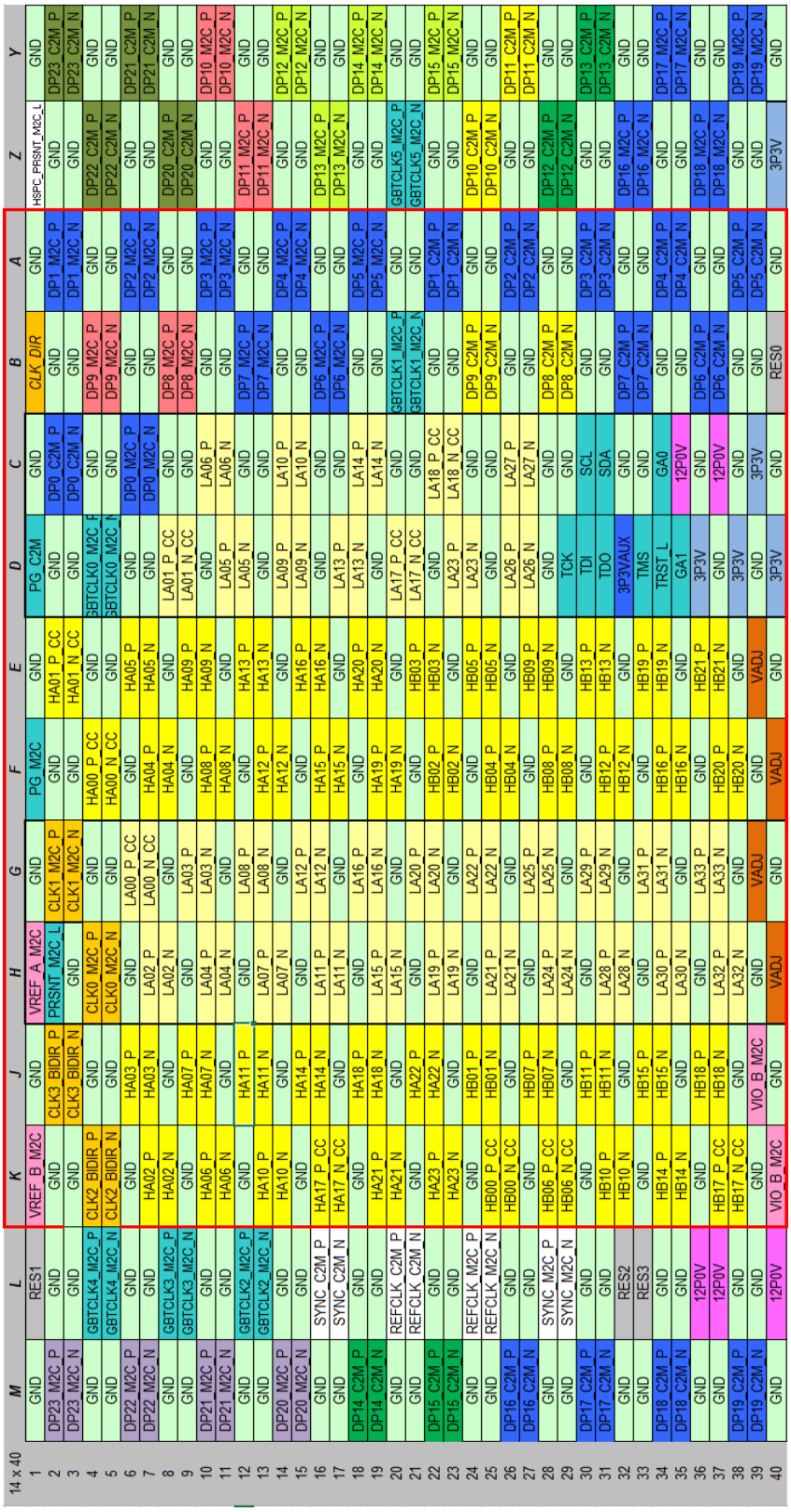


Figure (9): HSPC (Vita57.4) Carrier Card Connector Grid Labeling



14 x 40	M	L	K	J	H	G	F	E	D	C	B	A	Z	Y
1	GND	RES1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND	H5PC_PRSNT_M2C_L	GND
2	DP23_M2C_P	GND	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P	GND	DP23_C2M_P
3	DP23_M2C_N	GND	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N	GND	DP23_C2M_N
4	GND	GBTCLK4_M2C_P	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND	DP22_C2M_P	GND
5	GND	GBTCLK4_M2C_N	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND	DP22_C2M_N	GND
6	DP22_M2C_P	GND	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P	GND	DP21_C2M_P
7	DP22_M2C_N	GND	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N	GND	DP21_C2M_N
8	GND	GBTCLK3_M2C_P	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND	DP20_C2M_P	GND
9	GND	GBTCLK3_M2C_N	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND	DP20_C2M_N	GND
10	DP21_M2C_P	GND	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P	GND	DP10_M2C_P
11	DP21_M2C_N	GND	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N	GND	DP10_M2C_N
12	GND	GBTCLK2_M2C_P	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND	DP11_M2C_P	GND
13	GND	GBTCLK2_M2C_N	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND	DP11_M2C_N	GND
14	DP20_M2C_P	GND	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P	GND	DP12_M2C_P
15	DP20_M2C_N	GND	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N	GND	DP12_M2C_N
16	GND	SYNC_C2M_P	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND	DP13_M2C_P	GND
17	GND	SYNC_C2M_N	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND	DP13_M2C_N	GND
18	DP14_C2M_P	GND	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P	GND	DP14_M2C_P
19	DP14_C2M_N	GND	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N	GND	DP14_M2C_N
20	GND	REFCLK_C2M_P	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND	GBTCLK5_M2C_P	GND
21	GND	REFCLK_C2M_N	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND	GBTCLK5_M2C_N	GND
22	DP15_C2M_P	GND	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P	GND	DP15_M2C_P
23	DP15_C2M_N	GND	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N	GND	DP15_M2C_N
24	GND	REFCLK_M2C_P	GND	HB01_P	GND	LA22_P	GND	HB04_P	LA23_N	GND	DP9_C2M_P	GND	DP10_C2M_P	GND
25	GND	REFCLK_M2C_N	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_N	HB05_N	GND	GND	DP9_C2M_N	GND	DP10_C2M_N	GND
26	DP16_C2M_P	GND	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P	GND	DP11_C2M_P
27	DP16_C2M_N	GND	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N	GND	DP11_C2M_N
28	GND	SYNC_M2C_P	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND	DP12_C2M_P	GND
29	GND	SYNC_M2C_N	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND	DP12_C2M_N	GND
30	DP17_C2M_P	GND	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P	GND	DP13_C2M_P
31	DP17_C2M_N	GND	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N	GND	DP13_C2M_N
32	GND	RES2	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND	DP16_M2C_P	GND
33	GND	RES3	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND	DP16_M2C_N	GND
34	DP18_C2M_P	GND	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P	GND	DP17_M2C_P
35	DP18_C2M_N	GND	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N	GND	DP17_M2C_N
36	GND	12P0V	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND	DP18_M2C_P	GND
37	GND	12P0V	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND	DP18_M2C_N	GND
38	DP19_C2M_P	GND	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P	GND	DP19_M2C_P
39	DP19_C2M_N	GND	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N	GND	DP19_M2C_N
40	GND	12P0V	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND	3P3V	GND

Table (8): Vita57.4 FMC+ Pin Assignment

Table (9) illustrates FPGA pin assignment for the PL side FMC+ interface.

FMC+ Signal Name	FPGA Pin Number
FMC_PL_CLK[0]_M2C_	AP21
FMC_PL_CLK[0]_M2C_	AN21
FMC_PL_DP[0]_C2M_N	E34
FMC_PL_DP[0]_C2M_P	E33
FMC_PL_DP[0]_M2C_N	F37
FMC_PL_DP[0]_M2C_P	F36
FMC_PL_DP[1]_C2M_N	H32
FMC_PL_DP[1]_C2M_P	H31
FMC_PL_DP[1]_M2C_N	J39
FMC_PL_DP[1]_M2C_P	J38
FMC_PL_DP[2]_C2M_N	G34
FMC_PL_DP[2]_C2M_P	G33
FMC_PL_DP[2]_M2C_N	H37
FMC_PL_DP[2]_M2C_P	H36
FMC_PL_DP[3]_C2M_N	F32
FMC_PL_DP[3]_C2M_P	F31
FMC_PL_DP[3]_M2C_N	G39
FMC_PL_DP[3]_M2C_P	G38
FMC_PL_DP[4]_C2M_N	C34
FMC_PL_DP[4]_C2M_P	C33
FMC_PL_DP[4]_M2C_N	D37
FMC_PL_DP[4]_M2C_P	D36
FMC_PL_DP[5]_C2M_N	A34
FMC_PL_DP[5]_C2M_P	A33
FMC_PL_DP[5]_M2C_N	B37
FMC_PL_DP[5]_M2C_P	B36
FMC_PL_DP[6]_C2M_N	B32
FMC_PL_DP[6]_C2M_P	B31
FMC_PL_DP[6]_M2C_N	C39
FMC_PL_DP[6]_M2C_P	C38
FMC_PL_DP[7]_C2M_N	D32
FMC_PL_DP[7]_C2M_P	D31
FMC_PL_DP[7]_M2C_N	E39
FMC_PL_DP[7]_M2C_P	E38
FMC_PL_GBTCLK[0]_M	T32
FMC_PL_GBTCLK[0]_M	T31
FMC_PL_GBTCLK[1]_M	M32
FMC_PL_GBTCLK[1]_M	M31

FMC_PL_LA[0]_CC_N	AR18
FMC_PL_LA[0]_CC_P	AP18
FMC_PL_LA[1]_CC_N	AN20
FMC_PL_LA[1]_CC_P	AM20
FMC_PL_LA[2]_N	AT22
FMC_PL_LA[2]_P	AR22
FMC_PL_LA[3]_N	AT21
FMC_PL_LA[3]_P	AR21
FMC_PL_LA[4]_N	AW21
FMC_PL_LA[4]_P	AV21
FMC_PL_LA[5]_N	AK21
FMC_PL_LA[5]_P	AK22
FMC_PL_LA[6]_N	AV18
FMC_PL_LA[6]_P	AU18
FMC_PL_LA[7]_N	AL20
FMC_PL_LA[7]_P	AL21
FMC_PL_LA[8]_N	AM22
FMC_PL_LA[8]_P	AL22
FMC_PL_LA[9]_N	AT19
FMC_PL_LA[9]_P	AR19
FMC_PL_LA[10]_N	AV17
FMC_PL_LA[10]_P	AU17
FMC_PL_LA[11]_N	AM19
FMC_PL_LA[11]_P	AL19
FMC_PL_LA[12]_N	AH20
FMC_PL_LA[12]_P	AG20
FMC_PL_LA[13]_N	AJ19
FMC_PL_LA[13]_P	AJ20
FMC_PL_LA[14]_N	AK18
FMC_PL_LA[14]_P	AJ18
FMC_PL_LA[15]_N	AT17
FMC_PL_LA[15]_P	AR17
FMC_PL_LA[16]_N	AH18
FMC_PL_LA[16]_P	AG18
FMC_PL_LA[17]_CC_N	AR8
FMC_PL_LA[17]_CC_P	AP8
FMC_PL_LA[18]_CC_N	AR9
FMC_PL_LA[18]_CC_P	AP9
FMC_PL_LA[19]_N	AV12
FMC_PL_LA[19]_P	AU12
FMC_PL_LA[20]_N	AW8

FMC_PL_LA[20]_P	AW9
FMC_PL_LA[21]_N	AN13
FMC_PL_LA[21]_P	AM13
FMC_PL_LA[22]_N	AU10
FMC_PL_LA[22]_P	AT10
FMC_PL_LA[23]_N	AW11
FMC_PL_LA[23]_P	AV11
FMC_PL_LA[24]_N	AN7
FMC_PL_LA[24]_P	AN8
FMC_PL_LA[25]_N	AM14
FMC_PL_LA[25]_P	AL14
FMC_PL_LA[26]_N	AN12
FMC_PL_LA[26]_P	AM12
FMC_PL_LA[27]_N	AR11
FMC_PL_LA[27]_P	AR12
FMC_PL_LA[28]_N	AM10
FMC_PL_LA[28]_P	AL10
FMC_PL_LA[29]_N	AK14
FMC_PL_LA[29]_P	AJ14
FMC_PL_LA[30]_N	AH12
FMC_PL_LA[30]_P	AG12
FMC_PL_LA[31]_N	AK12
FMC_PL_LA[31]_P	AJ12
FMC_PL_LA[32]_N	AL7
FMC_PL_LA[32]_P	AL8
FMC_PL_LA[33]_N	AM9
FMC_PL_LA[33]_P	AL9
FMC_PL_PG_M2C	A10
FMC_PL_PRSNT_M2C_L	C10
FMC_PL_REFCLK_M2C_	AP11
FMC_PL_REFCLK_M2C_	AN11
FMC_PL_SYNC_C2M_N	AW10
FMC_PL_SYNC_C2M_P	AV10
FMC_PL_SYNC_M2C_N	AP10
FMC_PL_SYNC_M2C_P	AN10
HSPC_PL_PRSNT_M2C_	B10

Table (9): FPGA Mezzanine Connector (FMC+) Pin Assignment

7.1) FMC+ Clock

Clocks for the FMC+ I/Os are generated by the onboard Si5341 programmable clock generator through OUT2 (FMC_PL_REFCLK_C2M) , OUT3 (GTY_131_REFCLK) and OUT4 (GTY_130_REFCLK) ports as shown by figure (5) and table (3).

7.2) FMC VADJ

V_Adjust carries an adjustable voltage level power from the FPGA carrier board to the I/O Mezzanine modules.

As illustrated by figure (10) V_Adjust for the FMC+ is controlled by proper setting value of the **"R192"** resistor near the LTM4644 power module (U24). The default voltage value is set for I/O voltage level of 1.8V (maximum supported by the FPGA device)

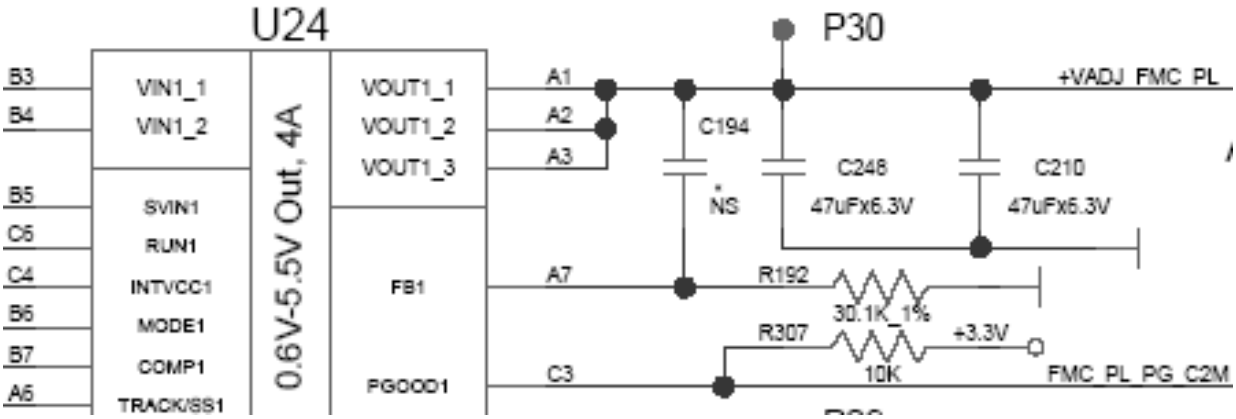


Figure (10): FMC+/FMC VADJ Configurations

Different output voltages can be generated by using the following formula for the configuration resistor (R192)

Rfb= (0.6V) (60.4K) / (Vout – 0.6V)

Table (10) provides required resistor values for different standard voltage levels.

V_{OUT} (V)	0.6	1.0	1.2	1.5	1.8
R_{FB} (kΩ)	OPEN	90.9	60.4	40.2	30.1

Table (10): RFB Resistor Table vs Various Output Voltages

8.0) ADC and DAC Ports

The HTG-ZRF platform provides access to eight 12-bit ADC (4GSPS) and eight 14-bit DAC (6.4GSPS) ports through sixteen SSMC connectors. The ADC and DAC ports are supported through high-performance front panel Mini Circuits TCM1-83X+ micro Rf connectors (with bandwidth from 10 to 8000 MHz).

Table (11) and (12) illustrate FPGA pin assignments for the ADC and DAC interface.

ADC Signal Name	FPGA Pin Number	Connector Number / Source
ADC_224_REFCLK_N	AF4	U67 Clock Fanout (Q0-N)
ADC_224_REFCLK_P	AF5	U67 Clock Fanout (Q0-P)
ADC_225_REFCLK_N	AD4	U67 Clock Fanout (Q1-N)
ADC_225_REFCLK_P	AD5	U67 Clock Fanout (Q1-P)
ADC_226_REFCLK_N	AB4	U67 Clock Fanout (Q2-N)
ADC_226_REFCLK_P	AB5	U67 Clock Fanout (Q2-P)
ADC_227_REFCLK_N	Y4	U67 Clock Fanout (Q3-N)
ADC_227_REFCLK_P	Y5	U67 Clock Fanout (Q3-P)
ADC_IN01_224_N	AP1	J20 SSMC / Rf Transformer
ADC_IN01_224_P	AP2	J20 SSMC / Rf Transformer
ADC_IN01_225_N	AK1	J19 SSMC / Rf Transformer
ADC_IN01_225_P	AK2	J19 SSMC / Rf Transformer
ADC_IN01_226_N	AF1	J18 SSMC / Rf Transformer
ADC_IN01_226_P	AF2	J18 SSMC / Rf Transformer
ADC_IN01_227_N	AB1	J17 SSMC / Rf Transformer
ADC_IN01_227_P	AB2	J17 SSMC / Rf Transformer
ADC_IN23_224_N	AM1	J10 SSMC / Rf Transformer
ADC_IN23_224_P	AM2	J10 SSMC / Rf Transformer
ADC_IN23_225_N	AH1	J9 SSMC / Rf Transformer
ADC_IN23_225_P	AH2	J9 SSMC / Rf Transformer
ADC_IN23_226_N	AD1	J8 SSMC / Rf Transformer
ADC_IN23_226_P	AD2	J8 SSMC / Rf Transformer
ADC_IN23_227_N	Y1	J7 SSMC / Rf Transformer
ADC_IN23_227_P	Y2	J7 SSMC / Rf Transformer

Table (11): ADC Interface Pin Assignment

DAC Signal Name	FPGA Pin Number	Connector Number / Source
DAC_228_REFCLK_N	R4	U66 Clock Fanout (Q1-N)
DAC_228_REFCLK_P	R5	U66 Clock Fanout (Q1-P)
DAC_228_SYSREF_N	U4	U66 Clock Fanout (Q0-N)
DAC_228_SYSREF_P	U5	U66 Clock Fanout (Q0-P)
DAC_229_REFCLK_N	N4	U66 Clock Fanout (Q2-N)

DAC_229_REFCLK_P	N5	U66 Clock Fanout (Q2-P)
DAC_VOUT0_228_N	U1	J16 SSMC / Rf Transformer
DAC_VOUT0_228_P	U2	J16 SSMC / Rf Transformer
DAC_VOUT0_229_N	J1	J14 SSMC / Rf Transformer
DAC_VOUT0_229_P	J2	J14 SSMC / Rf Transformer
DAC_VOUT1_228_N	R1	J6 SSMC / Rf Transformer
DAC_VOUT1_228_P	R2	J6 SSMC / Rf Transformer
DAC_VOUT1_229_N	G1	J4 SSMC / Rf Transformer
DAC_VOUT1_229_P	G2	J4 SSMC / Rf Transformer
DAC_VOUT2_228_N	N1	J15 SSMC / Rf Transformer
DAC_VOUT2_228_P	N2	J15 SSMC / Rf Transformer
DAC_VOUT2_229_N	E1	J13 SSMC / Rf Transformer
DAC_VOUT2_229_P	E2	J13 SSMC / Rf Transformer
DAC_VOUT3_228_N	L1	J5 SSMC / Rf Transformer
DAC_VOUT3_228_P	L2	J5 SSMC / Rf Transformer
DAC_VOUT3_229_N	C1	J3 SSMC / Rf Transformer
DAC_VOUT3_229_P	C2	J3 SSMC / Rf Transformer

Table (12): DAC Interface Pin Assignment

8.1) ADC/DAC Clock

U69 (Vectron part number:VCC6-LAB-122M880000) provides input clock to U68 (TI part number LMX2592 or LMX2594) clock generator and has start-up frequency of 122.88 MHz The LMX25xx should be programmed using Texas Instruments' TICS PRO software (http://www.ti.com/tool/TICSPRO-SW)

Bypassing the U69 oscillator, the J2 and J11 SMCC connectors (mounted near the front panel) can also be used for bringing external clocks to the LMX25xx clock generator. Enabling the external clock requires removal of the C685/C687 and installation of the C684/686 0.1uF capacitors. The provided board's assembly file should be used for locating these configuration capacitors.

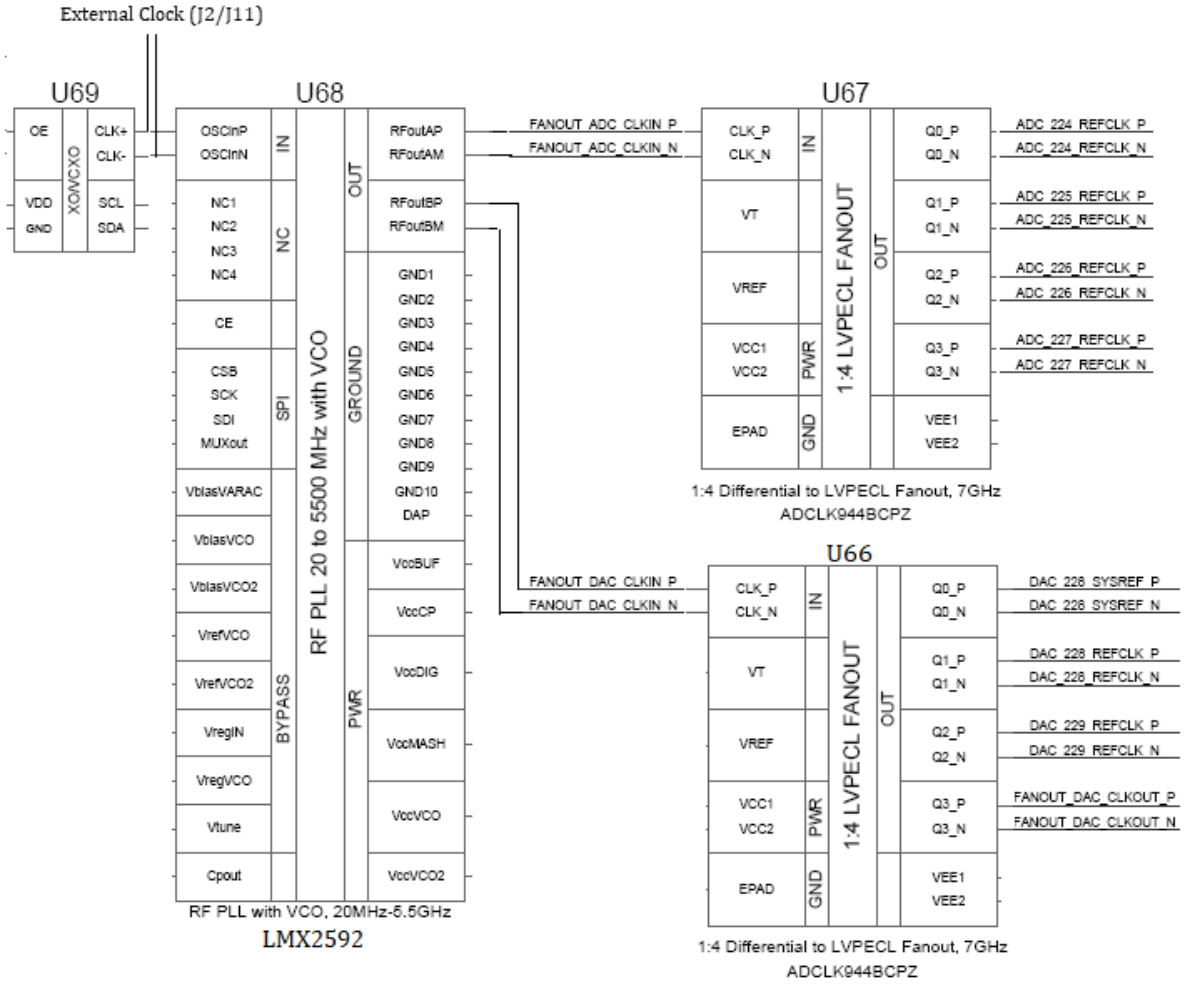


Figure (11): ADC/DAC Clock Diagram

9.0) USB To UART Bridges

The HTG-ZRF8 platform provides access to two UART ports for the PL and PS sides through two peripheral USB connectors (J1 and J12). These ports are supported by the Silicon labs CP2103 USB to UART controller chips (U70 and U71).

The CP2103 is a highly-integrated USB-to-UART Bridge Controller providing a simple solution for updating RS-232/RS-485 designs to USB using a minimum of components and PCB space. The CP2103 includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, EEPROM, and asynchronous serial data bus (UART) with full modem control signals in a compact 5x5 mm QFN-28 package (sometimes called "MLF" or "MLP"). No other external USB components are required.
The on-chip EEPROM may be used to customize the USB Vendor ID, Product ID, Product Description String, Power Descriptor, Device Release Number, and Device Serial Number as desired for OEM applications. The EEPROM is programmed on-board via the USB, allowing the programming step to be easily integrated into the product manufacturing and testing process.
Royalty-free Virtual COM Port (VCP) device drivers provided by Silicon Laboratories allow a CP2103-based product to appear as a COM port to PC applications. The CP2103 UART interface implements all RS-232/RS-485 signals, including control and handshaking signals; so, existing system firmware does not need to be

modified. The device also features up to four GPIO signals that can be user-defined for status and control information. Support for I/O interface voltages down to 1.8 V is provided via a VIO pin. In many existing RS-232 designs, all that is required to update the design from RS-232 to USB is to replace the RS-232 level-translator with the CP2103.

Driver for the CP2103 device is available at following site for download or upgrade :

https://www.silabs.com/products/mcu/Pages/USBtoUARTBridgeVCPDrivers.aspx

Table (13) illustrates FPGA pin assignment for the USB-TO-UART interfaces.

FPGA Signal Name	FPGA Pin Number
UART_PL_CTS	AU7
UART_PL_GPIO0	AR6
UART_PL_GPIO1	AU5
UART_PL_RST_N	AT7
UART_PL_RTS	AV7
UART_PL_RXD	AU8
UART_PL_SUSPEND_N	AR7
UART_PL_TXD	AV8
USB_PL_PERI_PWR	AT6
MIO18_UART0_RXD	Y27
MIO19_UART0_TXD	W28

Table (13): USB To UART FPGA Pin Assignment

10.0) ARM Trace Port

The HTG-ZRF8 provides access to one standard ARM Trace/Debug port (38-pin Mictor connector). The pin out follows the single target connector pinout specification as defined in the ARM "Architecture Specification.

Table (14) illustrates FPGA pin assignment for the ARM Trace/Debug port (J22)

FPGA Signal Name	FPGA Pin Number
TRACECLK	AL16
TRACECTL	AP16
TRACEDATA0	AR16
TRACEDATA1	AN17
TRACEDATA10	AR13
TRACEDATA11	AU13
TRACEDATA12	AK16
TRACEDATA13	AL15
TRACEDATA14	AH17
TRACEDATA15	AJ16
TRACEDATA2	AM17
TRACEDATA3	AF16

TRACEDATA4	AP14
TRACEDATA5	AR14
TRACEDATA6	AP13
TRACEDATA7	AT15
TRACEDATA8	AN16
TRACEDATA9	AK17
TRACEDBGACK	AU14
TRACEDBGRQ	AJ15
TRACEEXTTRIG	AU15
TRACERTCK	AL17
TRACESRST_B	AH15
TRACETCK	AG17
TRACETDI	AT16
TRACETDO	AH16
TRACETMS	AF17
TRACETRST_B	AP15

Table (14): Trace/Debug Port's FPGA Pin Assignment

11.0) SDIO Interface

The HTG-ZRF8 supports a secure digital input/output (SDIO) interface providing access to general purpose non-volatile SDIO memory cards and peripherals. The SDIO signals are connected to the PS bank 501 of the onboard Zynq UltraScale+ FPGA. A SD 2.0-compliant voltage level-translator (SN74AVCA406EZQS) is present between the onboard Zynq UltraScale+ RFSoC FPGA and the SD card connector (J35).

Table (15) illustrates FPGA pin assignment for the SDIO Interface.

FPGA Signal Name	FPGA Pin Number
MIO39_SDIO_SEL	B28
MIO40_SDIO_DIR_CMD	D26
MIO41_SDIO_DIR_DAT	C28
MIO42_SDIO_DIR_DAT	E28
MIO44_SDIO_PROTECT	F27
MIO45_SDIO_DETECT	G27
MIO46_SDIO_DAT0	A29
MIO47_SDIO_DAT1	C29
MIO48_SDIO_DAT2	D29
MIO49_SDIO_DAT3	B29
MIO50_SDIO_CMD	F29
MIO51_SDIO_CLK	E29

Table (15): SDIO Port's FPGA Pin Assignment

12.0) 10/100/1000 Mbps Ethernet

The HTG-ZRF8 platform provides access to one 10/100/1000 Mbps Ethernet port (J30) supported by Texas Instruments DP83867IRPAP PHY chip connected to the processor's I/Os of the FPGA.

The DP83867 device is a fully featured Physical Layer transceiver with integrated PMD sublayers to support 10BASE-Te, 100BASE-TX and 1000BASE-T Ethernet protocols. This device interfaces directly to the MAC layer through the IEEE 802.3 Standard Media Independent Interface (MII), the IEEE 802.3 Gigabit Media Independent Interface (GMII) or Reduced GMII (RGMII). The DP83867 provides precision clock synchronization, including a synchronous Ethernet clock output. It has low latency and provides IEEE 1588 Start of Frame Detection.

Table (16) illustrates FPGA pin assignment for the Ethernet interface.

FPGA Signal Name	FPGA Pin Number
MIO64_ETH_TX_CLK	K27
MIO65_ETH_TX_D0	L27
MIO66_ETH_TX_D1	N27
MIO67_ETH_TX_D2	J28
MIO68_ETH_TX_D3	H29
MIO69_ETH_TX_CTRL	M27
MIO70_ETH_RX_CLK	K28
MIO71_ETH_RX_D0	H28
MIO72_ETH_RX_D1	J29
MIO73_ETH_RX_D2	K29
MIO74_ETH_RX_D3	M28
MIO75_ETH_RX_CTRL	N28
MIO76_ETH_MDC	M29
MIO77_ETH_MDIO	L29

Table (16): Ethernet Port's FPGA Pin Assignment

Status LEDs are mounted on the board with the following functions:

LED_2 (D34): By default, this pin indicates receive or transmit activity. Additional functionality is configurable via LEDCR1[11:8] register bits of the PHY device.

LED_1 (D37): By default, this pin indicates that 1000BASE-T link is established. Additional functionality is configurable via LEDCR1[7:4] register bits of the PHY device.

LED_0 (D33): By default, this pin indicates that link is established. Additional functionality is configurable via LEDCR1[3:0] register bits of the PHY device.

13.0) Display Port

The HTG-ZRF8 platform provides access to one Display Port (J32) connected to the processor's single-ended and serial I/Os of the FPGA.

Reference clock for the Display Port serial transceivers is provided by the onboard SI5341 clock generator (U19).

Table (17) illustrates FPGA pin assignment for the Serial Port interface.

FPGA Signal Name	FPGA Pin Number
DP_TX0_N	AD37
DP_TX0_P	AD36
DP_TX1_N	AF37
DP_TX1_P	AF36
MIO27_DP_AUX_OUT	C25
MIO28_DP_HPD	F25
MIO29_DP_OE	B25
MIO30_DP_AUX_IN	D25

Table (17): Display Port's FPGA Pin Assignment

14.0) USB 2.0/3.0

The HTG-ZRF8 platform provides access to a USB 2.0 through Microchip USB3320 chip and USB 3.0 through GTR serial transceivers of the FPGA's processor side.

The Microchip USB3320 is a USB 2.0 Transceiver that provides a configurable physical layer (PHY). The USB3320 meets all of the electrical requirements to be used as a Hi-Speed USB Host, Device, or an On-the-Go (OTG) transceiver. In addition to the supporting USB signaling, the USB3320 also provides USB UART mode and USB Audio mode. USB3320 uses the industry standard UTMI+ Low Pin Interface (ULPI) to connect the USB Transceiver to the Link.

Reference clock for the USB3.0 serial transceivers is provided by the onboard SI5341 clock generator (U19).

Table (18) illustrates FPGA pin assignment for the USB interface.

FPGA Signal Name	FPGA Pin Number
MIO52_USB_CLK	N26
MIO53_USB_DIR	L25
MIO54_USB_D2	M26
MIO55_USB_NXT	J25
MIO56_USB_D0	L26
MIO57_USB_D1	H25
MIO58_USB_STP	H26
MIO59_USB_D3	H27

MIO6_USER_SW1	W26
MIO60_USB_D4	J26
MIO61_USB_D5	G28
MIO62_USB_D6	K26
MIO63_USB_D7	G29
USB3_RX_N	AG39
USB3_RX_P	AG38
USB3_TX_N	AH37
USB3_TX_P	AH36

Table (18): USB Port's FPGA Pin Assignment

15.0) SATA

The HTG-ZRF8 platform provides access to one Serial ATA port (J33). The port can be used for standard SATA storage access applications or board-to-board connection.

Reference clock for the SATA serial transceivers is provided by the onboard SI5341 clock generator (U19).

Table (19) illustrates FPGA pin assignment for the SATA interface.

FPGA Signal Name	FPGA Pin Number
SATA_RX_N	AJ39
SATA_RX_P	AJ38
SATA_TX_N	AK37
SATA_TX_P	AK36

Table (19): SATA Port's FPGA Pin Assignment

16.0) 1-PPS Interface

The HTG-ZRF8 platform provides access to one 1-PPS interface through one MCX connector, one Comparator, one 8-bit ADC (3MSPS), and one Schmitt-Trigger Buffer.

Table (20) illustrates FPGA pin assignment for the 1-PPS interface.

FPGA Signal Name	FPGA Pin Number
IRIG_ADC_CS_N	B7
IRIG_ADC_SCLK	D8
IRIG_ADC_SDO	A7
IRIG_COMP_OUT	B9
IRIG_TRIG_OUT	B8

Table (20): 1-PPS Port's FPGA Pin Assignment

17.0) LEDs, XDAC, User I/O Headers & Pushbuttons

The HTG-ZRF8 platform provides user LEDs, XDAC headers, user I/O headers, and Push Buttons.

Table (21) illustrates FPGA pin assignment and reference designators for each interface.

FPGA Signal Name	FPGA Pin Number	Reference Designator
PL_USER_LED1_G	A6	D10 GREEN LED
PL_USER_LED2_G	C6	D9 GREEN LED
PL_USER_LED3_R	D6	D8 RED LED
PL_USER_LED4_R	E6	D7 RED LED
PL_USER_PB	AT5	PB3 PUSH BUTTON
PL_USER_SW1	D20	S1 SWITCH – KEY#1
PL_USER_SW2	A25	S1 SWITCH – KEY#2
PL_USER_SW3	B23	S1 SWITCH – KEY#3
PL_USER_SW4	D19	S1 SWITCH – KEY#4
MIO13_USER_LED1_G	R28	D6 GREEN LED
MIO20_USER_LED2_G	V28	D5 GREEN LED
MIO21_USER_LED3_R	V29	D4 RED LED
MIO22_USER_LED4_R	Y28	D3 RED LED
MIO23_USER_PB	U29	PB4 PUSH BUTTON
MIO6_USER_SW1	W26	S1 SWITCH – KEY#5
MIO24_USER_SW2	Y29	S1 SWITCH – KEY#6
MIO25_USER_SW3	W29	S1 SWITCH – KEY#7
MIO43_USER_SW4	D28	S1 SWITCH – KEY#8
PS_SRST_N	AB28	PB1 PUSH BUTTON
PS_PROG_N	AA27	PB2 PUSH BUTTON
XDAC_DXN	AA16	J27 PIN #1
XDAC_DXP	AA17	J27 PIN #2
XDAC_VN_F	Y16	J24 PIN #1
XDAC_VP_F	W17	J24 PIN #2
FAN_PWM	AW13	J26 FAN HEADER

Table (21): User Interface FPGA Pin Assignment

18.0) IP Protection

The HTG-ZRF8 platform provides access to a special circuit (U7) for protection of intellectual properties loaded to the FPGA (pin # A9) by using Maxim DS2432 chip.

The DS2432 combines 1024 bits of EEPROM, a 64-bit secret, an 8-byte register/control page with up to five user read/write bytes, a 512-bit SHA-1 engine, and a fully-featured 1-Wire interface in a single chip. Each DS2432 has its own 64-bit ROM registration number that is factory lasered into the chip to provide

a guaranteed unique identity for absolute traceability. Data is transferred serially via the 1-Wire protocol, which requires only a single data lead and a ground return. The DS2432 has an additional memory area called the scratchpad that acts as a buffer when writing to the main memory, the register page or when installing a new secret. Data is first written to the scratchpad from where it can be read back. After the data has been verified, a copy scratchpad command will transfer the data to its final memory location, provided that the DS2432 receives a matching 160-Bit MAC. The computation of the MAC involves the secret and additional data stored in the DS2432 including the device's registration number. Only a new secret can be loaded without providing a MAC. The SHA-1 engine can also be activated to compute 160-bit message authentication codes (MAC) when reading a memory page or to compute a new secret, instead of loading it. Applications of the DS2432 include intellectual property security, after-market management of consumables, and tamper-proof data carriers.

Additional information is available at http://datasheets.maximintegrated.com/en/ds/DS2432.pdf

19.0) I2C Bus Switch

All I2C-controlled devices on the HTG-ZRF8 platform are controlled by the FPGA Logic or/and the processor signals and the I2C Bus Switch chip (U51) as shown by the below FPGA signals and figure (12)

I2C_RST_N_PL	FPGA Pin: D10
I2C_SCL_PL	FPGA Pin: E9
I2C_SDA_PL	FPGA Pin: E8
MIO14_I2C0_SCL	FPGA Pin: P29
MIO15_I2C0_SDA	FPGA Pin: U28
MIO16_I2C1_SCL	FPGA Pin: R29
MIO17_I2C1_SDA	FPGA Pin: T29

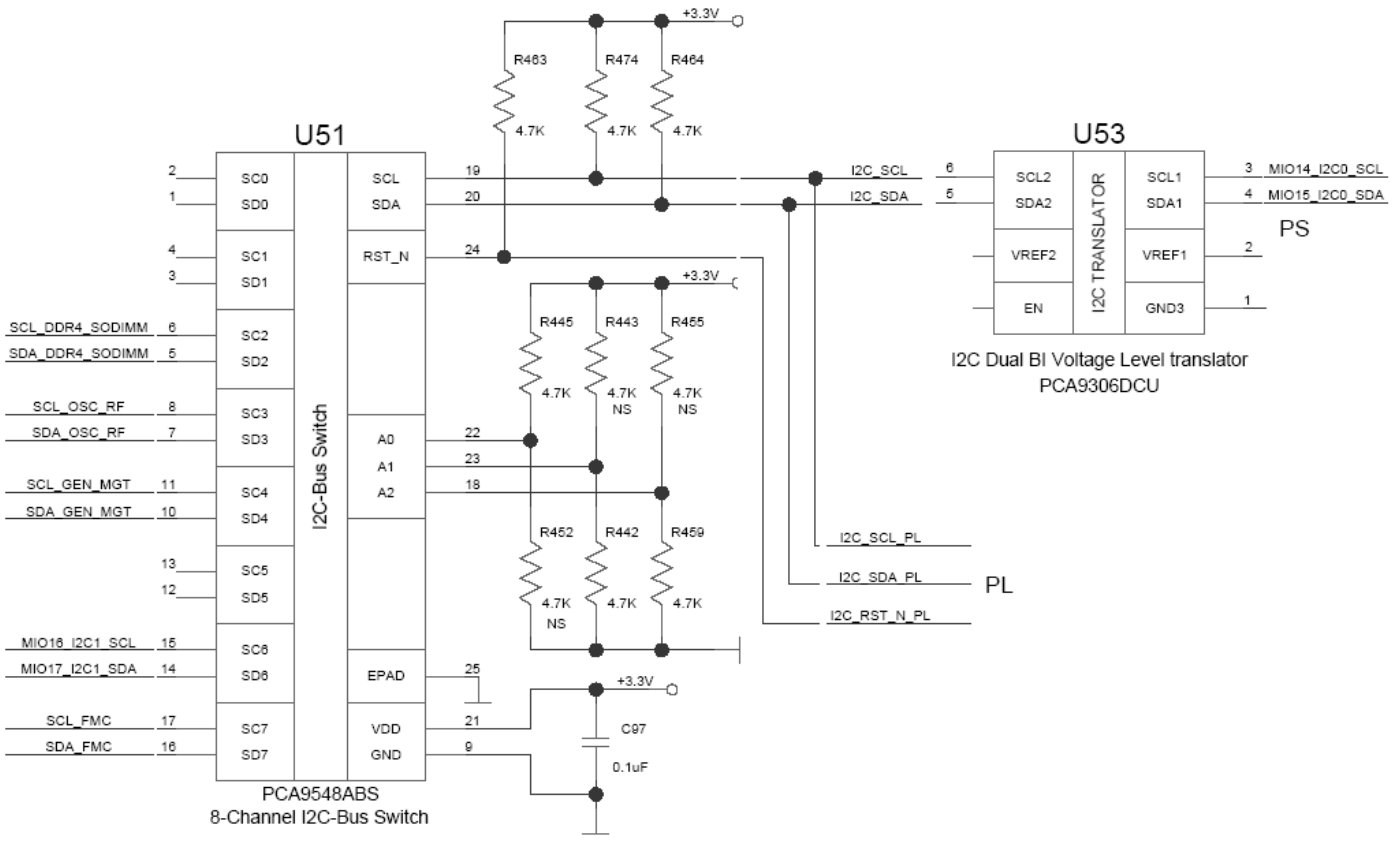


Figure (12): I2C Bus Switch

20.0) Configuration

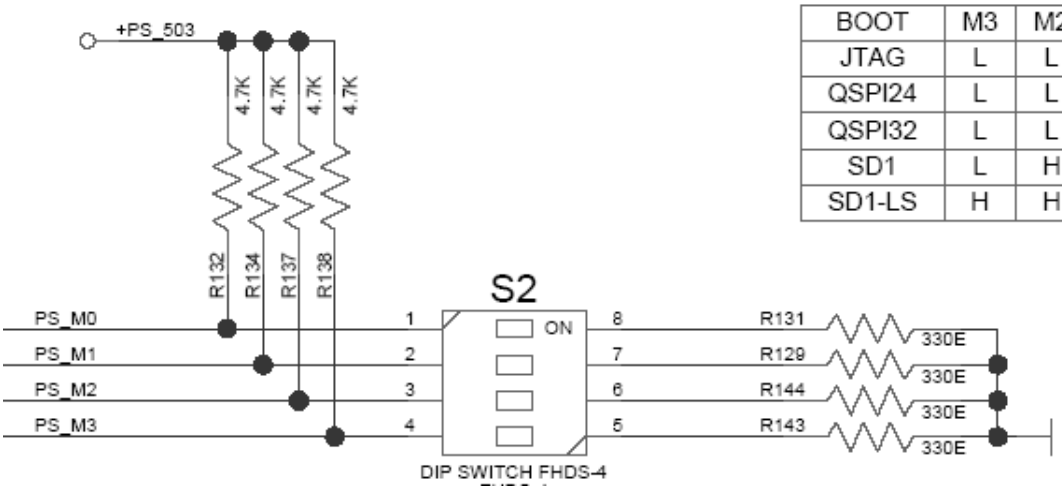
The HTG-ZRF8 can be configured using its Jtag, QSPI, or MicroSD port.

Quad-SPI

Booting from the dual Quad-SPI nonvolatile configuration memory is accomplished by storing a valid Zynq UltraScale+ MPSoC boot image (.MCS) into the Quad-SPI flash devices connected to the MIO Quad-SPI interface and setting the boot mode pins S2 [4:1] = QSFPI32 shown by the figure (22)

Micro SD

Booting from an SD card is accomplished by storing a valid Zynq UltraScale+ MPSoC boot image file onto a SD card (plugged into SD socket J35) connected to the MIO SD interface and setting the boot mode pins S2 [4:1] = SD as shown by the figure (13).



BOOT	M3	M2	M1	M0
JTAG	L	L	L	L
QSPI24	L	L	L	H
QSPI32	L	L	H	L
SD1	L	H	L	H
SD1-LS	H	H	H	L

Figure (13): Configuration Option