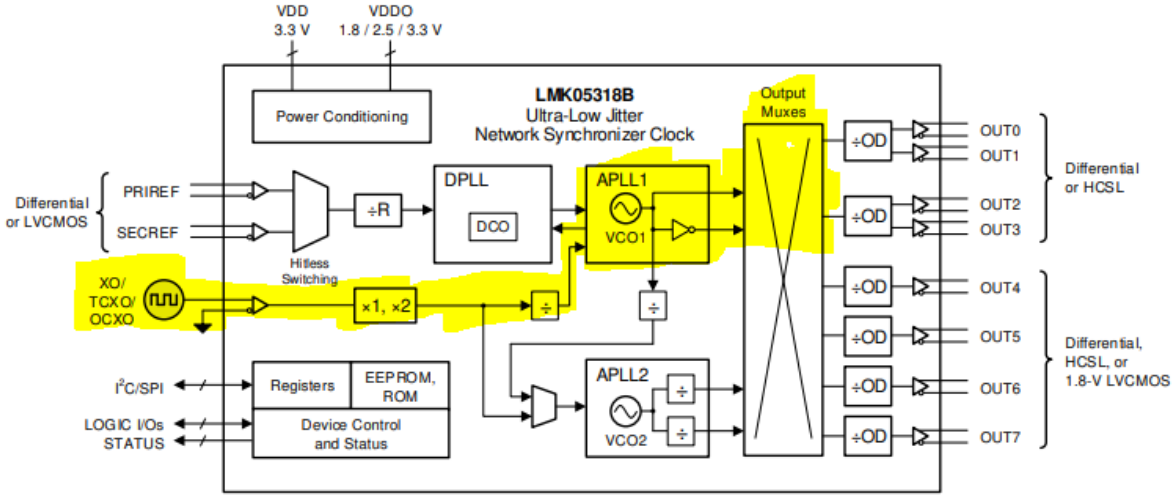
How the LMK05318B Operates

Here is an overview of how our LMK05318B works:

Here is a block diagram of the LMK05318B:



Simplified Block Diagram

No matter what output frequencies are required from the device, an APLL is required. The APLL locks to a XO input and the APLL output is fed to directly to the output muxes (as the highlighting shows above). Therefore, without the APLL enabled, there will be no output clocks.

Also, please note that the output frequencies will not be generated until the APLL has locked to the XO.

Now looking at the possible types of XO inputs, here are all the possibilities:

1. A XO, OCXO, or TCXO can be fed differentially or single-ended into the XO input pins.
    a. For a differential XO/OCXO/TCXO input the below terminations will be used based on which driver format is used as the output of the XO/OCXO/TCXO.

Driver	R_S (Ω)
LVDS	open
CML*	open
3.3-V LVPECL	150
2.5-V LVPECL	82
HCSL	50

*CML driver has 50-Ω pull-up

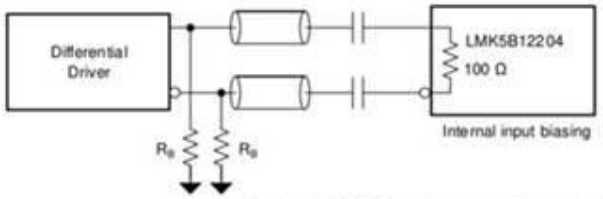
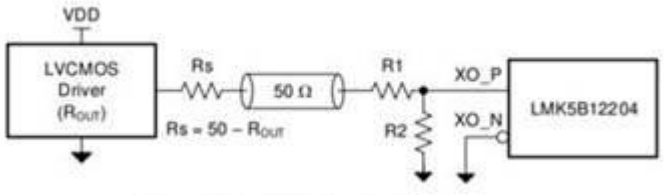


Figure 9-14. AC-Coupled Differential to Reference (PRIREF/SECREF) or XO Inputs

b. For a single-ended XO/OCXO/TCXO input the below terminations will be used based on the voltage swing coming from the output of the XO/OCXO/TCXO.



VDD	R1 (Ω)	R2 (Ω)
3.3 V	125	375
2.5 V	0	open
1.8 V	0	open

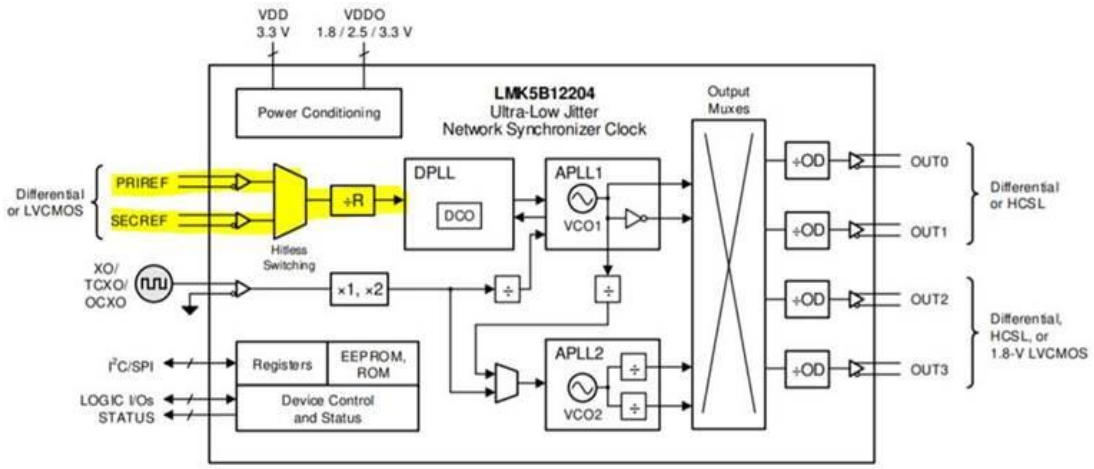
Figure 9-8. Single-Ended LVCMOS to XO Input (XO_P)

2. A single-ended LVCMOS clock (up to 2.5 V) can be fed into the **XO INPUT**.
    a. Please note this will be a different clock than the one being fed into the PRIREF or SECREF.

Also, here are some additional facts about the XO input that are important to note:

1. In DPLL mode, the XO frequency must have a non-integer relationship to the VCO1 frequency so APLL1 can operate in fractional mode (required for proper DPLL operation).
2. In APLL-only mode, the XO frequency can have either an integer or non-integer relationship to the VCO1 frequency.
3. **The phase noise performance of the clock being fed into the XO input will affect the output clocks phase noise performance (specifically at the 0 Hz to 1kHz range). This is why an XO/OCXO/TCXO is recommended to be used as the XO input as they typically have much better phase noise performance.**

Once you have the XO input and APLL properly configured based on the instructions above, you can have the additional ability to fed a reference clock to the PRIREF or SECREF input of the device (as shown in the highlighting below).



Simplified Block Diagram

The most important thing to note is that the reference clock will not affect the output clocks phase noise performance. Rather, the reference clock will affect the output clocks frequency accuracy (or stability).

Here are some additional facts about the reference inputs (PRIREF and SECREF):

1. The reference clocks are used as inputs to the DPLL internal to the device.
    a. The DPLL will lock to these reference inputs and configure the output clocks accuracy based on the accuracy of the reference clock.
        i. Therefore, the ppm error of the reference clock will determine the accuracy of the output clock coming from the LMK5B12204.