How to Build a Schematic for the LMK05318B

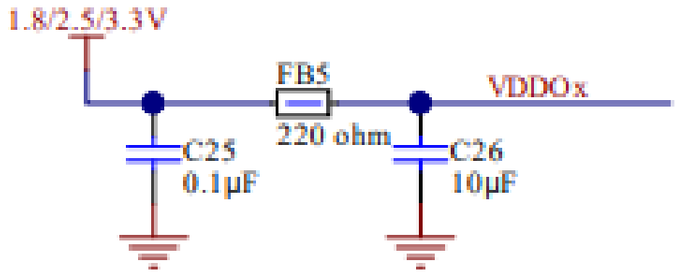
The recommended pin terminations for the LMK05318B schematic are as follows.

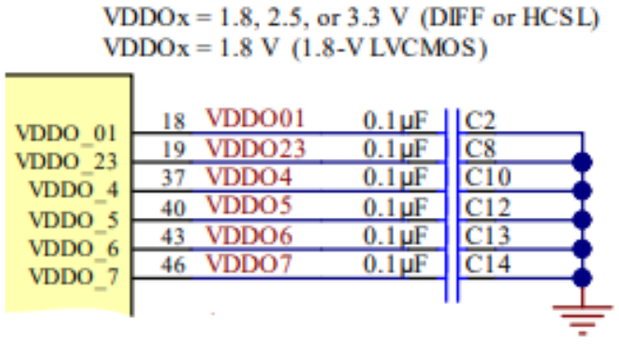
Notes:

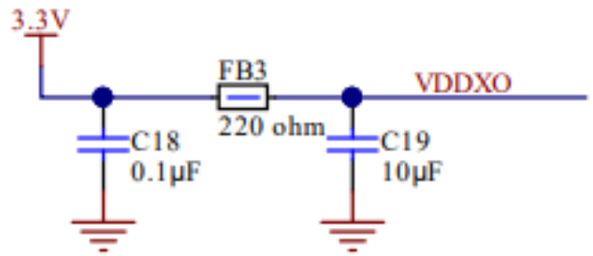
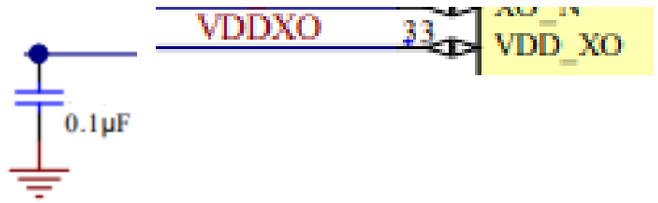
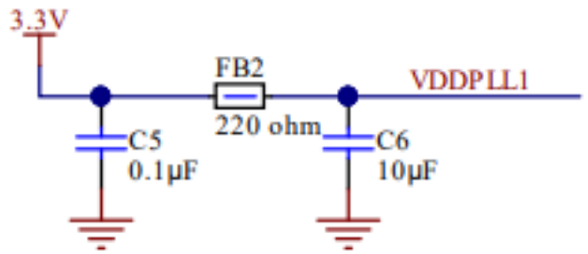
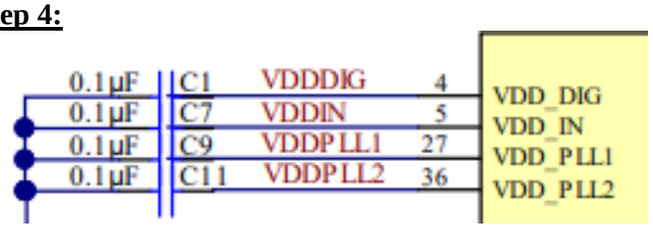
1. P = Power, G = Ground, I = Input, O = Output, I/O = Input or Output, A = Analog, S = Configuration.

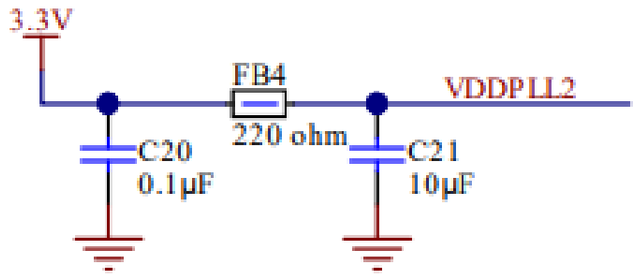
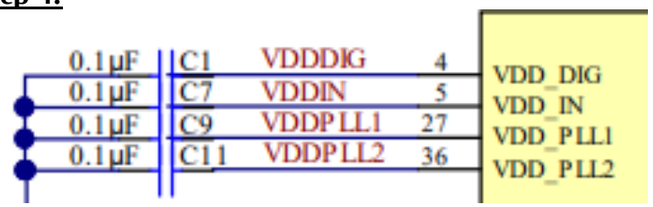
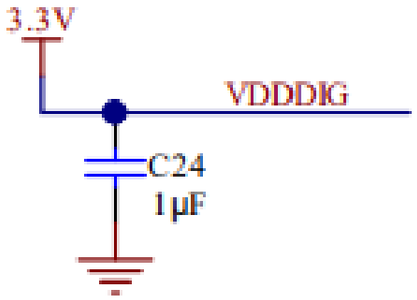
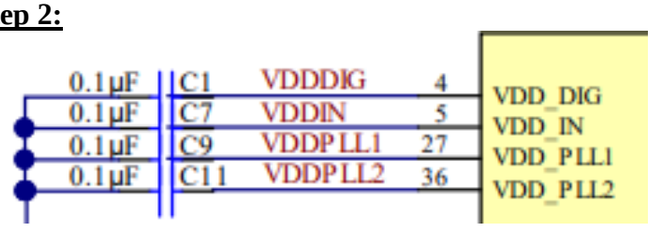
<table>
<tr><th colspan="2">PIN</th><th>TYPE</th><th>DESCRIPTION</th><th>PIN TERMINATION</th><th>TI Feedback</th></tr>
<tr><th>NAME</th><th>NO.</th><th></th><th></th><th></th><th></th></tr>
<tr><td colspan="6">POWER</td></tr>
<tr><td>VDDO_01</td><td>18</td><td>P</td><td rowspan="6">These pins power the outputs.

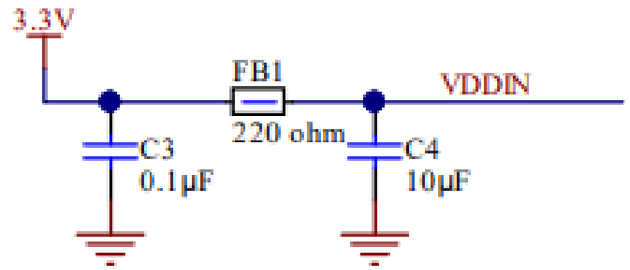
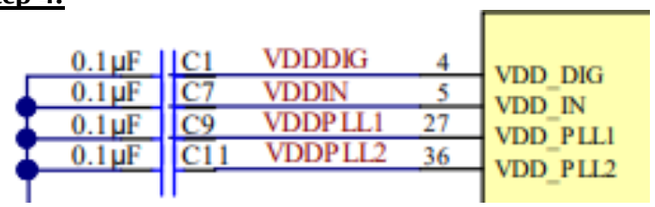
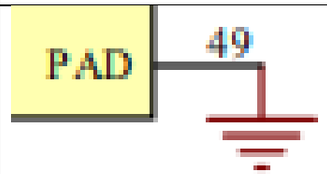
1. Place a 0.1 uF capacitor close to the supply
2. Place a ferrite bead (recommended 220 ohm) to reduce crosstalk
3. Place a 10 uF decoupling capacitor
4. Place a 0.1 uF decoupling capacitor close to each power pin.

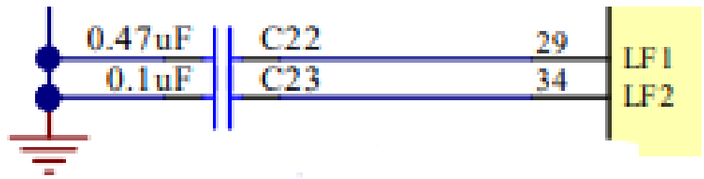
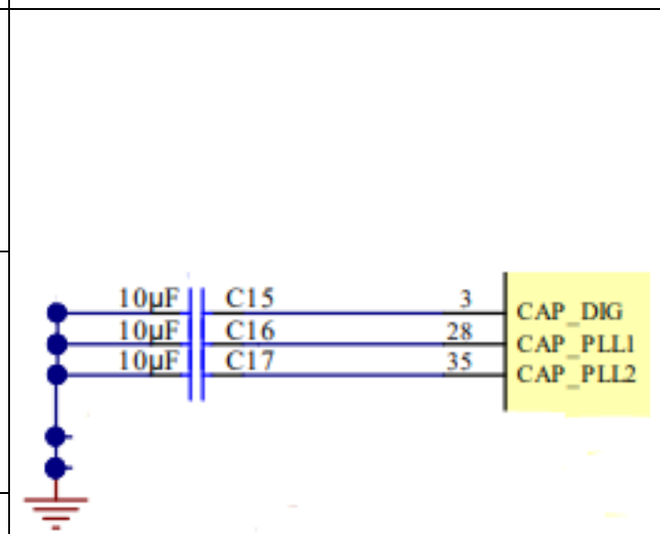
NOTE: Outputs with the same frequencies can share steps 1-3 above, but each pin requires its own 0.1 uF (step 4).</td><td rowspan="6"><u>Step 1-3:</u>
 

<u>Step 4:</u>
 
</td><td></td></tr>
<tr><td>VDDO_23</td><td>19</td><td>P</td><td></td></tr>
<tr><td>VDDO_4</td><td>37</td><td>P</td><td></td></tr>
<tr><td>VDDO_5</td><td>40</td><td>P</td><td></td></tr>
<tr><td>VDDO_6</td><td>43</td><td>P</td><td></td></tr>
<tr><td>VDDO_7</td><td>46</td><td>P</td><td></td></tr>
</table>

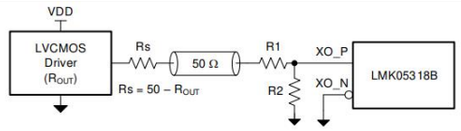
VDD_XO	33	P	Power supply for XO 1. Place a 0.1 uF capacitor close to the supply 2. Place a ferrite bead (recommended 220 ohm) to reduce crosstalk 3. Place a 10 uF decoupling capacitor 4. Place a 0.1 uF decoupling capacitor close to the pin.	**Step 1-3:**  **Step 4:** 	
VDD_PLL1	27	P	Power supply for APLL1 1. Place a 0.1 uF capacitor close to the supply 2. Place a ferrite bead (recommended 220 ohm) to reduce crosstalk 3. Place a 10 uF decoupling capacitor 4. Place a 0.1 uF decoupling capacitor close to the pin.	**Step 1-3:**  **Step 4:** 	

VDD_PLL2	36	P	Power supply for APLL2 1. Place a 0.1 uF capacitor close to the supply 2. Place a ferrite bead (recommended 220 ohm) to reduce crosstalk 3. Place a 10 uF decoupling capacitor 4. Place a 0.1 uF decoupling capacitor close to the pin.	**Step 1-3:**  **Step 4:** 	
VDD_DIG	4	P	Power supply for digital 1. Place a 1 uF capacitor close to the supply 2. Place a 0.1 uF decoupling capacitor close to the pin.	**Step 1:**  **Step 2:** 	

VDD_IN	5	P	Power supply for inputs 1. Place a 0.1 uF capacitor close to the supply 2. Place a ferrite bead (recommended 220 ohm) to reduce crosstalk 3. Place a 10 uF decoupling capacitor 4. Place a 0.1 uF decoupling capacitor close to the pin.	**Step 1-3:**  **Step 4:** 	
DAP	PAD	G	Tie GND (DAP) to GND		

PIN NAME	PIN NO.	TYPE	DESCRIPTION	PIN TERMINATION	TI Feedback
CORE BLOCKS					
LF1	29	A	1. Place a 470 nF capacitor on LF1 **NOTE:** This is the external loop filter capacitor for APLL1		
LF2	34	A	1. Place a 100 nF capacitor on LF2 **NOTE:** This is the external loop filter capacitor for APLL2		
CAP_DIG	3	A	1. Place a 10 uF capacitor on CAP_DIG **NOTE:** This is the external bypass capacitor for Digital Core Logic		
CAP_PLL1	28	A	1. Place a 10 uF capacitor on CAP_PPL1 **NOTE:** This is the external bypass capacitor for APLL1 VCO		
CAP_PLL2	35	A	1. Place a 10 uF capacitor on CAP_PPL2 **NOTE:** This is the external bypass capacitor for APLL2 VCO		

<table>
<tr><th colspan="2">PIN</th><th rowspan="2">TYPE</th><th rowspan="2">DESCRIPTION</th><th rowspan="2">PIN TERMINATION</th><th rowspan="2">TI Feedback</th></tr>
<tr><th>NAME</th><th>NO.</th></tr>
<tr><td colspan="6">INPUT BLOCKS</td></tr>
<tr><td>XO_P</td><td>31</td><td>I</td><td rowspan="2">XO/TCXO/OCXO Input

1. Please select a termination shown on the right that matches your XO input type.</td><td rowspan="6"> 

<table>
<tr><th>VDD</th><th>R1 (Ω)</th><th>R2 (Ω)</th></tr>
<tr><td>3.3 V</td><td>125</td><td>375</td></tr>
<tr><td>2.5 V</td><td>0</td><td>open</td></tr>
<tr><td>1.8 V</td><td>0</td><td>open</td></tr>
</table>

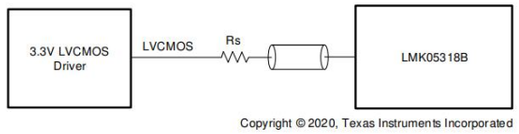
Figure 9-8. Single-Ended LVCMOS to XO Input (XO_P)
 

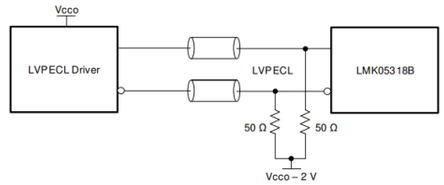
Figure 9-9. Single-Ended LVCMOS (1.8, 2.5, 3.3 V) to Reference (PRIREF_P/SECREF_P)
 

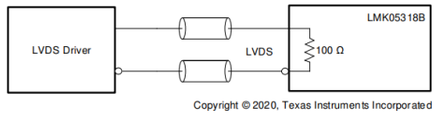
Figure 9-10. DC-Coupled LVPECL to Reference (PRIREF_P/SECREF_P) or XO Inputs
 

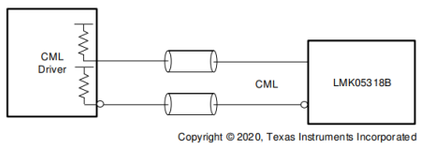
Figure 9-11. DC-Coupled LVDS to Reference (PRIREF/SECREF) or XO Inputs
 

Figure 9-12. DC-Coupled CML (Source Terminated) to Reference (PRIREF/SECREF) or XO Inputs</td><td></td></tr>
<tr><td>XO_N</td><td>32</td><td>I</td><td></td></tr>
<tr><td>PRIREF_P</td><td>6</td><td>I</td><td rowspan="4">Clock Inputs

1. Please select a termination shown on the right that matches your input format type.</td><td></td></tr>
<tr><td>PRIREF_N</td><td>7</td><td>I</td><td></td></tr>
<tr><td>SECREF_P</td><td>10</td><td>I</td><td></td></tr>
<tr><td>SECREF_N</td><td>11</td><td>I</td><td></td></tr>
</table>

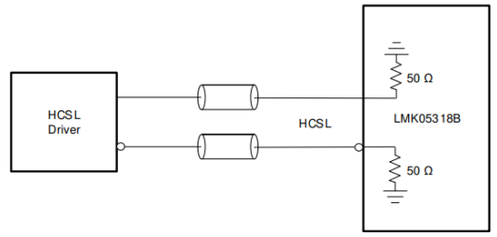


Figure 9-13. HCSL (Load Terminated) to Reference (PRIREF/SECREF) or XO Inputs

Driver	R_B (Ω)
LVDS	open
CML*	open
3.3-V LVPECL	150
2.5-V LVPECL	82
HCSL	50

*CML driver has 50-Ω pull-up

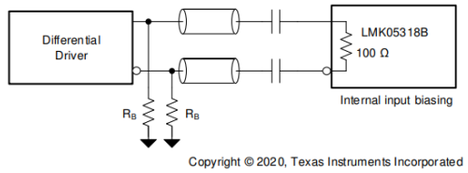
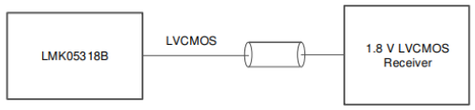
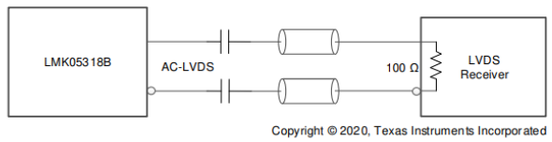
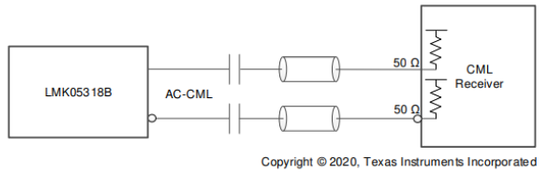
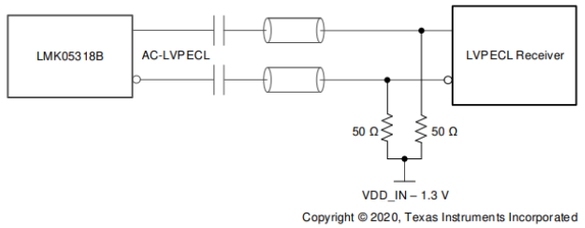
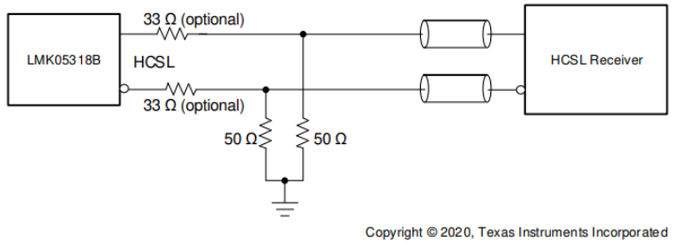


Figure 9-14. AC-Coupled Differential to Reference (PRIREF/SECREF) or XO Inputs

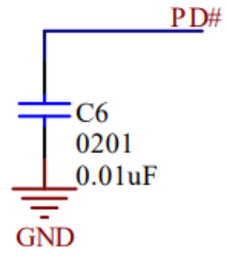
PIN		TYPE	DESCRIPTION	PIN TERMINATION	TI Feedback
NAME	NO.				
OUTPUT BLOCKS					
OUT0_P	14	O	Clock Outputs 1. Please select a termination shown on the right that matches your output format type.	 **Figure 9-26. 1.8-V LVCMOS Output to 1.8-V LVCMOS Receiver**  Copyright © 2020, Texas Instruments Incorporated **Figure 9-27. AC-LVDS Output to LVDS Receiver With Internal Termination/Biasing**  Copyright © 2020, Texas Instruments Incorporated **Figure 9-28. AC-CML Output to CML Receiver With Internal Termination/Biasing**  Copyright © 2020, Texas Instruments Incorporated **Figure 9-29. AC-LVPECL Output to LVPECL Receiver With External Termination/Biasing**  Copyright © 2020, Texas Instruments Incorporated If HCSL Internal Termination (50-Ω to GND) is enabled, short 33-Ω and remove 50-Ω external resistors. **Figure 9-30. HCSL Output to HCSL Receiver With External Source Termination**	
OUT0_N	15	O			
OUT1_P	17	O			
OUT1_N	16	O			
OUT2_P	20	O			
OUT2_N	21	O			
OUT3_P	23	O			
OUT3_N	22	O			
OUT4_P	39	O			
OUT4_N	38	O			
OUT5_P	42	O			
OUT5_N	41	O			
OUT6_P	45	O			
OUT6_N	44	O			
OUT7_P	48	O			
OUT7_N	47	O			

<table>
<tr><th colspan="2">PIN</th><th>TYPE</th><th>DESCRIPTION</th><th>PIN TERMINATION</th><th>TI Feedback</th></tr>
<tr><th>NAME</th><th>NO.</th><th></th><th></th><th></th><th></th></tr>
<tr><td colspan="6">LOGIC CONTROL/STATUS</td></tr>
<tr><td>HW_SW_CTRL</td><td>9</td><td>I</td><td colspan="2">The HW_SW_CTRL can be tied to GND, tied to VCC, or left floating. Please observe the table below to determine what setting is selected for each termination.

6.1 Device Start-Up Modes

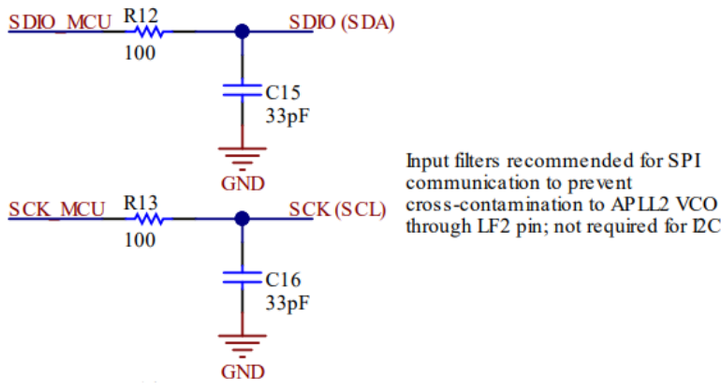
The HW_SW_CTRL input pin selects the device start-up mode that determines the memory page (EEPROM or ROM) used to initialize the registers, the serial interface, and the logic pin functions at power-on reset. The initial register settings determine the frequency configuration of the device on start-up. After start-up, the device registers can be accessed through the serial interface for device monitoring and programming, and the logic pins will function as defined by the selected mode.

Table 6-2. Device Start-Up Modes
<table><tr><th>HW_SW_CTRL INPUT LEVEL(1)</th><th>START-UP MODE</th><th>MODE DESCRIPTION</th></tr><tr><td>0</td><td>EEPROM + I²C (Soft pin mode)</td><td>Registers are initialized from EEPROM, and I²C interface is enabled.
Logic pins:
• SDA/SDI, SCL/SCK: I²C Data, I²C Clock (open-drain)
• GPIO0/SYNCN: Output SYNC Input (active low). Pull up externally if not used.
• GPIO1/SCS (1): I²C Address LSB Select (Low = 00b, Float = 01b, High = 10b)
• GPIO2/SDO/FINC (2): DPLL DCO Frequency Increment (active high)
• STATUS1/FDEC (2): DPLL DCO Frequency Decrement (active high), or Status output</td></tr><tr><td>Float (V_{IM})</td><td>EEPROM + SPI (Soft pin mode)</td><td>Registers are initialized from EEPROM, and SPI interface is enabled.
Logic pins:
• SDA/SDI, SCL/SCK: SPI Data In (SDI), SPI Clock (SCK)
• GPIO0/SYNCN: Output SYNC Input (active low). Pull up externally if not used.
• GPIO1/SCS: SPI Chip Select (SCS)
• GPIO2/SDO/FINC: SPI Data Out (SDO)</td></tr><tr><td>1</td><td>ROM + I²C (Hard pin mode)</td><td>Registers are initialized from the ROM page selected by GPIO pins, and I²C interface is enabled.
Logic pins:
• SDA/SDI, SCL/SCK: I²C Data, I²C Clock (open-drain)
• GPIO[2:0] (1): ROM Page Select Inputs (000b to 111b) during POR.
• After POR, GPIO2/SDO/FINC and STATUS1/FDEC pins can function the same as for HW_SW_CTRL = 0.</td></tr></table>(1) The input levels on these pins are sampled only during POR.
(2) FINC and FDEC pins are only available when DCO mode and GPIO pin control are enabled by registers.</td><td></td></tr>
<tr><td>PDN</td><td>13</td><td>I</td><td>Device power down (Active Low)

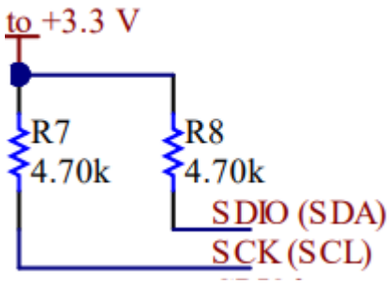
1. It is recommended to place a 0.01 uF capacitor on the PD#</td><td> 
</td><td></td></tr>
</table>

<table>
<tr>
<td>SDA/SDI</td>
<td>25</td>
<td>I/O</td>
<td>SPI or I²C Data (SDA)

For the SPI interface:
1. Place a 100-ohm series resistor
2. Place a 33-pF capacitor to GND

For the I2C interface:
1. Place a 4.7 kohm resistor tied to V_{cc}</td>
<td rowspan="2"><u>SPI Interface:</u>
 

Input filters recommended for SPI communication to prevent cross-contamination to APLL2 VCO through LF2 pin; not required for I2C

<u>I2C Interface:</u>
 
</td>
<td></td>
</tr>
<tr>
<td>SCL/SCK</td>
<td>26</td>
<td>I</td>
<td>SPI or I²C Clock (SCL)

For the SPI interface:
1. Place a 100-ohm series resistor
2. Place a 33-pF capacitor to GND

For the I2C interface:
1. Place a 4.7 kohm resistor tied to V_{cc}</td>
<td></td>
</tr>
</table>

<table>
<tr><td>GPIO0/SYNCN</td><td>12</td><td>I</td><td rowspan="3">Please observe the table below to determine what setting is selected for each termination.

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<table><tr><th>HW_SW_CTRL INPUT LEVEL(1)</th><th>START-UP MODE</th><th>MODE DESCRIPTION</th></tr><tr><td>0</td><td>EEPROM + I²C (Soft pin mode)</td><td>Registers are initialized from EEPROM, and I²C interface is enabled.
Logic pins:
• SDA/SDI, SCL/SCK: I²C Data, I²C Clock (open-drain)
• GPIO0/SYNCN: Output SYNC Input (active low). Pull up externally if not used.
• GPIO1/SCS (1): I²C Address LSB Select (Low = 00b, Float = 01b, High = 10b)
• GPIO2/SDO/FINC (2): DPLL DCO Frequency Increment (active high)
• STATUS1/FDEC (2): DPLL DCO Frequency Decrement (active high), or Status output</td></tr><tr><td>Float (V_{IM})</td><td>EEPROM + SPI (Soft pin mode)</td><td>Registers are initialized from EEPROM, and SPI interface is enabled.
Logic pins:
• SDA/SDI, SCL/SCK: SPI Data In (SDI), SPI Clock (SCK)
• GPIO0/SYNCN: Output SYNC Input (active low). Pull up externally if not used.
• GPIO1/SCS: SPI Chip Select (SCS)
• GPIO2/SDO/FINC: SPI Data Out (SDO)</td></tr><tr><td>1</td><td>ROM + I²C (Hard pin mode)</td><td>Registers are initialized from the ROM page selected by GPIO pins, and I²C interface is enabled.
Logic pins:
• SDA/SDI, SCL/SCK: I²C Data, I²C Clock (open-drain)
• GPIO[2:0] (1): ROM Page Select Inputs (000b to 111b) during POR.
• After POR, GPIO2/SDO/FINC and STATUS1/FDEC pins can function the same as for HW_SW_CTRL = 0.</td></tr></table>(1) The input levels on these pins are sampled only during POR.
(2) FINC and FDEC pins are only available when DCO mode and GPIO pin control are enabled by registers.</td><td></td></tr>
<tr><td>GPIO1/SCS</td><td>24</td><td>I</td><td></td></tr>
<tr><td>GPIO2/SDO/FINC</td><td>30</td><td>I/O</td><td></td></tr>
<tr><td>STATUS0</td><td>1</td><td>I/O</td><td rowspan="2">Each output has programmable status signal selection, driver type (3.3-V LVCMOS or open-drain), and status polarity. Open-drain requires an external pullup resistor. Leave pin floating if unused. In I2C mode, the STATUS1/FDEC pin can function as a DCO mode control input pin. See Table 6-2 above for more details.</td><td></td></tr>
<tr><td>STATUS1/FDEC</td><td>2</td><td>I/O</td><td></td></tr>
<tr><td>REFSEL</td><td>8</td><td>I</td><td>REFSEL can be tied to GND, tied to VCC, or left floating.
1. REFSEL = 0 (select PRIREF as input)
2. REFSEL = 1 (select SECREF as input)
3. REFSEL = Float or VIM (Auto Select input)

This control pin must be enabled by register default or programming. Leave pin floating if unused.</td><td></td></tr>
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