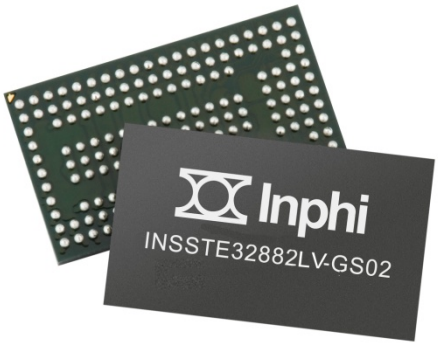
INSSTE32882LV
DDR3(L) Registering Clock Driver with Parity Checking Data Sheet



Applications

- Mid and High Performance Servers
- High Performance Workstations
- High Reliability & Telecom Systems

Features

- Single Register Quad Rank RDIMM support
- INSSTE32882LV-GS02 meets or exceeds all JESD82-xx performance specifications for DDR3(L)-800/1066/1333/1600 rates at 1.5V and 1.35 V V_{DD}. Specifications highlighted in blue exceed JEDEC specifications
- Operational at DDR3(L)-1866 rates
- Exceeds JEDEC re-driven dynamic clock offset specification (t_{DYNOFF})
- Exceeds JEDEC Jitter requirements
- Supports custom RDIMM modules via programmable driver characteristics
- Supports existing RDIMM modules
- Supports all JEDEC lower power modes including weak-drive mode
- ESD protection exceeds JESD22
  HBM – **4000V**
  CDM – 500V
- Latch-up exceeds JESD78 class 2
- Available in two 176 TFBGA Eco-Friendly "Green" Package types
  8.00 mm x 13.50 mm (MO-246F) or
  6.00 mm x 15.00 mm (MO-246B)

Description

This 28-bit 1:2 or 26-bit 1:2 and 4-bit 1:1 registering clock driver with parity is designed for 1.5 V or 1.35 V V_{DD} operation.

All inputs are 1.5/1.35 V CMOS compatible. All outputs are 1.5/1.35 V CMOS drivers optimized to drive single/multi- terminated traces in DDR3 RDIMM. The clock outputs Yn and Yn# and control outputs QxCKEn, QxCSn# and QxODTn can be driven with a different strength and skew to compensate for different loading and equalize signal travel speed.

The INSSTE32882LV has two basic modes of operation associated with the Quad Chip Select Enable (QCSEN#) input. When the QCSEN# input pin is pulled HIGH (or open), the component has two chip select inputs, DCS0# and DCS1#, and two copies of each chip select output, QACS0#, QACS1#, QBCS0# and QBCS1#. This is the "QuadCS disabled" mode. When the QCSEN# input pin is pulled LOW, the component has four chip select inputs DCS[3:0]#, and four chip select outputs, QCS[3:0]#. This is the "QuadCS enabled" mode. Through the remainder of this specification, DCS[n:0]# will indicate all of the chip select inputs, where n=1 for QuadCS disabled, and n=3 for QuadCS enabled. QxCS[n:0]# will indicate all of the chip select outputs.

Description (cont'd.)

The INSSTE32882LV operates from a differential clock (CK and CK#). Data are registered at the crossing of CK going HIGH, and CK# going LOW. The data could be either re-driven to the outputs once exactly one of the input signals DCS[n:0]# is driven LOW or it could be used to access device internal control registers when certain input conditions are met.

Based on control register settings the device can change its output characteristics to match different DIMM net topologies. The timing can be changed to compensate for different flight time of signals within the target application. By disabling unused outputs the power consumption is reduced.

Initialization

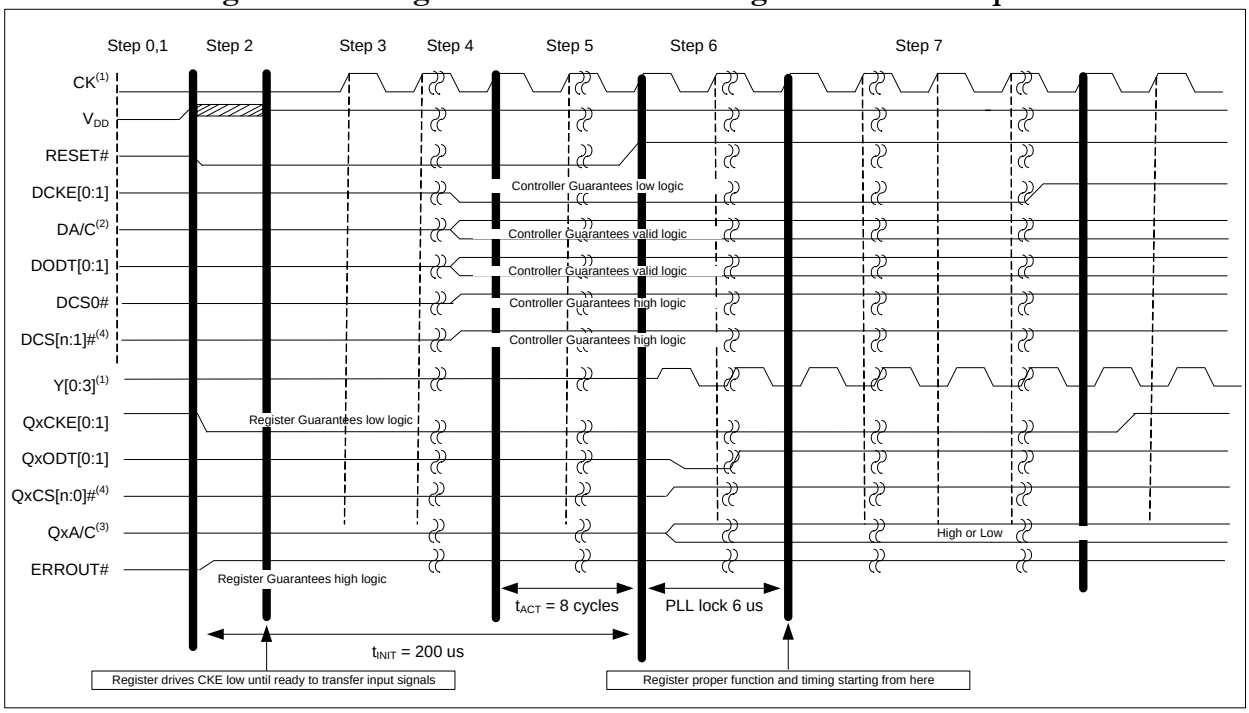
The INSSTE32882LV can be powered-on at 1.5 V or 1.35 V. After the voltage transition, stable power is provided for a minimum of 200 µS with RESET# asserted.

When the reset input RESET# is LOW, all input receivers are disabled, and can be left floating. Therefore the reference voltage (VREF) doesn't need to be stable. In addition, when RESET# is LOW, all control registers are restored to their default states. The outputs QACKE0, QACKE1, QBCKE0 and QBCKE1 are driven LOW during reset. All other outputs float. As long as the RESET# input is pulled LOW the register is in low power state and input termination is not present. A certain period of time (t_{ACT}) before the RESET# input is pulled HIGH the reference voltage needs to be stable within specification, the clock input signal must be stable, the register inputs DCS0# and DCS1# must be pulled HIGH to prevent accidental access to the control registers and DCKE0 as well as DCKE1 must be pulled LOW. After reset and after the stabilization time (t_{STAB}) the register will meet the input setup- and hold specification, as well as accept and transfer input signals to the corresponding outputs. The RESET# input must always be held at a valid logic level once the input clock is present.

To ensure defined outputs from the register before a stable clock has been supplied, the register will enter the reset state during power-up. It will leave this state only after a LOW to HIGH transition on RESET# while a stable clock signal is present on CK and CK#. In the DDR3(L) RDIMM application, RESET# is specified to be completely asynchronous with respect to CK and CK#.

Initialization (cont'd.)

Figure 1. Timing of clock and data during initialization sequence



(1) CK# is left out for better visibility
(2) DCKE0, DCKE1, DODT0, DODT1, DCS0# and DCS1# are not included in this range
(3) QxCKEn, QxODTn, QxCSn# are not included in this range
(4) n=1 for QuadCS disabled mode, n=3 for QuadCS enabled mode

Initialization (cont'd.)

From a device perspective, the initialization sequence is as shown in Table 1 and Table 2.

Table 1 -- INSSTE32882LV Device Initialization Sequence for Inputs [1]

Step	Power	Inputs: Signals provided by the controller							
	VDD, AVDD, PVDD	RESET#	Vref	DCS[n:0]#[2]	DODT[0:1]	DCKE[0:1]	DA/C	PAR_IN	CK CK#
0	0V	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z
1	0-->V_{DD}	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	L
2[4]	V_{DD} 1.5 V-->1.35 V 1.35 V-->1.5 V	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	L
3	V_{DD}	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	Running
4	V_{DD}	L	X or Z	H	X or Z	L	X or Z	X or Z	Running
5	V_{DD}	L	Stable Voltage	H	X	L	X	X	Running
6	V_{DD}	H	Stable Voltage	H	X	L	X	X	Running
7[7]	V_{DD}	H	Stable Voltage	H	X	X	X	X	Running

Table 2 -- INSSTE32882LV Device Initialization Sequence for Outputs [1]

Step	Power	Outputs: Signals provided by the device						
	VDD AVDD PVDD	QxCS[n:0]#[2]	QxODT[0:1]	QxCKE[0:1]	QxA/C	ERROUT#	Y[0:3] Y[0:3]#	FBOUT[3]
0	0V	Z	Z	Z	Z	Z	Z	Z
1	0-->V_{DD}	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z
2[4]	V_{DD} 1.5 V-->1.35 V 1.35 V-->1.5 V	Z	Z	L[5]	Z	H[5]	Z	Z
3	V_{DD}	Z	Z	L	Z	H	Z	Z
4	V_{DD}	Z	Z	L	Z	H	Z	Z
5	V_{DD}	Z	Z	L	Z	H	Z	Z
6	V_{DD}	H	L[6]	L	X or Z	H	Running	Running
7[7]	V_{DD}	After Step 6 (Step 7 and beyond), the device outputs are as defined in the device Function Tables (see Tables 14-18)						

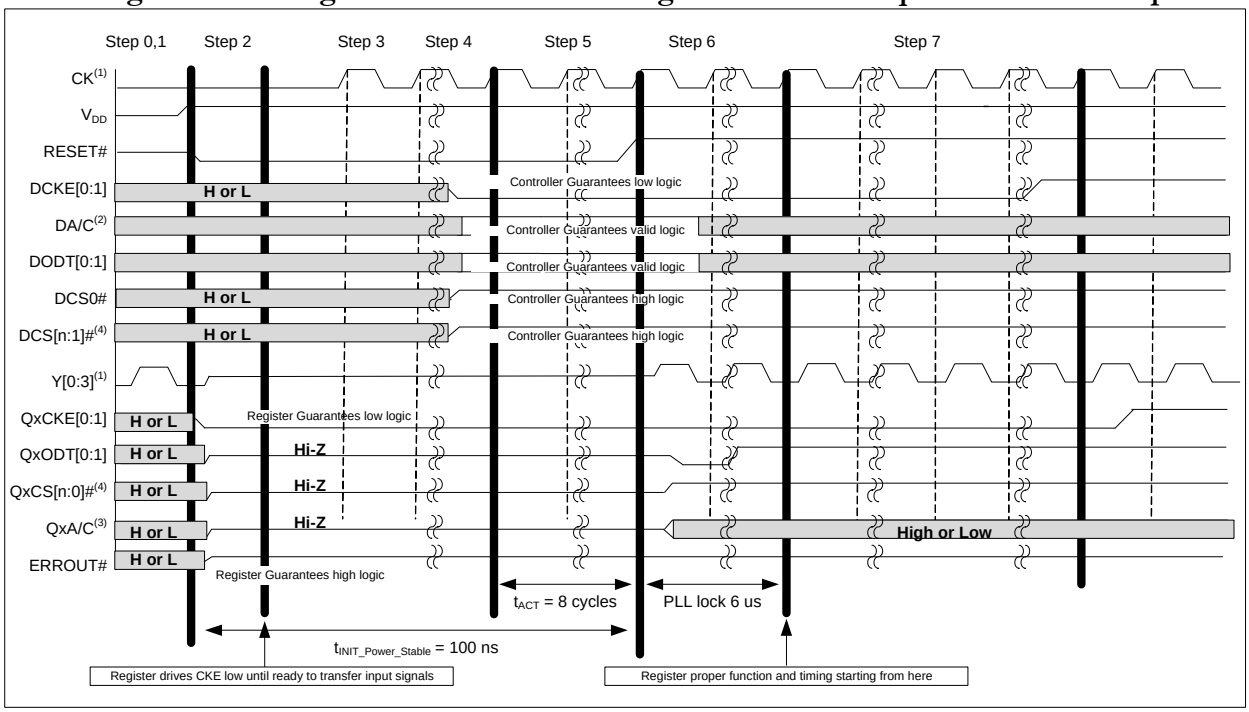
Notes:
1 X = Logic LOW or logic HIGH. Z = floating.
2. n = 1 for QuadCS disabled mode, n = 3 for QuadCS enabled mode
3. The feedback clock (FBOUT and FBOUT#) pins may or may not be actively driven by the device.
4. The system may power up using either 1.5 V or 1.35 V. The BIOS reads the SPD and adjusts the voltage if needed from 1.35 V to 1.5 V or from 1.5 V to 1.35 V. After the voltage transition, stable power is provided for a minimum of 200 uS with RESET# asserted.
5. QxCKEn and ERROUT# will be driven to these logic states by the register after RESET# is driven LOW and VDD is 1.5 V or 1.35 V (nominal).
6. This indicates the state of QxODTx after RESET# switches from LOW-to-HIGH and before the rising CK edge (falling CK# edge). After the first rising CK edge, within (tSTAB - tACT) us, the state of QxODTx is a function of DODTx (HIGH or LOW).
7. Step 7 is a typical usage example and is not a register requirement.

As part of the initialization, all control words are reset to their default state that is "0". After initialization, the memory controller only needs to write to the control registers whose contents need to be changed.

Reset Initialization with Stable Power

The timing diagram in Figure 2 depicts the initialization sequence with stable power and clock. This will apply to the situation when we have a soft reset in the system. RESET# is asserted for a minimum of 100 ns. This RESET# timing is based on DDR3(L) DRAM Reset Initialization with Stable Power requirement, and is a minimum requirement. Actual RESET# timing can vary based on specific system requirement, but it cannot be less than 100ns as required by JESD79-3 Specification.

Figure 2. Timing of clock and data during initialization sequence with stable power



(1) CK# is left out for better visibility
(2) DCKE0, DCKE1, DODT0, DODT1, DCS0# and DCS1# are not included in this range
(3) QxCKEn, QxODTn, QxCSn# are not included in this range
(4) n=1 for QuadCS disabled mode, n=3 for QuadCS enabled mode

Reset Initialization with Stable Power (cont'd.)

Table 3 -- INSSTE32882LV Device Initialization Sequence when Power and Clock are Stable for Inputs [1]

Step	Power	Inputs: Signals provided by the controller							
	VDD, AVDD, PVDD	RESET#	Vref	DCS[n:0]#[2]	DODT[0:1]	DCKE[0:1]	DA/C	PAR_IN	CK CK#
0	V_{DD}	H	Stable Voltage	X	X	X	X	X	Running
1	V_{DD}	H	Stable Voltage	X	X	X	X	X	Running
2	V_{DD}	L	Stable Voltage	X	X	X	X	X	Running
3	V_{DD}	L	Stable Voltage	X	X	X	X	X	Running
4	V_{DD}	L	Stable Voltage	H	X	L	X	X	Running
5	V_{DD}	L	Stable Voltage	H	X	L	X	X	Running
6	V_{DD}	H	Stable Voltage	H	X	L	X	X	Running
7[6]	V_{DD}	H	Stable Voltage	H	X	X	X	X	Running

Table 4 -- INSSTE32882LV Device Initialization Sequence when Power and Clock are Stable for Outputs [1]

Step	Power	Outputs: Signals provided by the device						
	VDD AVDD PVDD	QxCS[n:0]#[2]	QxODT[0:1]	QxCKE[0:1]	QxA/C	ERROUT#	Y[0:3] Y[0:3]#	FBOUT[3]
0	V_{DD}	X	X	X	X	X	Running	Running
1	V_{DD}	X	X	X	X	X	Running	Running
2	V_{DD}	Z	Z	L[4]	Z	H[4]	Z	Z
3	V_{DD}	Z	Z	L	Z	H	Z	Z
4	V_{DD}	Z	Z	L	Z	H	Z	Z
5	V_{DD}	Z	Z	L	Z	H	Z	Z
6	V_{DD}	H	L[5]	L	X	H	Running	Running
7	V_{DD}	After Step 6 (Step 7 and beyond), the device outputs are as defined in the device Function Tables (see Tables 4-18)						

Notes:
1. X = Logic LOW or logic HIGH. Z = floating.
2. n = 1 for QuadCS disabled mode, n = 3 for QuadCS enabled mode
3. The feedback clock (FBOUT and FBOUT#) pins may or may not be actively driven by the device.
4. QxCKEn and ERROUT# will be driven to these logic states by the register after RESET# is driven LOW and VDD is 1.5 V or 1.35 V (nominal).
5. This indicates the state of QxODTx after RESET# switches from LOW-to-HIGH and before the rising CK edge (falling CK# edge). After the first rising CK edge, within (tSTAB - tACT) us, the state of QxODTx is a function of DODTx (HIGH or LOW).
6. Step 7 is a typical usage example and is not a register requirement.

Parity

The INSSTE32882LV includes a parity checking function. The INSSTE32882LV accepts a parity bit from the memory controller at its input pin PAR_IN one cycle after the corresponding data input, compares it with the data received on the D-inputs and indicates on its open-drain ERROUT# pin (active LOW) whether a parity error has occurred. The computation only takes place for data which is qualified by at least one of the DCS[n:0]# signals being acceptable.

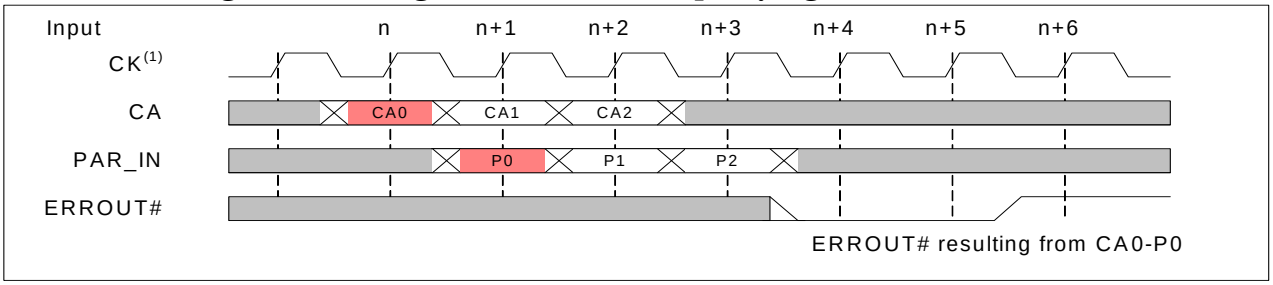
If an error occurs, an ERROUT# is driven LOW with the third input clock edge after the corresponding data on the D-inputs. It becomes high impedance with the 5th input clock cycle after the data corresponding with a parity error. In case of consecutive errors ERROUT# becomes high impedance with the 5th input clock cycle after the last data corresponding with a parity error. The DIMM-dependent signals (DCKE[1:0], DCS#[n:0], and DODT[1:0]) are not included in the parity check computations.

Parity Timing Scheme Waveforms

The PAR_IN signal arrives one input clock cycle after the corresponding data input signals. ERROUT# is generated three input clock cycles after the corresponding data is registered. If ERROUT# goes LOW, it stays LOW for a minimum of two input clock cycles or until RESET# is driven LOW.

Figure 3 shows the parity diagram with single parity-error occurrence and assumes the occurrence of only one parity error when data is clocked in at the n input clock cycle (PAR_IN clocked in on the n+1 input clock cycle).

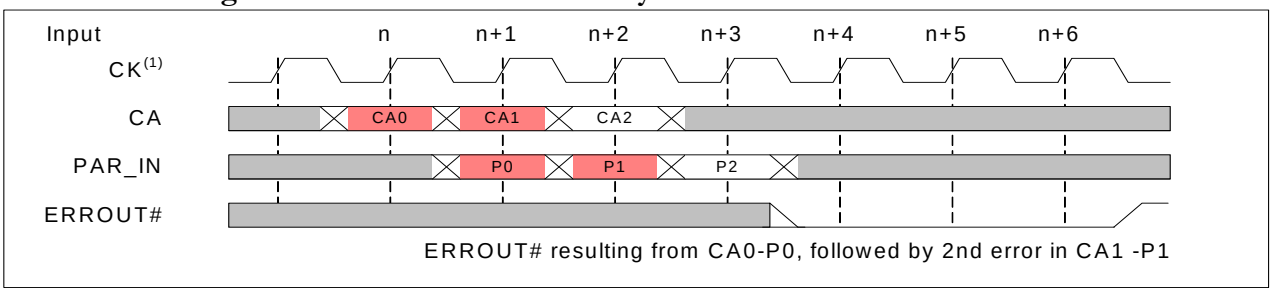
Figure 3. Timing of clock, data, and parity signal



(1) CK# is left out for better visibility

Figure 4 shows the parity diagram with two consecutive parity-error occurrences and assumes the occurrence of both parity errors when data is clocked in at the n and n+1 input clock cycles (PAR_IN clocked in on the n+1 and n+2 input clock cycles).

Figure 4. Two Consecutive Parity-Error Occurrences

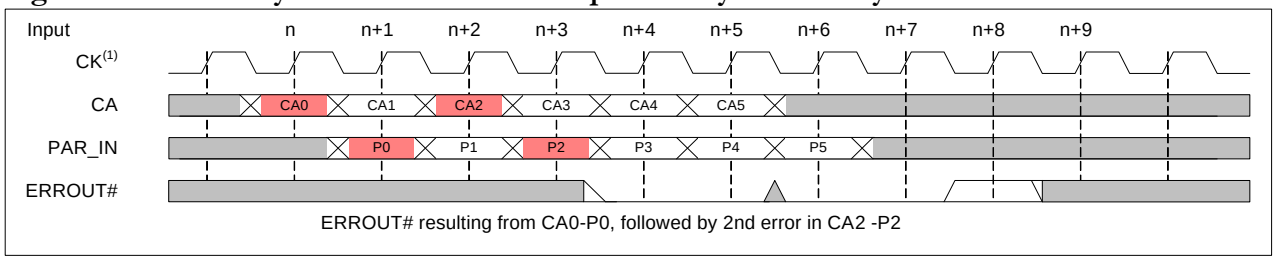


(1) CK# is left out for better visibility

Parity Timing Scheme Waveforms (cont'd.)

Figure 5 shows the parity diagram with two parity-error occurrences separated by a clock cycle with no error occurrence. The diagram assumes the occurrence of two parity errors when data is clocked in at the n and n+2 input clock cycles (PAR_IN clocked in on the n+1 and n+3 input clock cycles).

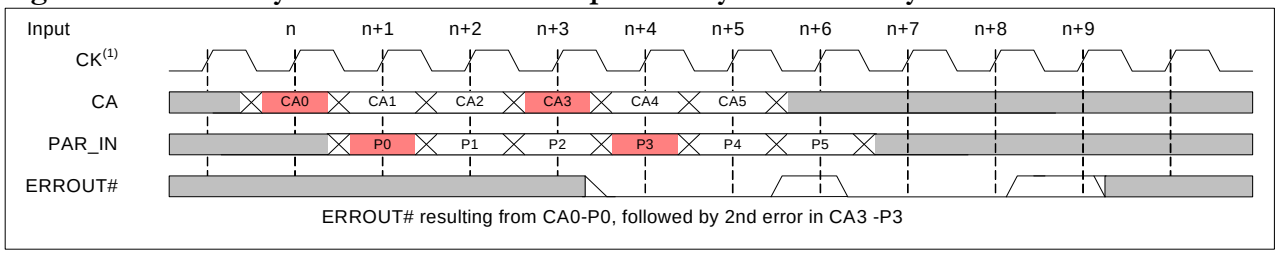
Figure 5. Two Parity-Error Occurrences Separated by a Clock Cycle of No Error Occurrence



(1) CK# is left out for better visibility

Figure 6 shows the parity diagram with two parity-error occurrences separated by two input clock cycles with no error occurrence. The diagram assumes the occurrence of two parity errors when data is clocked in at the n and n+3 input clock cycles (PAR_IN clocked in on the n+1 and n+4 input clock cycles).

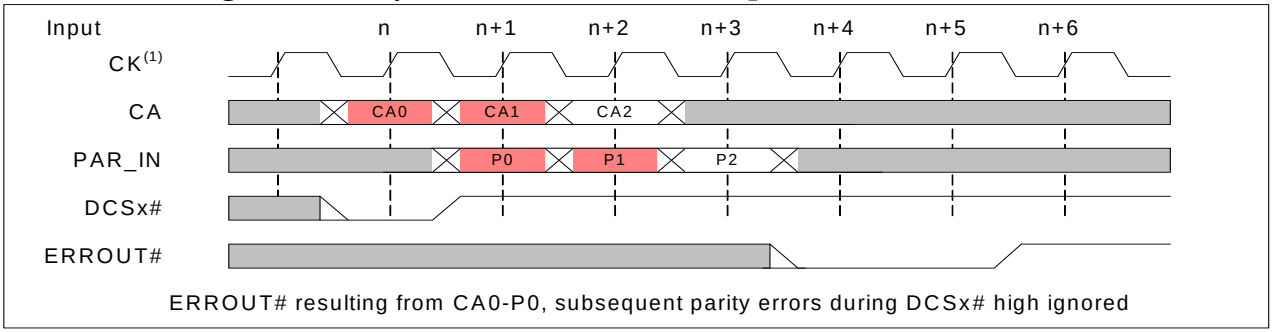
Figure 6. Two Parity-Error Occurrences Separated by two Clock Cycles of No Error Occurrence



(1) CK# is left out for better visibility

Figure 7 shows the parity diagram with two parity-error occurrences; during chip-select and chip-deselect modes. The diagram assumes the occurrence of both parity errors when data is clocked in at the n and n+1 input clock cycles (PAR_IN clocked in on the n+1 and n+2 input clock cycles). Parity error in the chip-select mode is detected, but parity error in the chip-deselect mode is ignored.

Figure 7. Parity-Error Occurrence in Chip-Deselect Mode

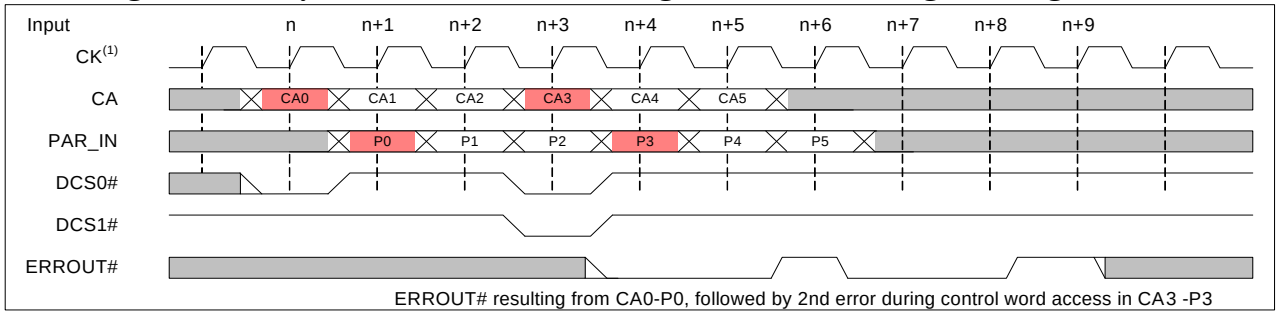


(1) CK# is left out for better visibility

Parity Timing Scheme Waveforms (cont'd.)

Figure 8 shows the parity diagram with two parity-error occurrences; during normal operation and during control register programming. The diagram assumes the occurrence of both parity errors when data is clocked in at the n and n+3 input clock cycles (PAR_IN clocked in on the n+1 and n+4 input clock cycles). The data on the n+3 input clock pulse is intended for the control mode register. Parity error during control mode register programming is detected and the parity functionality is the same as during normal operation. If a parity error occurs, the command is ignored.

Figure 8. Parity-Error Occurrences during Control Word Programming



(1) CK# is left out for better visibility

Power Saving Modes

The device supports different power saving mechanisms.

When both inputs CK and CK# are being held LOW, the device stops operation and enters low-power static and standby operation. It stops its PLL and floats all outputs except QACKE0, QACKE1, QBCKE0 and QBCKE1 which are kept driven LOW. Before the device is taken out of standby operation by applying a stable input clock signal, the register inputs DCS[n:0]# must be pulled HIGH to prevent accidental access to the control registers and DCKE0 as well as DCKE1 must be pulled LOW for a certain period of time (t_{ACT}). The input clock must be stable for a time (t_{STAB}) before any access to the device takes place. Stopping the clocks (CK=CK#=LOW) will only put the INSSTE32882LV in the low-power mode and will not clear the content of the Control Words. The control word registers will reset only when RESET# is driven LOW.

A float feature can be enabled by setting the corresponding bits in the control register. This causes the device to monitor all the DCS[n:0]# inputs and to float all outputs corresponding with the chip select gated inputs when both DCS[n:0]# are HIGH. If any one of the DCS[n:0]# input is LOW, the Qn outputs will function normally.

Once all DCS[n:0]# inputs are HIGH, the gated address command inputs to the register can float to conserve input termination power. DCKE0, DCKE1, DODT0 and DODT1 need to be driven by the system all the time.

The RESET# input has priority over all other power saving mechanisms. When RESET# is driven LOW, it will force the Qn outputs to float, the ERROUT# output HIGH, the QACKE0, QACKE1, QBCKE0 and QBCKE1 outputs LOW and disables Input Bus Termination (IBT).

Register CKE Power Down

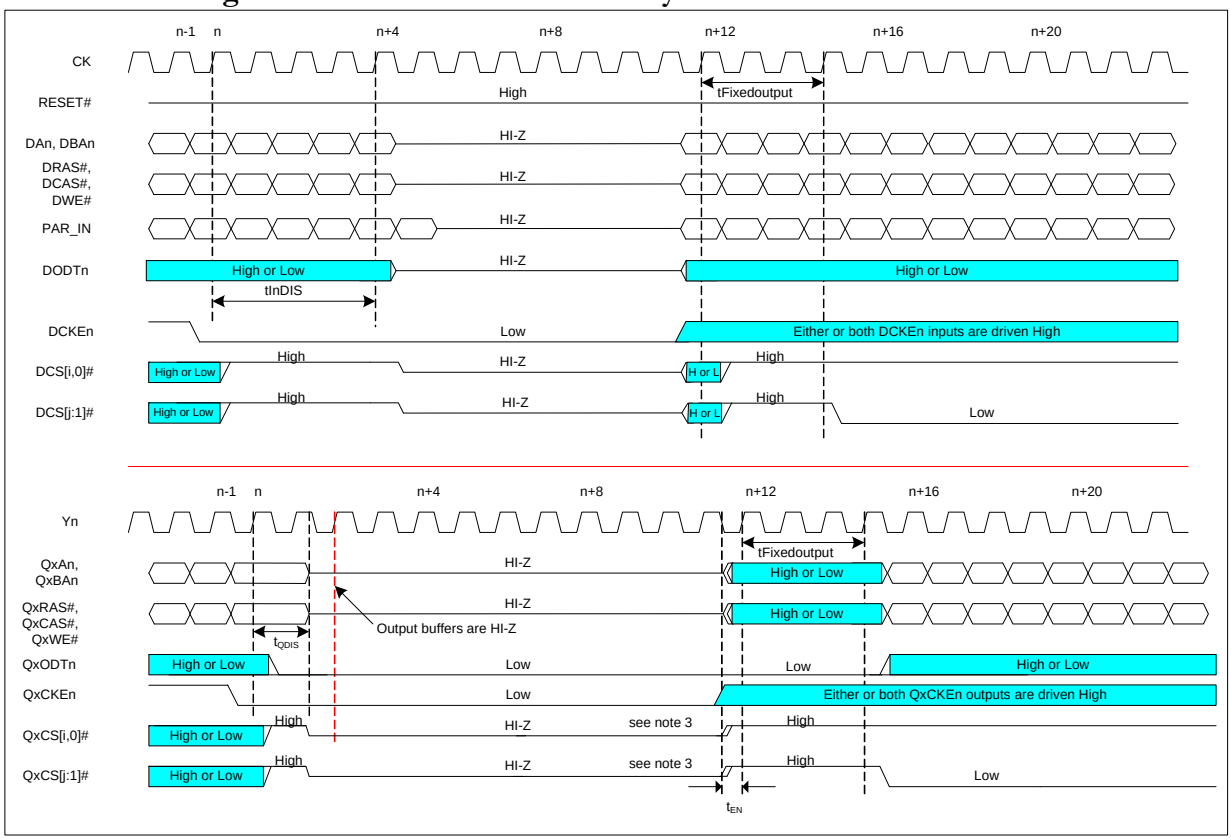
The INSSTE32882LV monitors both DCKEn input signals and enters into power saving state when it latches LOW on both DCKEn inputs and at least one of the DCKEn input has transitioned from HIGH to LOW. If any input Chip Select signal, DCS[n:0]#, is asserted together with DCKEn, the INSSTE32882LV transfers the corresponding command to its outputs together with QxCKEn LOW.

There are two modes of CKE Power Down selected by control word RC9. Bit DBA0 in RC9 indicates whether register turns off IBT or keeps IBT on.

Register CKE Power Down With IBT Off

Upon entry into CKE Power Down mode with IBT off, all register input buffers including IBT are disabled except for CK/CK#, DCKEn, FBIN/FBIN#, and RESET#. The INSSTE32882LV disables input buffers within t_{InDIS} clocks after latching both DCKEn LOW. In order to eliminate any false parity check error, the PAR_IN input buffer has to be kept active for 1 tCK after the Address and Command input buffers are disabled. After t_{InDIS}, the register can tolerate floating input except for CK/CK#, DCKEn and RESET#. The INSSTE32882LV also disables all its output buffers except for Yn/Yn#, QxODTn, QxCKEn and FBOUT/FBOUT#. The Yn/Yn# and FBOUT/FBOUT# outputs continue to drive a valid phase accurate clock signal. The QxODTn and QxCKEn outputs are driven LOW. The register output buffers are Hi-Z t_{QDIS} clock after QxCKEn is driven LOW. This is shown in Figure 9.

Figure 9. Power Down Mode Entry and Exit with IBT Off



(1) i, j only apply for QuadCS capable register. When QuadCS is enabled, i = 2, j = 3
(2) QuadCS disabled: During CKE Power Down Entry/Exit, driving DCS[1,0]# LOW is illegal as it will force INSSTE32882LV into Register Control Word access mode.
(3) Upon CKE Power Down exit, QxCSn# will be held HIGH for maximum of 1 tCK regardless of what DCSn# input level is. For all other operations, QxCSn# outputs will follow DCSn# inputs.

Register CKE Power Down With IBT Off (cont'd.)

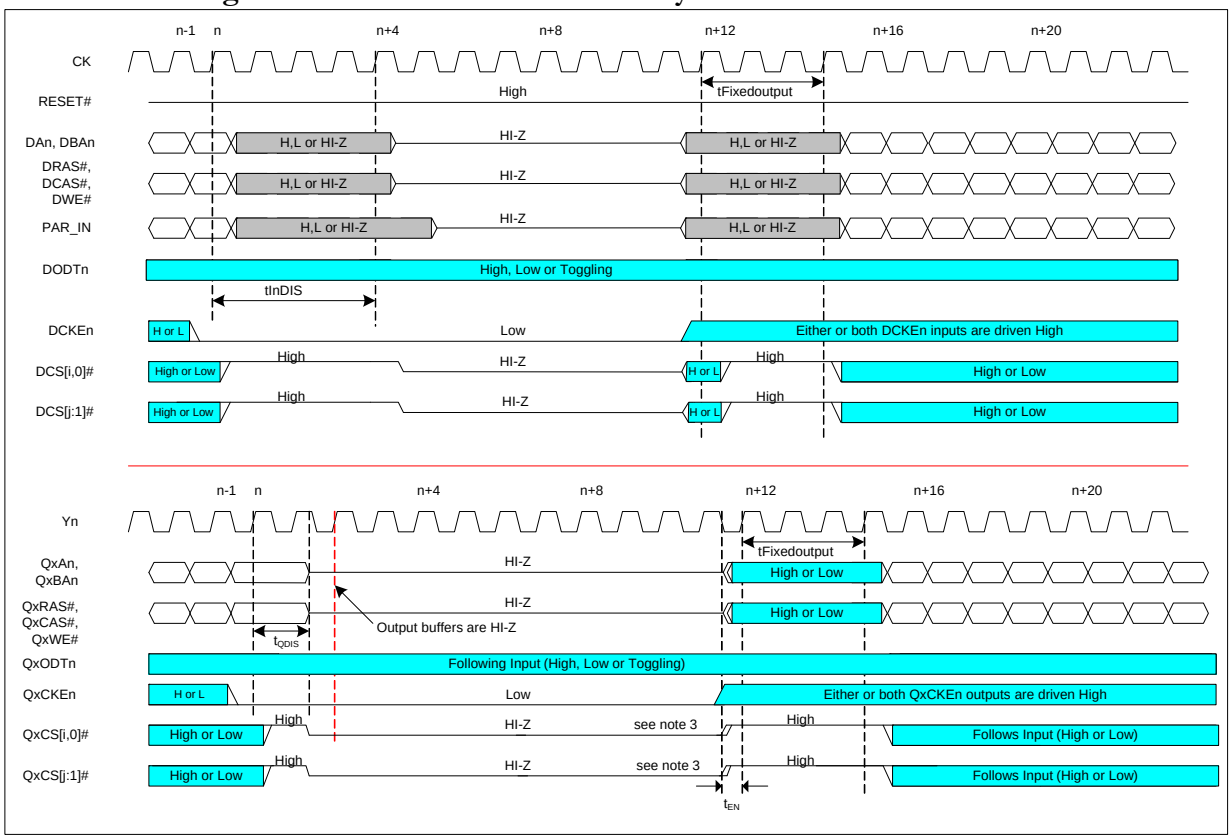
To re-enable the register from this power saving state, valid logic levels are required at all register inputs when either or both DCKEn input are driven HIGH. Upon either DCKE0 or DCKE1 input going HIGH, the register immediately starts driving HIGH on the appropriate QxCKEn signal. The QxCSn# signals are driven HIGH and QxODTn signals are driven LOW. Other output signals QxRAS#, QxCAS#, QxWE# and QxAddr are driven either HIGH or LOW to ensure stable valid logic on all register outputs when QxCKEn goes HIGH. The register drives output signals to these levels for $t_{Fixedoutput}$ to allow input receivers to be stabilized. After the input receivers are stabilized, the register outputs follow their corresponding input levels. When exiting CKE power down mode, either one of the Chip select register inputs DCSn# can be asserted for 1 tCK. For QuadCS capable register, when working in quad rank mode, either two of the Chip select register inputs DCSn# can be asserted for 1 tCK. The register guarantees that input receivers are stabilized within $t_{Fixedoutput}$ clocks after DCKEn input is driven HIGH. This is shown in Figure 10.

Register CKE Power Down With IBT On

Upon entry into CKE Power Down Mode with IBT on, all register input buffers excluding IBT are disabled except for CK/CK#, DCKEn, DODTn, FBIN/FBIN#, and RESET#. The INSSTE32882LV disables input buffers within t_{InDIS} clocks after latching both DCKEn LOW. In order to eliminate any false parity check error, the PAR_IN input buffer has to be kept active for 1 tCK after the Address and Command input buffers are disabled. After t_{InDIS}, the register can tolerate floating input except for CK/CK#, DCKEn, DODTn and RESET#. The INSSTE32882LV also disables all its output buffers except for Yn/Yn#, QxODTn, QxCKEn and FBOUT/FBOUT#. The Yn/Yn# and FBOUT/FBOUT# outputs continue to drive a valid phase accurate clock signal. The QxCKEn outputs are driven LOW. The register output buffers are Hi-Z t_{QDIS} clock after QxCKEn is driven LOW. This is shown in Figure 10.

Register CKE Power Down With IBT On (cont'd.)

Figure 10. Power Down Mode Entry and Exit with IBT On



(1) i, j only apply for QuadCS capable register. When QuadCS is enabled, i = 2, j = 3
(2) QuadCS disabled: During CKE Power Down Entry/Exit, driving DCS[1,0]# LOW is illegal as it will force INSSTE32882LV into Register Control Word access mode.
(3) Upon CKE Power Down exit, QxCSn# will be held HIGH for maximum of 1 tCK regardless of what DCSn# input level is. For all other operations, QxCSn# outputs will follow DCSn# inputs.

To re-enable the INSSTE32882LV from this Power Down Mode with IBT on, valid logic levels are required at all device inputs when either or both DCKEn inputs are driven HIGH. Upon either DCKE0 or DCKE1 input going HIGH, the INSSTE32882LV immediately starts driving HIGH on the appropriate QxCKEn signals. The QxCSn# signals are driven HIGH and the QxODTn signals follow the inputs. Other output signals QxRAS#, QxCAS#, QxWE# and QxAddr are driven either HIGH or LOW to ensure stable valid logic on all device outputs when QxCKEn goes HIGH. The device drives output signals to these levels for $t_{Fixedoutput}$ to allow input receivers to be stabilized. After the input receivers are stabilized, the register outputs follow their corresponding input levels. When exiting CKE power down mode, either one of the Chip select register inputs DCSn# can be asserted for 1 tCK. For QuadCS capable register, when working in quad rank mode, either two of the Chip select register inputs DCSn# can be asserted for 1 tCK. The device guarantees that input receivers are stabilized within $t_{Fixedoutput}$ clocks after DCKEn input is driven HIGH. This is shown in Figure 10.

Clock Stopped Power Down Mode

To support S3 Power Management mode or any other operation that allows Yn clocks to float, the INSSTE32882LV supports a Clock Stopped Power Down Mode. When both inputs CK and CK# are being held LOW ($V_{IL(static)}$) or float (will eventually settle at LOW because of the (10 K-100 KΩ) pulldown resistor in the CK/CK# input buffer), the device stops operation and enters low-power static and standby operation. The corresponding timing requirements are shown in Figure 11, "Clock Stopped Power Down Entry and Exit with IBT On" and Figure 12, "Clock Stopped Power Down Entry and Exit with IBT Off", and parameters shown in Table 25. The register device will stop its PLL and floats all outputs except QACKE0, QACKE1, QBCKE0 and QBCKE1, which will be kept driven LOW.

The Clock Stopped power down mode can only be utilized once the DRAM receives a self-refresh command. In this state, the DRAM ignores all inputs except DCKEn. Hence, all register outputs besides QxCKE0 and QxCKE1 are disabled.

Clock Stopped Power Down Mode Entry

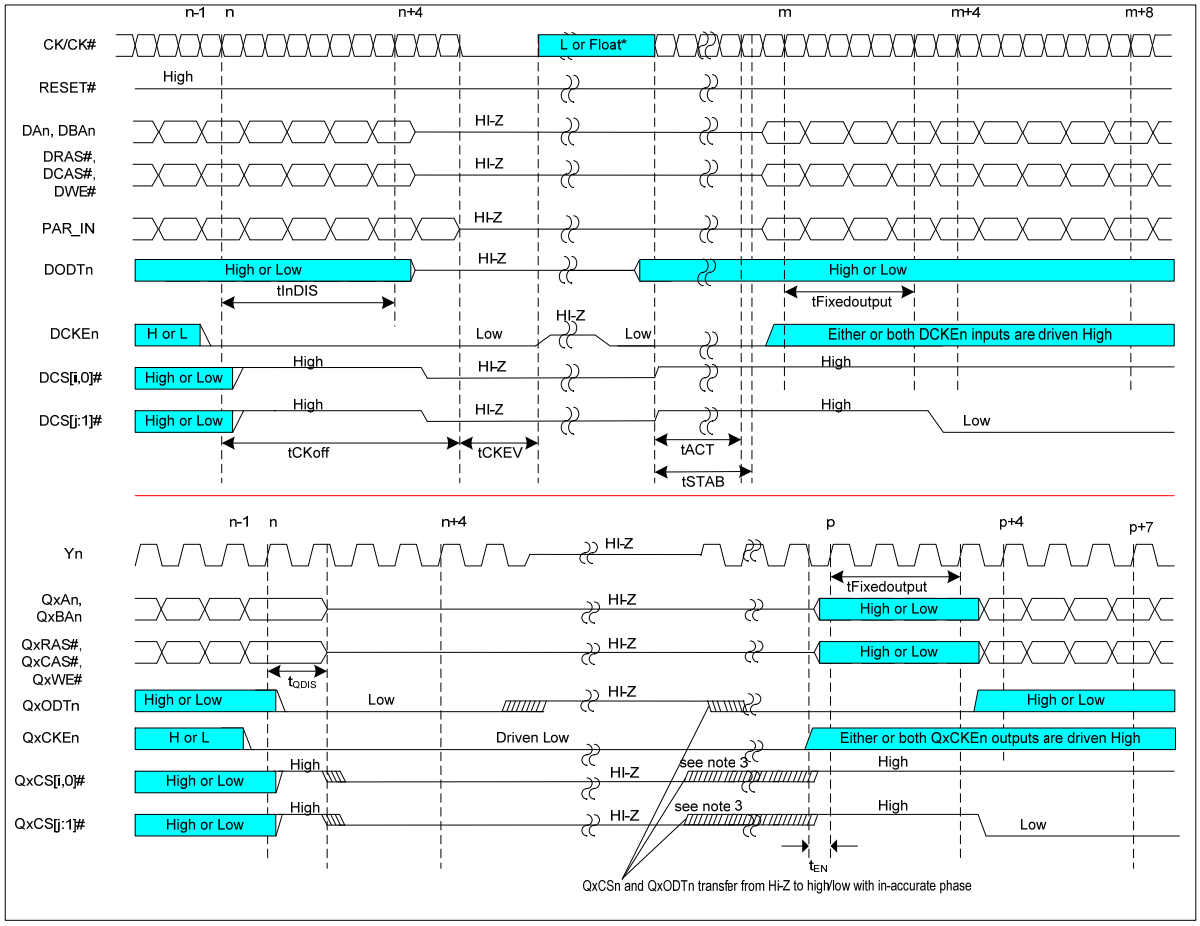
To enter Clock Stopped Power Down mode, the register will first enter CKE power down mode. Once in CKE power down mode, DCKEn will continue being deasserted for a minimum of one t_{CKoff} before pulling CK and CK# LOW. After holding CK and CK# LOW ($V_{IL(static)}$) for at least one t_{CKEV}, both CK and CK# can be floated (because of the (10 K-100 KΩ) pulldown resistor in the CK/CK# input buffer, CK/CK# will stay at LOW even though they are not being driven). The register is now in Clock Stopped Power Down mode. After CK and CK# are pulled LOW, DCKEn will remain LOW for at least one t_{CKEV} before it floats (if needed to float). At this point, all input receivers and input termination of the INSSTE32882LV are disabled. The only active input circuits are CK and CK#, which are required to detect the wake up request from the host.

Clock Stopped Power Down Mode Exit

To wake up the register after entering Clock Stopped Power Down, the register inputs DCS[n:0]# must be driven to HIGH (to prevent accidental access to the control registers), and DCKEn to LOW. After that, a frequency and phase accurate input clock signal must be applied. Within $t_{ACT,}$ after CK and CK# resumes normal operation, the INSSTE32882LV outputs start becoming a function of their corresponding inputs. The state of the DCS[n:0]# inputs must not be changed before the end of t_{STAB}. The input clock CK and CK# must be stable for a time equal or greater than t_{STAB} before any access to the INSSTE32882LV can take place.

Clock Stopped Power Down Mode (cont'd.)

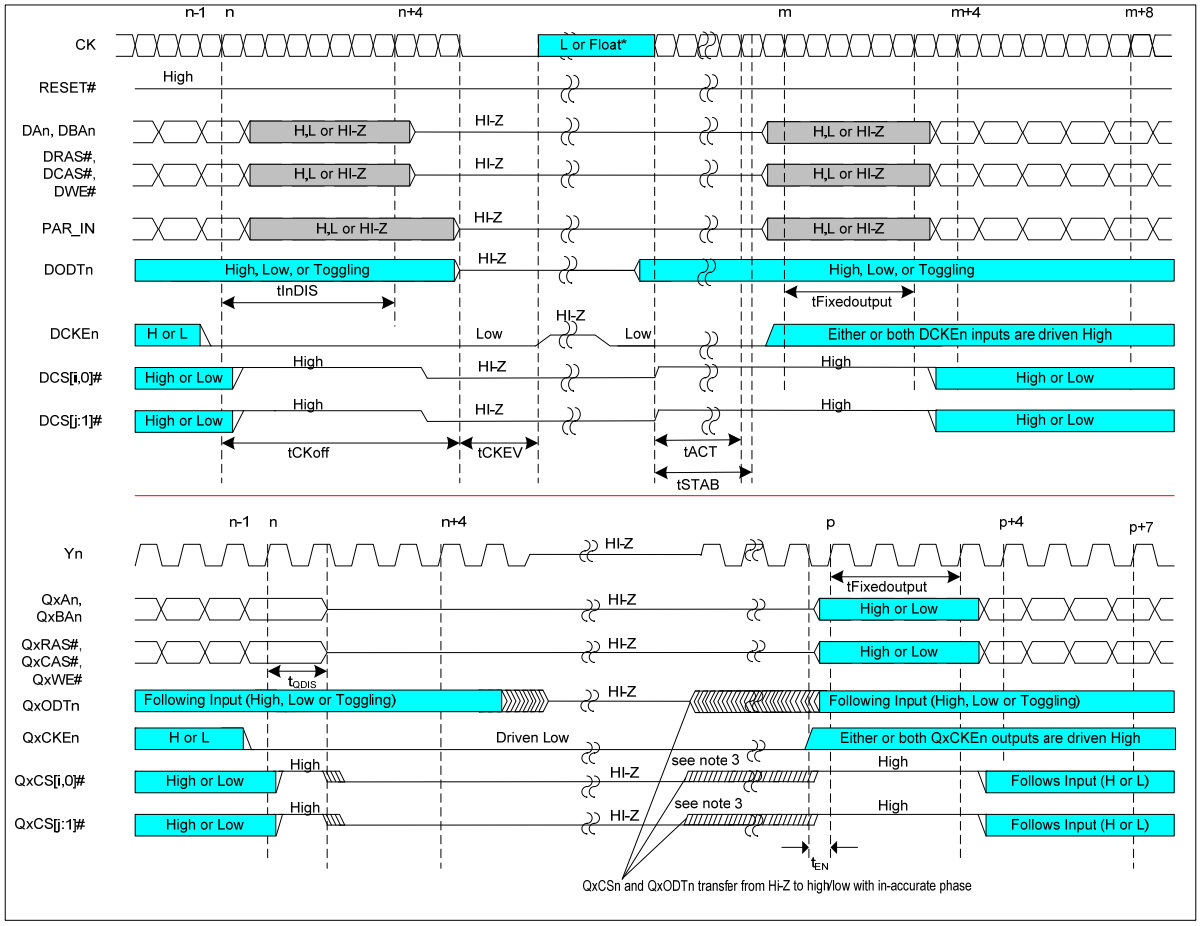
Figure 11. Clock Stopped Power Down Entry and Exit with IBT Off



(1) i, j only apply for QuadCS capable register. When QuadCS is enabled, i = 2, j = 3
(2) With RC9[DBA0]='1'
(3) When CK/CK# inputs are floated, CK/CK# inputs are pulled LOW by the (10 K-100 KΩ) pulldown resistor in the CK/CK# input buffer.
(4) Upon CKE Power Down exit, QxCSn# will be held HIGH for maximum of 1 tCK regardless of what DCSn# input level is. For all other operation QxCSn# outputs will follow DCSn# inputs.

Clock Stopped Power Down Mode (cont'd.)

Figure 12. Clock Stopped Power Down Entry and Exit with IBT On

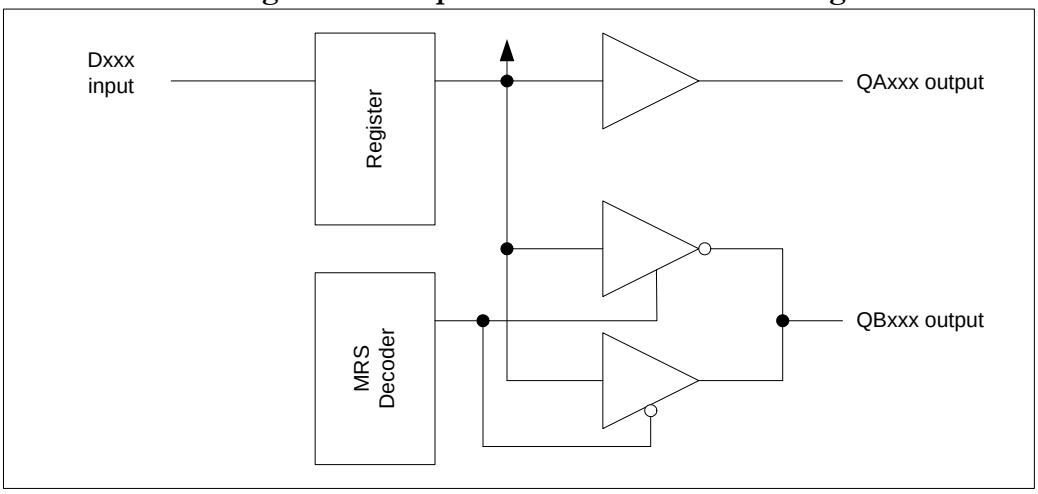


(1) i, j only apply for QuadCS capable register. When QuadCS is enabled, i = 2, j = 3
(2) With RC9[DBA0]='0'
(3) When CK/CK# inputs are floated, CK/CK# inputs are pulled LOW by the (10 K-100 KΩ) pulldown resistor in the CK/CK# input buffer.
(4) Upon CKE Power Down exit, QxCSn# will be held HIGH for maximum of 1 tCK regardless of what DCSn# input level is. For all other operation QxCSn# outputs will follow DCSn# inputs.

Dynamic 1T/3T Timing Transaction and Output Inversion Enabling/Disabling

Output Inversion is always enabled by default, after RESET# is de-asserted, to conserve power and reduce simultaneous output switching current. All A-outputs will follow the equivalent inputs; however the following B-outputs will be driven to the complement of the matching A-outputs: QBA3 - QBA9, QBA11, QBA13 - QBA15, QBBA0 - QBBA2.

Figure 13. Output Inversion Functional Diagram



The Output Inversion feature is not used during DRAM MRS Command access. When Output Inversion is disabled, all corresponding A and B output drivers of the INSSTE32882LV are driven to the same logic levels. Output Inversion must be disabled when the MRS and EMRS commands must be issued to the DRAMs, for example, to assure that the same programming is issued to all DRAMs in a rank.

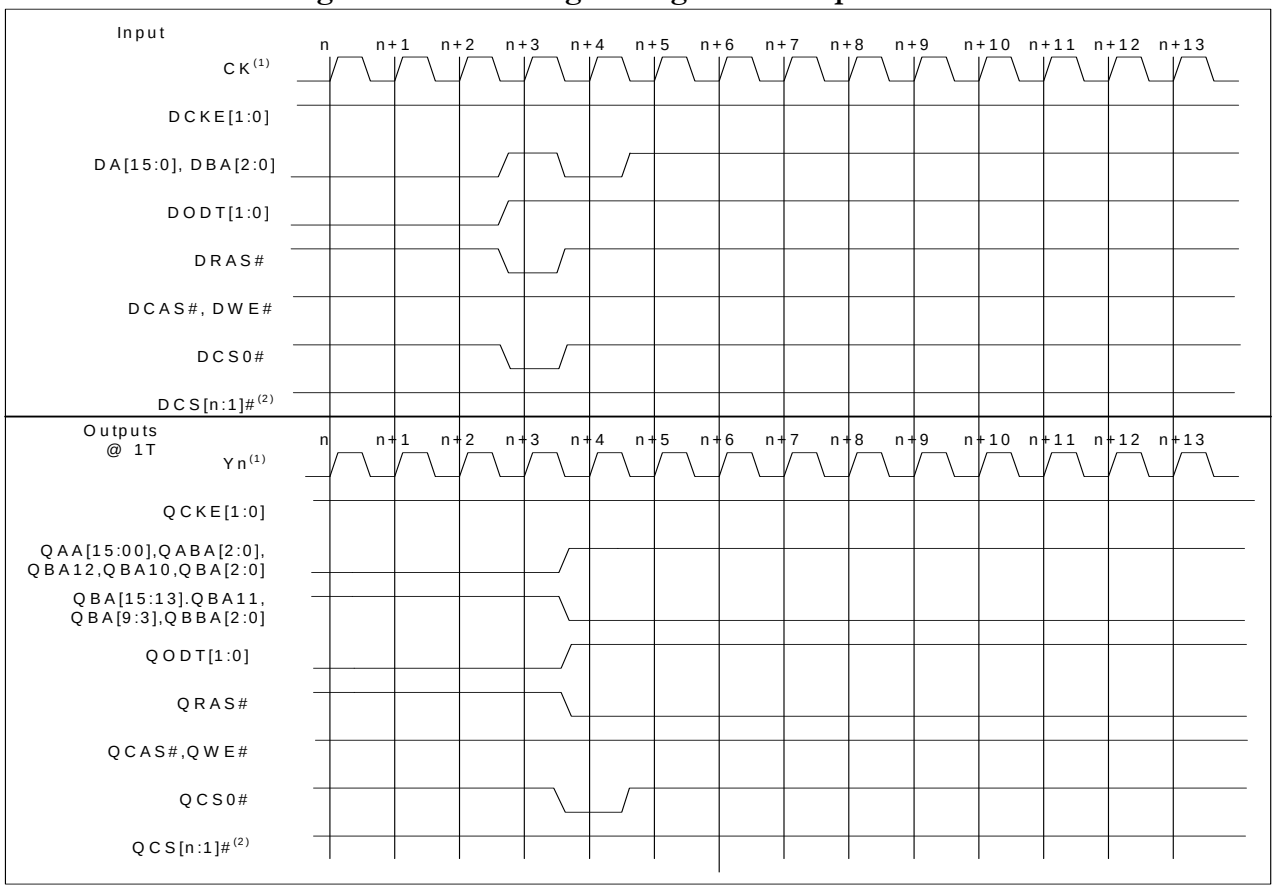
With Output Inversion disabled during MRS access, in order to allow correct DRAM accesses with the consequently increased simultaneous switching propagation delay the devices supports 3T timing. If this feature is invoked the device drives the received data on its outputs for three cycles instead of one. The only exception are the QxCS[n:0]# outputs, which are the QACS0#, QACS1#, QBCS0# and QBCS1# outputs in the QuadCS disabled mode and are QCS[3:0]# in the QuadCS enabled mode.

When the device decodes the MRS command (DRAS#=0, DCAS#=0, DWE=0 and only one DCSn#=0), it will disable the Output Inversion function and pass the DRAM MRS command with an additional (one) clock delay on the appropriate QxCSn# signal to the DRAM. Back-to-back MRS command via the INSSTE32882LV must have a minimum of three clock delays. The INSSTE32882LV will automatically enable Output Inversion if there are no DRAM MRS Commands three clocks after the previous MRS command.

The inputs and outputs relationships for 1T timing and 3T timing are shown in Figure 14, Figure 15 and Figure 16.

Dynamic 1T/3T Timing Transaction and Output Inversion Enabling/Disabling (cont'd.)

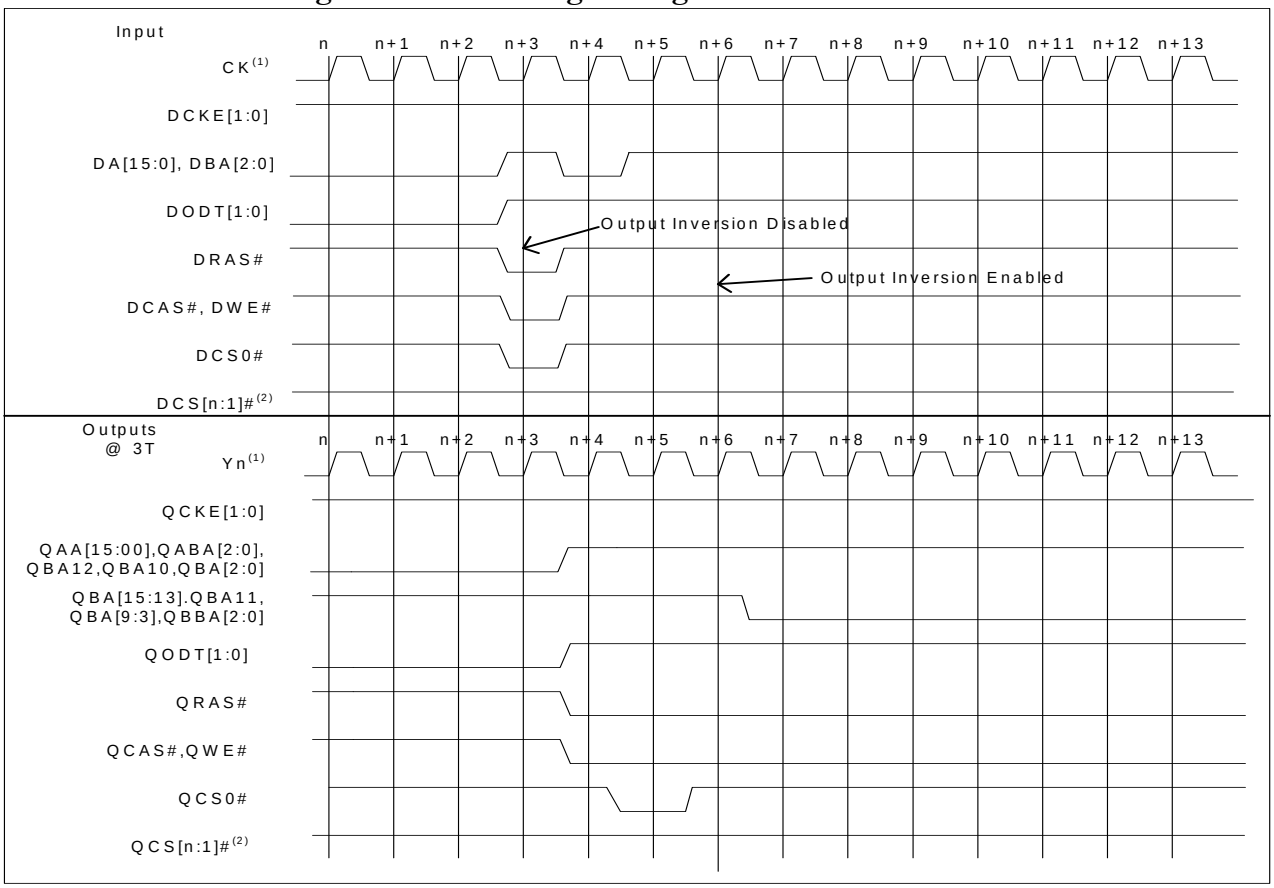
Figure 14. 1T Timing During Normal Operation



(1) CK# and Yn# left out for better visibility
(2) n=1 for QuadCS disabled, n=3 for QuadCS enabled

Dynamic 1T/3T Timing Transaction and Output Inversion Enabling/Disabling (cont'd.)

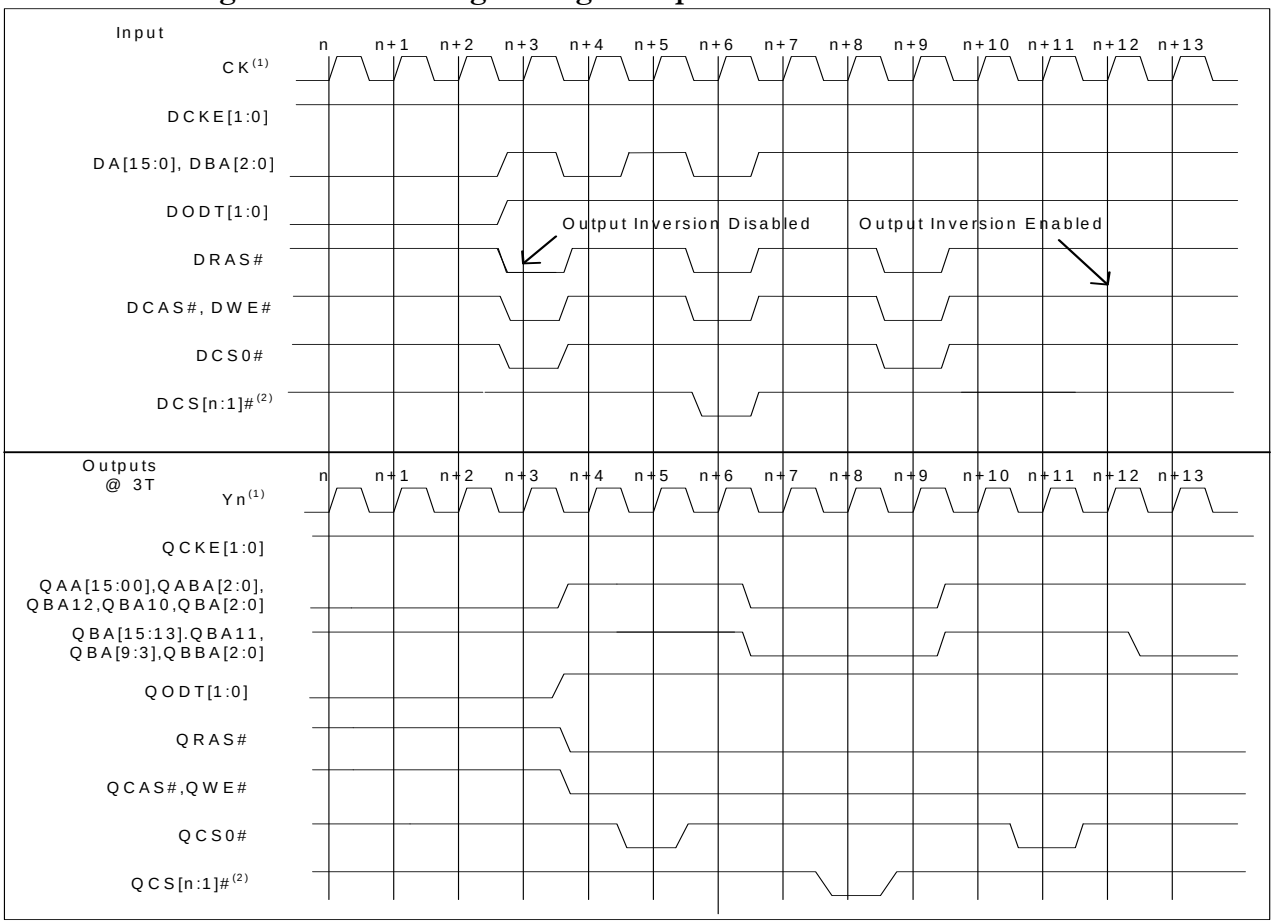
Figure 15. 3T Timing During DRAM MRS Command



(1) CK# and Yn# left out for better visibility
(2) n=1 for QuadCS disabled, n=3 for QuadCS enabled

Dynamic 1T/3T Timing Transaction and Output Inversion Enabling/Disabling (cont'd.)

Figure 16. 3T Timing During Multiple DRAM MRS Commands



(1) CK# and Yn# left out for better visibility
(2) n=1 for QuadCS disabled, n=3 for QuadCS enabled

Control Words

The INSSTE32882LV registers have internal control bits for adapting the configuration of certain device features. The control bits are accessed by the simultaneous assertion of both DCS0# and DCS1# in the QuadCS disabled mode. In the QuadCS enable mode, the simultaneous assertion of both DCS2# and DCS3# during normal operation, and the assertion of all four DCS[3:0]# inputs also result in control word access. However, assertion of any three DCS[3:0]# inputs is not legal. Register Qn outputs including QxCKE0, QxCKE1, QxODT0 and QxODT1 remain in their previous state. Select signals QxCS[n:0]# are set to HIGH during control word access.

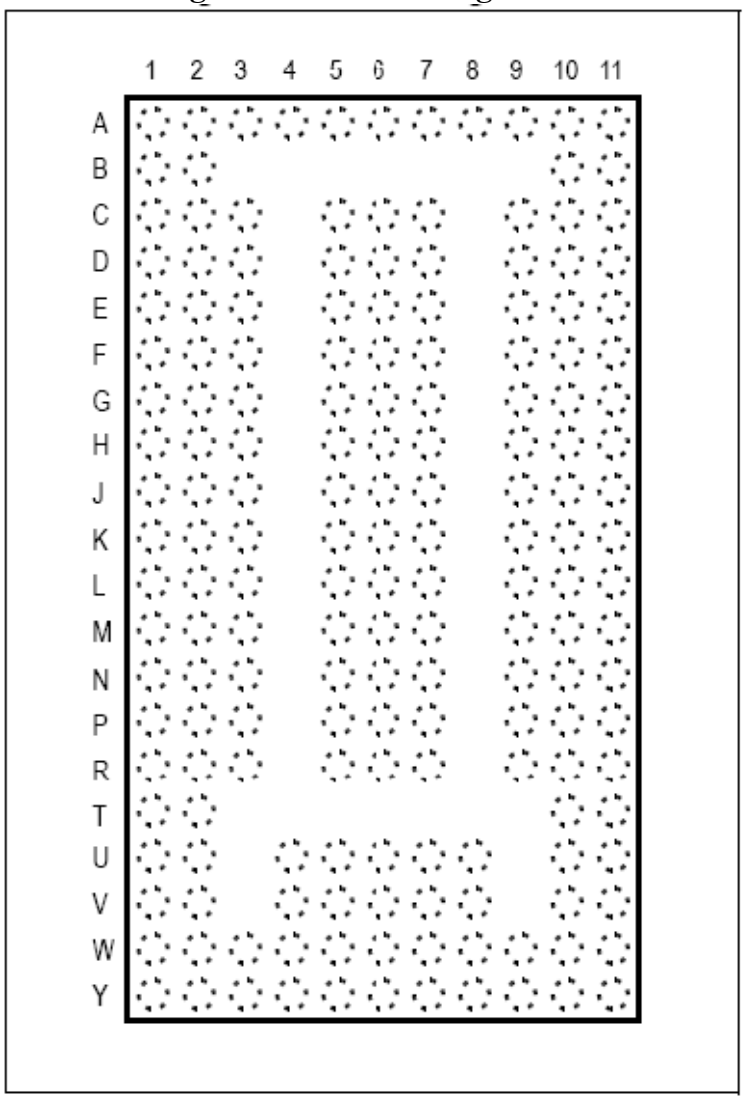
The INSSTE32882LV allocates decoding for up to 16 words of control bits, RC0 through RC15. Selection of each word of control bits is presented on inputs DA0 through DA2 and DBA2. Data to be written into the configuration registers need to be presented on DA3, DA4, DBA0 and DBA1. Bits DA[15:5] must be LOW and at least one DCKEn input must be HIGH for a valid access. During control word write, at least one DCKEn must be asserted. If register CKE power down mode is disabled, DCKEn input is a don't care (either HIGH or LOW). The inputs on DRAS#, DCAS#, DWE# and DODT[1:0] can be either HIGH or LOW and are ignored by the register during control word access. In all cases address and command parity is checked during control word write operations. ERROUT# is asserted and the command is ignored if a parity error is detected. Using this mechanism, controllers may use the INSSTE32882LV to validate the address and command bus signal integrity to the module as long as one or more of the parity checked input signals DA3..DA15, DBA0, DBA1, DRAS#, DCAS#, DWE# are kept HIGH.

Control word access must be possible at any defined frequency independent of the current setting of RC2[DBA1] control registers.

Pinout Configuration

Package option includes 176-ball Thin-Profile Fine-Pitch BGA (TFBGA) with 0.65mm ball pitch, 11x20 grids, 8.0mm x 13.5mm. It is using mechanical outline MO-246F. The device pinout supports outputs on the outer two left and right columns to support easy DIMM signal routing. Corresponding inputs are placed in a way that two devices can be placed back to back for 4 Rank modules while the data inputs share the same vias. Each input and output is located close to an associated no ball position or on the outer two rows to allow low cost via technology combined with the small 0.65mm ball pitch.

Figure 17. Pinout Configuration



Pinout top view for 176-ball TFBGA (front configuration, QuadCS mode disabled)

176-ball, 11 × 20 grid, TOP VIEW

Table 5 - "Ball Assignment; MIRROR=LOW, QCSEN#=HIGH (or Float)," specifies the pinout for INSSTE32882LV-GS01 and INSSTE32882LV-GS02 in front configuration with QuadCS mode disabled. The device has symmetric pinout with inputs at the south side and outputs to east and west sides. This allows back-to-back mounting on both sides of the PCB if more than one device is needed.

Table 5 - Ball Assignment; MIRROR=LOW, QCSEN#=HIGH (or Float)

176 Ball BGA for Register											
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**
A	QAA13	QAA8	QCSEN#	VSS	RESET#	MIRROR	ERROUT#	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	QACS1#	VDD		VDD	VDD	VDD		VDD	QBCS1#	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	QAWE#	QACS0#	VDD		VDD	VDD	VDD		VDD	QBCS0#	QBWE#
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	QACAS#	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	QBCAS#
P	QARAS#	QAODT1	DA3		VSS	VSS	VSS		DA4	QBODT1	QBRAS#
R	DCKE1	DA14	DA15		DA5	RSVD	DA2		DA1	DA10	DODT1
T	DCKE0	DCS0#								DCS1#	DODT0
U	DA12	DBA2		Y1#	PVSS	PVDD	PVDD	Y0#		DA13	DCAS#
V	DA9	DA11		Y1	PVSS	PVSS	PVDD	Y0		DRAS#	DWE#
W	DA8	DA6	FBIN#	Y3#	AVSS	CK#	RSVD	Y2#	FBOUT#	DA0	DBA0
Y	DA7	RSVD	FBIN	Y3	AVDD	CK	VREFCA	Y2	FBOUT	PAR_IN	DBA1

Pins A9 and W7 are reserved for future functions and must not be connected on system
Pin Y2 and R6 are reserved for DCS2# and DCS3# in QuadCS mode and must not be connected on system
Blank space indicate no ball is populated at that grid point -- vias on the module may be located in these areas

Pinout top view for 176-ball TFBGA (back configuration, QuadCS mode disabled)

Table 6 - "Ball Assignment; MIRROR=HIGH, QCSEN#=HIGH (or Float)," specifies the pinout for INSSTE32882LV-GS01 and INSSTE32882LV-GS02 in back configuration with QuadCS mode disabled.

Table 6 - Ball Assignment; MIRROR=HIGH, QCSEN#=HIGH (or Float)

176 Ball BGA for Register											
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**
A	QAA13	QAA8	QCSEN#	VSS	RESET#	MIRROR	ERROUT#	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	QACS1#	VDD		VDD	VDD	VDD		VDD	QBCS1#	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	QAWE#	QACS0#	VDD		VDD	VDD	VDD		VDD	QBCS0#	QBWE#
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	QACAS#	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	QBCAS#
P	QARAS#	QAODT1	DA4		VSS	VSS	VSS		DA3	QBODT1	QBRAS#
R	DODT1	DA10	DA1		DA2	RSVD	DA5		DA15	DA14	DCKE1
T	DODT0	DCS1#								DCS0#	DCKE0
U	DCAS#	DA13		Y1#	PVSS	PVDD	PVDD	Y0#		DBA2	DA12
V	DWE#	DRAS#		Y1	PVSS	PVSS	PVDD	Y0		DA11	DA9
W	DBA0	DA0	FBIN#	Y3#	AVSS	CK#	RSVD	Y2#	FBOUT#	DA6	DA8
Y	DBA1	PAR_IN	FBIN	Y3	AVDD	CK	VREFCA	Y2	FBOUT	RSVD	DA7

Pins A9 and W7 are reserved for future functions and must not be connected on the system.
Pins Y10 and R6 are reserved for DCS2# and DCS3# in QuadCS mode and must not be connected on the system.
Blank space indicates no ball is populated at that grid point -- vias on the module may be located in these areas.

Pinout top view for 176-ball TFBGA (front configuration, QuadCS mode enabled)

Table 7 - "Ball Assignment; MIRROR=LOW, QCSEN#=LOW," specifies the pinout for INSSTE32882LV-GS01 and INSSTE32882LV-GS02 in front configuration with QuadCS mode enabled.

Table 7 - Ball Assignment; MIRROR=LOW, QCSEN#=LOW

176 Ball BGA for Register											
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**
A	QAA13	QAA8	QCSEN#	VSS	RESET#	MIRROR	ERROUT#	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	QCS1#	VDD		VDD	VDD	VDD		VDD	QCS3#	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	QAWE#	QCS0#	VDD		VDD	VDD	VDD		VDD	QCS2#	QBWE#
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	QACAS#	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	QBCAS#
P	QARAS#	QAODT1	DA3		VSS	VSS	VSS		DA4	QBODT1	QBRAS#
R	DCKE1	DA14	DA15		DA5	DCS3#	DA2		DA1	DA10	DODT1
T	DCKE0	DCS0#								DCS1#	DODT0
U	DA12	DBA2		Y1#	PVSS	PVDD	PVDD	Y0#		DA13	DCAS#
V	DA9	DA11		Y1	PVSS	PVSS	PVDD	Y0		DRAS#	DWE#
W	DA8	DA6	FBIN#	Y3#	AVSS	CK#	RSVD	Y2#	FBOUT#	DA0	DBA0
Y	DA7	DCS2#	FBIN	Y3	AVDD	CK	VREFCA	Y2	FBOUT	PAR_IN	DBA1

Pins A9 and W7 are reserved for future functions -- must not be connected on the system
Blank space indicate no ball is populated at that grid point -- vias on the module may be located in these areas

Pinout top view for 176-ball TFBGA (back configuration, QuadCS mode enabled)

Table 8 - "Ball Assignment; MIRROR=HIGH, QCSEN#=LOW," specifies the pinout for INSSTE32882LV-GS02 in back configuration with QuadCS mode enabled.

Table 8 - Ball Assignment; MIRROR=HIGH, QCSEN#=LOW

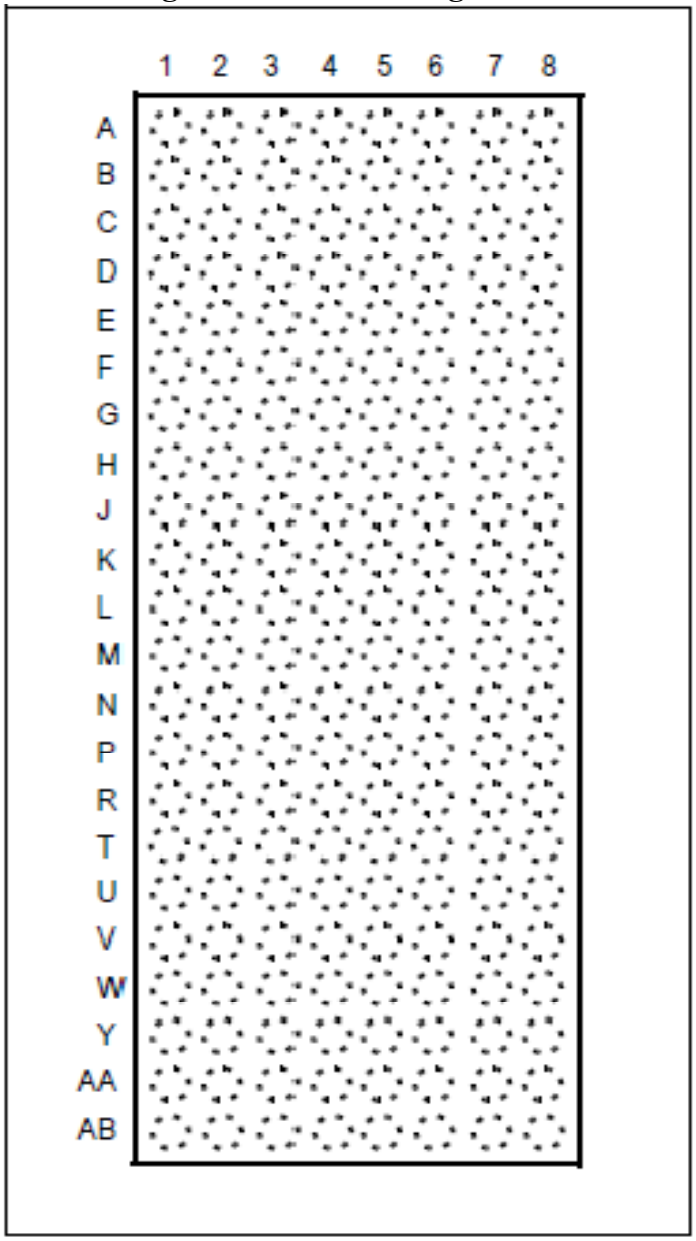
176 Ball BGA for Register											
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**
A	QAA13	QAA8	QCSEN#	VSS	RESET#	MIRROR	ERROUT#	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	QCS1#	VDD		VDD	VDD	VDD		VDD	QCS3#	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	QAWE#	QCS0#	VDD		VDD	VDD	VDD		VDD	QCS2#	QBWE#
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	QACAS#	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	QBCAS#
P	QARAS#	QAODT1	DA4		VSS	VSS	VSS		DA3	QBODT1	QBRAS#
R	DODT1	DA10	DA1		DA2	DCS3#	DA5		DA15	DA14	DCKE1
T	DODT0	DCS1#								DCS0#	DCKE0
U	DCAS#	DA13		Y1#	PVSS	PVDD	PVDD	Y0#		DBA2	DA12
V	DWE#	DRAS#		Y1	PVSS	PVSS	PVDD	Y0		DA11	DA9
W	DBA0	DA0	FBIN#	Y3#	AVSS	CK#	RSVD	Y2#	FBOUT#	DA6	DA8
Y	DBA1	PAR_IN	FBIN	Y3	AVDD	CK	VREFCA	Y2	FBOUT	DCS2#	DA7

Pins A9 and W7 are reserved for future functions -- must not be connected on the system
Blank space indicate no ball is populated at that grid point -- vias on the module may be located in these areas

Pinout configuration for Narrow Package

Package option includes 176-ball Thin-Profile Fine-Pitch BGA (TFBGA) with 0.65mm ball pitch, 8x22 grids, 6.0mm x 15.0mm. It is using the mechanical outline MO-246B. Equivalent to the 11x20 grid configuration the device pinout supports outputs on the outer two left and right columns. Corresponding inputs are placed in a way that two devices can be placed back to back for 4 Rank modules while the data inputs share the same vias.

Figure 18. Pinout Configuration



Pinout top view for 176-ball TFBGA Narrow Package (front configuration, QuadCS mode disabled)

176-ball, 8 × 22 grid, TOP VIEW

Table 9 - "Ball Assignment; MIRROR=LOW, QCSEN#=HIGH (or Float)," specifies the pinout for INSSTE32882LV-GS02 in front configuration with QuadCS mode disabled. The device has symmetric pinout with inputs at the south side and outputs to east and west sides. This allows back-to-back mounting on both sides of the PCB if more than one device is needed.

Table 9 - Ball Assignment; MIRROR=LOW, QCSEN#=HIGH (or Float)

176 Ball BGA for Register								
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
A	QAA13	QAA8	QCSEN#	RESET#	ERROUT#	RSVD	QBA8	QBA13
B	QAA14	QAA7	VSS	VSS	MIRROR	VSS	QBA7	QBA14
C	QAA9	QAA6	VDD	VDD	VDD	VDD	QBA6	QBA9
D	QAA11	QAA5	VSS	VSS	VSS	VSS	QBA5	QBA11
E	QAA2	QAA4	VDD	VDD	VDD	VDD	QBA4	QBA2
F	QAA1	QAA3	VSS	VSS	VSS	VSS	QBA3	QBA1
G	QAA0	QABA1	VDD	VDD	VDD	VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS	VSS	VSS	VSS	QBBA0	QBA12
J	QABA2	QACS1#	VDD	VDD	VDD	VDD	QBCS1#	QBBA2
K	QAA15	QACKE0	VSS	VSS	VSS	VSS	QBCKE0	QBA15
L	QAWE#	QACS0#	VDD	VDD	VDD	VDD	QBCS0#	QBWE#
M	QAA10	QACKE1	VSS	VSS	VSS	VSS	QBCKE1	QBA10
N	QACAS#	QAODT0	VDD	VDD	VDD	VDD	QBODT0	QBCAS#
P	QARAS#	QAODT1	VSS	VSS	VSS	VSS	QBODT1	QBRAS#
R	DA14	DCKE1	VDD	VDD	VDD	VDD	DODT1	DA10
T	DCS0#	DCKE0	VSS	VSS	VSS	VSS	DODT0	DCS1#
U	DA12	DA3	Y1#	PVSS	PVDD	Y0#	DA4	DCAS#
V	DA5	DA9	Y1	PVSS	PVDD	Y0	DWE#	DA2
W	DA8	DA15	Y3#	PVSS	PVDD	Y2#	DA1	DBA0
Y	DA7	DBA2	Y3	AVSS	AVDD	Y2	DA13	DBA1
AA	DA11	RSVD	FBIN#	CK#	RSVD	FBOUT#	PAR_IN	DRAS#
AB	DA6	RSVD	FBIN	CK	VREFCA	FBOUT	RSVD	DA0

Pins A6, AA2, AA5, AB2, and AB7 are reserved for future functions and must not be connected on system. The system must provide a solder pad for these pins. The device design needs to tolerate floating on these pins. A3 may be left floating since it has an internal pull-up resistor.

Pinout top view for 176-ball TFBGA Narrow Package (back configuration, QuadCS mode disabled)

Table 10 - "Ball Assignment; MIRROR=HIGH, QCSEN#=HIGH (or Float)," specifies the pinout for INSSTE32882LV-GS02 in back configuration with QuadCS mode disabled.

Table 10 - Ball Assignment; MIRROR=HIGH, QCSEN#=HIGH (or Float)

176 Ball BGA for Register								
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
A	QAA13	QAA8	QCSEN#	RESET#	ERROUT#	RSVD	QBA8	QBA13
B	QAA14	QAA7	VSS	VSS	MIRROR	VSS	QBA7	QBA14
C	QAA9	QAA6	VDD	VDD	VDD	VDD	QBA6	QBA9
D	QAA11	QAA5	VSS	VSS	VSS	VSS	QBA5	QBA11
E	QAA2	QAA4	VDD	VDD	VDD	VDD	QBA4	QBA2
F	QAA1	QAA3	VSS	VSS	VSS	VSS	QBA3	QBA1
G	QAA0	QABA1	VDD	VDD	VDD	VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS	VSS	VSS	VSS	QBBA0	QBA12
J	QABA2	QACS1#	VDD	VDD	VDD	VDD	QBCS1#	QBBA2
K	QAA15	QACKE0	VSS	VSS	VSS	VSS	QBCKE0	QBA15
L	QAWE#	QACS0#	VDD	VDD	VDD	VDD	QBCS0#	QBWE#
M	QAA10	QACKE1	VSS	VSS	VSS	VSS	QBCKE1	QBA10
N	QACAS#	QAODT0	VDD	VDD	VDD	VDD	QBODT0	QBCAS#
P	QARAS#	QAODT1	VSS	VSS	VSS	VSS	QBODT1	QBRAS#
R	DA10	DODT1	VDD	VDD	VDD	VDD	DCKE1	DA14
T	DCS1#	DODT0	VSS	VSS	VSS	VSS	DCKE0	DCS0#
U	DCAS#	DA4	Y1#	PVSS	PVDD	Y0#	DA3	DA12
V	DA2	DWE#	Y1	PVSS	PVDD	Y0	DA9	DA5
W	DBA0	DA1	Y3#	PVSS	PVDD	Y2#	DA15	DA8
Y	DBA1	DA13	Y3	AVSS	AVDD	Y2	DBA2	DA7
AA	DRAS#	PAR_IN	FBIN#	CK#	RSVD	FBOUT#	RSVD	DA11
AB	DA0	RSVD	FBIN	CK	VREFCA	FBOUT	RSVD	DA6

Pins A6, AA5, AA7, AB2, and AB7 are reserved for future functions and must not be connected on system. The system must provide a solder pad for these pins. The device design needs to tolerate floating on these pins. A3 may be left floating since it has an internal pull-up resistor.

Pinout top view for 176-ball TFBGA Narrow Package (front configuration, QuadCS mode enabled)

Table 11 - "Ball Assignment; MIRROR=LOW, QCSEN#=LOW," specifies the pinout for INSSTE32882LV-GS02 in front configuration with QuadCS mode enabled.

Table 11 - Ball Assignment; MIRROR=LOW, QCSEN#=LOW

176 Ball BGA for Register								
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
A	QAA13	QAA8	QCSEN#	RESET#	ERROUT#	RSVD	QBA8	QBA13
B	QAA14	QAA7	VSS	VSS	MIRROR	VSS	QBA7	QBA14
C	QAA9	QAA6	VDD	VDD	VDD	VDD	QBA6	QBA9
D	QAA11	QAA5	VSS	VSS	VSS	VSS	QBA5	QBA11
E	QAA2	QAA4	VDD	VDD	VDD	VDD	QBA4	QBA2
F	QAA1	QAA3	VSS	VSS	VSS	VSS	QBA3	QBA1
G	QAA0	QABA1	VDD	VDD	VDD	VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS	VSS	VSS	VSS	QBBA0	QBA12
J	QABA2	QCS1#	VDD	VDD	VDD	VDD	QCS3#	QBBA2
K	QAA15	QACKE0	VSS	VSS	VSS	VSS	QBCKE0	QBA15
L	QAWE#	QCS0#	VDD	VDD	VDD	VDD	QCS2#	QBWE#
M	QAA10	QACKE1	VSS	VSS	VSS	VSS	QBCKE1	QBA10
N	QACAS#	QAODT0	VDD	VDD	VDD	VDD	QBODT0	QBCAS#
P	QARAS#	QAODT1	VSS	VSS	VSS	VSS	QBODT1	QBRAS#
R	DA14	DCKE1	VDD	VDD	VDD	VDD	DODT1	DA10
T	DCS0#	DCKE0	VSS	VSS	VSS	VSS	DODT0	DCS1#
U	DA12	DA3	Y1#	PVSS	PVDD	Y0#	DA4	DCAS#
V	DA5	DA9	Y1	PVSS	PVDD	Y0	DWE#	DA2
W	DA8	DA15	Y3#	PVSS	PVDD	Y2#	DA1	DBA0
Y	DA7	DBA2	Y3	AVSS	AVDD	Y2	DA13	DBA1
AA	DA11	DCS2#	FBIN#	CK#	RSVD	FBOUT#	PAR_IN	DRAS#
AB	DA6	RSVD	FBIN	CK	VREFCA	FBOUT	DCS3#	DA0

Pins A6, AA5, and AB2 are reserved for future functions and must not be connected on system.
The system must provide a solder pad for these pins. The device design needs to tolerate floating on these pins.
A3 may be left floating since it has an internal pull-up resistor.

Pinout top view for 176-ball TFBGA Narrow Package (back configuration, QuadCS mode enabled)

Table 12 - "Ball Assignment; MIRROR=HIGH, QCSEN#=LOW," specifies the pinout for INSSTE32882LV-GS02 in back configuration with QuadCS mode enabled.

Table 12 - Ball Assignment; MIRROR=HIGH, QCSEN#=LOW

176 Ball BGA for Register								
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
A	QAA13	QAA8	QCSEN#	RESET#	ERROUT#	RSVD	QBA8	QBA13
B	QAA14	QAA7	VSS	VSS	MIRROR	VSS	QBA7	QBA14
C	QAA9	QAA6	VDD	VDD	VDD	VDD	QBA6	QBA9
D	QAA11	QAA5	VSS	VSS	VSS	VSS	QBA5	QBA11
E	QAA2	QAA4	VDD	VDD	VDD	VDD	QBA4	QBA2
F	QAA1	QAA3	VSS	VSS	VSS	VSS	QBA3	QBA1
G	QAA0	QABA1	VDD	VDD	VDD	VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS	VSS	VSS	VSS	QBBA0	QBA12
J	QABA2	QCS1#	VDD	VDD	VDD	VDD	QCS3#	QBBA2
K	QAA15	QACKE0	VSS	VSS	VSS	VSS	QBCKE0	QBA15
L	QAWE#	QCS0#	VDD	VDD	VDD	VDD	QCS2#	QBWE#
M	QAA10	QACKE1	VSS	VSS	VSS	VSS	QBCKE1	QBA10
N	QACAS#	QAODT0	VDD	VDD	VDD	VDD	QBODT0	QBCAS#
P	QARAS#	QAODT1	VSS	VSS	VSS	VSS	QBODT1	QBRAS#
R	DA10	DODT1	VDD	VDD	VDD	VDD	DCKE1	DA14
T	DCS1#	DODT0	VSS	VSS	VSS	VSS	DCKE0	DCS0#
U	DCAS#	DA4	Y1#	PVSS	PVDD	Y0#	DA3	DA12
V	DA2	DWE#	Y1	PVSS	PVDD	Y0	DA9	DA5
W	DBA0	DA1	Y3#	PVSS	PVDD	Y2#	DA15	DA8
Y	DBA1	DA13	Y3	AVSS	AVDD	Y2	DBA2	DA7
AA	DRAS#	PAR_IN	FBIN#	CK#	RSVD	FBOUT#	DCS2#	DA11
AB	DA0	RSVD	FBIN	CK	VREFCA	FBOUT	DCS3#	DA6

Pins A6, AA5, and AB2 are reserved for future functions and must not be connected on system.
The system must provide a solder pad for these pins. The device design needs to tolerate floating on these pins.
A3 may be left floating since it has an internal pull-up resistor.

Terminal Functions

Table 13

Signal Group	Terminal Name	Description	Electrical Characteristics
Ungated inputs	DCKE[1:0], DODT[1:0]	DRAM corresponding register function pins not associated with Chip Selects.	1.5 V/1.35 V CMOS[1]
Chip Select gated inputs	DA0...DA15, DBA0...DBA2, DRAS#, DCAS#, DWE#	DRAM corresponding register inputs, re-driven only when either chip select is LOW. If both chip selects are LOW the register maintains the state of the previous input clock cycle at its outputs	1.5 V/1.35 V CMOS[1]
Chip Select Inputs	DCS0#, DCS1#	DRAM corresponding register Chip Select signals. These pins initiate DRAM address/command decodes, and as such exactly one will be LOW when a valid address/command is present which should be re- driven.	1.5 V/1.35 V CMOS[1]
	DCS2#, DCS3#	DRAM corresponding register Chip Select signals when QuadCS mode is enabled. DCS2# and DCS3# inputs are disabled when QuadCS mode is disabled.	1.5 V/1.35 V CMOS[1]
Re-driven Outputs	QxA0..QxA15, QxBA0..QxBA2, QxCS0[1:0]#, QxCKE[1:0], QxODT[1:0], QxRAS#, QxCAS#, QxWE#	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock; x is A or B; Outputs are grouped as A or B and may be enabled or disabled via RC0.	1.5 V/1.35 V CMOS[2]
Parity input	PAR_IN	Input parity is received on pin PAR_IN and should maintain parity across the Chip Select Gated inputs (see above), at the rising edge of the input clock, one input clock cycle after corresponding data and one or both chip selects are LOW.	1.5 V/1.35 V CMOS[1]
Parity error output	ERROUT#	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs. ERROUT# will be active for two clock cycles, and delayed by 3 clock cycles to the corresponding input data.	Open-drain
Clock Inputs	CK, CK#	Differential master clock input pair to the PLL; weak internal pull-down resitors (10KΩ~100KΩ).	1.5 V/1.35 V CMOS[1]
Clock Outputs	Y0, Y0#… Y3, Y3#	Re-driven clock	1.5 V/1.35 V CMOS
Misc. Inputs	RESET#	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float. Once RESET# becomes HIGH the outputs get enabled and are driven LOW until the first access has been performed. RESET# also resets the ERROUT# signal.	CMOS[3]
	MIRROR	Selects between two different ball-outs for front or back operation. When the MIRROR input is HIGH, the device input bus termination (IBT) is turned off on all inputs, except the DCSn# and DODTn inputs.	CMOS[3]

Notes:
1. 1.5 V/1.35 V CMOS inputs use VREFCA as the switching point reference for these receivers.
2. These outputs are optimized for memory applications to drive DRAM inputs to 1.5 V or 1.35 V signaling levels
3. Voltage levels according standard JESD8-11A, wide range, non terminated logic

Terminal Functions (cont'd.)

Table 13 (cont'd.)

Signal Group	Terminal Name	Description	Electrical Characteristics
Misc. Inputs	QCSEN#	Enables the QuadCS mode. The QCSEN# input has a weak internal pull-up resistor (10 KΩ ~ 100 KΩ)	CMOS[2]
	VREFCA[1]	Input reference voltage for SSTL_15 inputs.	VDD/2
	VDD	Power supply voltage	Power Input
	VSS	Ground	Ground Input
	AVDD	Analog supply voltage	Analog Power
	AVSS	Analog Ground	Analog Ground
	PVDD	Clock logic and clock output driver power supply	Clock Driver Output Power
	PVSS	Clock logic and clock output driver ground	Clock Driver Output Ground
	RSVD	Reserved pins, must be left floating	I/O

Notes:
1. 1.5 V/1.35 V CMOS inputs use VREFCA as the switching point reference for these receivers.
2. Voltage levels according to standard JESD8-11A, wide range, non-terminated logic.

Function Tables

Table 14 -- Function table (each flip flop) with QuadCS mode disabled

Inputs								Outputs		
RESET#	**DCS[1:0]#**	**CK[1]**	**CK#[1]**	**ADDR[2]**	**CMD[3]**	**CTRL[4]**	**Qn**	**QxCS[1:0]#**	**QxODTn**	**QxCKEn**
H	LL	↑	↓	Control Word	Control Word	Control Word	No Change	HH	No Change	No Change
H	XX	L or H	H or L	X	X	X	No Change	No Change	No Change	No Change
H	LH	↑	↓	X	X	X	Follows Inputs	LH	Follows Inputs	Follows Inputs
H	XX	L	L	X	X	X	Float	Float	Float	L
H	HL	↑	↓	X	X	X	Follows Inputs	HL	Follows Inputs	Follows Inputs
H	HH	↑	↓	X or Float	X or Float	X	No Change or Float[5]	HH	Follows Inputs	Follows Inputs
L	X or Float	X or Float	X or Float	X or Float	X or Float	X or Float	Float	Float	Float	L

Notes:
1. It is illegal to hold both the CK and CK# inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when RESET# is driven HIGH.
2. ADDR = DA[15:0], DBA[2:0]
3. CMD = DRAS#, DCAS#, DWE#
4. CTRL = DODTn, DCKEn
5. Depending on Control Word RC0 Bit DA4. If RC0[DA4] is cleared, previous state is maintained. Address floating is disabled independent of control word RC0 once 3T timing is activated

Function Tables (cont'd.)

Table 15 -- Function table (each flip flop) with QuadCS mode enabled

Inputs					Outputs			
RESET#	**DCS[3:0]#**	**CK[1]**	**CK#[1]**	**A/C/E[2]**	**Qn**	**QCS[3:0]#**	**QxODTn**	**QxCKEn**
H	LLHH	↑	↓	Control Word	No Change	HHHH	No Change	No Change
H	HHLL							
H	LLLL							
H	XXXX	L or H	H or L	X	No Change	No Change	No Change	No Change
H	LHHH	↑	↓	Dn	Dn	LHHH	DODTn	DCKEn
H	HLHH	↑	↓	Dn	Dn	HLHH	DODTn	DCKEn
H	HHLH	↑	↓	Dn	Dn	HHLH	DODTn	DCKEn
H	HHHL	↑	↓	Dn	Dn	HHHL	DODTn	DCKEn
H	LHLH	↑	↓	Dn	Dn	LHLH	DODTn	DCKEn
H	HLLH	↑	↓	Dn	Dn	HLLH	DODTn	DCKEn
H	LHHL	↑	↓	Dn	Dn	LHHL	DODTn	DCKEn
H	HLHL	↑	↓	Dn	Dn	HLHL	DODTn	DCKEn
H	XXXX	L	L	X	Float	Float	Float	L
H	HHHH	↑	↓	X	No Change or Float[3]	HHHH	DODTn	DCKEn
H	LLLH	↑	↓	X	Ilegal Input States			
H	LLHL							
H	LHLL							
H	HLLL							
L	X or Float	X or Float	X or Float	X or Float	Float	Float	Float	L

Notes:
1. It is illegal to hold both the CK and CK# inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when RESET# is driven HIGH.
2. A/C/E = DA0..DA15, DBA0..DBA2, DRAS#, DCAS#, DWE#, DODTn, DCKEn
3. Depending on Control Word RC0 Bit DA4. If RC0[DA4] is cleared, previous state is maintained. Address floating is disabled independent of control word RC0 once 3T timing is activated

Function Tables (cont'd.)

Table 16 -- Parity, low power and Standby function table with QuadCS mode disabled

Inputs						Outputs
RESET#	**DCS[1:0]#**	**CK[1]**	**CK#[1]**	**Σ of A/C[2]**	**PAR_IN[3]**	**ERROUT#[4]**
H	XL	↑	↓	Even	L	H
H	XL	↑	↓	Odd	L	L
H	XL	↑	↓	Even	H	L
H	XL	↑	↓	Odd	H	H
H	LX	↑	↓	Even	L	H
H	LX	↑	↓	Odd	L	L
H	LX	↑	↓	Even	H	L
H	LX	↑	↓	Odd	H	H
H	HH	↑	↓	X	X	H[5]
H	XX	L or H	H or L	X	X	ERROUT#n_0
H	XX	L	L	X	X	H[6]
L	X or Float	X or Float	X or Float	X or Float	X or Float	H

Notes:
1. It is illegal to hold both the CK and CK# inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when RESET# is driven HIGH.
2. A/C = DA0..DA15, DBA0..DBA2, DRAS#, DCAS#, DWE#. Inputs DCKE0, DCKE1, DODT0, DODT1, DCS[1:0]# are not included in this range. This column represents the sum of the number of A/C signals that are electrically HIGH.
3. PAR_IN arrives one clock cycle after data to which it applies, ERROUT# is issued 3 clock cycles after the failing data.
4. This transition assumes ERROUT# is HIGH at the crossing of CK going HIGH and CK# going LOW. If ERROUT# is LOW, it stays latched LOW for exactly two clock cycles or until RESET# is driven LOW.
5. Same 3 cycle delay for ERROUT# is valid for the de-select phase (see Figure 7)
6. The system is not allowed to pull CK and CK# LOW while ERROUT# is asserted.

Function Tables (cont'd.)

Table 17 -- Parity, low power and Standby function table with QuadCS mode enabled

Inputs						Outputs
RESET#	**DCS[3:0]#**	**CK[1]**	**CK#[1]**	**Σ of A/C[2]**	**PAR_IN[3]**	**ERROUT#[4]**
H	LXXX XLXX XXLX XXXL	↑	↓	Even	L	H
H	LXXX XLXX XXLX XXXL	↑	↓	Odd	L	L
H	LXXX XLXX XXLX XXXL	↑	↓	Even	H	L
H	LXXX XLXX XXLX XXXL	↑	↓	Odd	H	H
H	HHHH	↑	↓	X	X	H[5]
H	XXXX	L or H	H or L	X	X	ERROUT#n_0
H	XXXX	L	L	X	X	H[6]
L	X or Float	X or Float	X or Float	X or Float	X or Float	H

Notes:
1. It is illegal to hold both the CK and CK# inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when RESET# is driven HIGH.
2. A/C = DA0..DA15, DBA0..DBA2, DRAS#, DCAS#, DWE#. Inputs DCKE0, DCKE1, DODT0, DODT1, DCS[3:0]# are not included in this range. This column represents the sum of the number of A/C signals that are electrically HIGH.
3. PAR_IN arrives one clock cycle after data to which it applies, ERROUT# is issued 3 clock cycles after the failing data.
4. This transition assumes ERROUT# is HIGH at the crossing of CK going HIGH and CK# going LOW. If ERROUT# is LOW, it stays latched LOW for exactly two clock cycles or until RESET# is driven LOW.
5. Same 3 cycle delay for ERROUT# is valid for the de-select phase (see Figure 7)
6. The system is not allowed to pull CK and CK# LOW while ERROUT# is asserted.

Function Tables (cont'd.)

Table 18 -- PLL function table

Inputs					Outputs				
RESET#	**AVDD**	**OEn[1]**	**CK[2]**	**CK#[2]**	**Yn**	**Yn#**	**FBOUT**	**FBOUT#**	**PLL**
L	X	X	X	X	Float	Float	Float	Float	Off
H	V_{DD} nominal	L	L	H	L	H	L	H	On
H	V_{DD} nominal	L	H	L	H	L	H	L	On
H	V_{DD} nominal	H	L	H	Float	Float	L	H	On
H	V_{DD} nominal	H	H	L	Float	Float	H	L	On
H	V_{DD} nominal	X	L	L	Float	Float	Float	Float	Off
H	GND[3]	L	L	H	L	H	L	H	Bypass/Off
H	GND[4]	L	H	L	H	L	H	L	Bypass/Off
H	GND[5]	H	L	H	Float	Float	L	H	Bypass/Off
H	GND[6]	H	H	L	Float	Float	H	L	Bypass/Off
H	GND[7]	X	L	L	Float	Float	Float	Float	Bypass/Off
H	X	X	H	H	Reserved				

Notes:
1. The Output Enable (OEn) to disable the output buffer is not an input signal to the INSSTE32882LV, but an internal signal from the PLL power down control and test logic. It is controlled by setting or clearing the corresponding bit in the Clock Driver mode register.
2. It is illegal to hold both the CK and CK# inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when RESET# is driven HIGH.
3. This is a device test mode and all register timing parameter are not guaranteed.

Control Words

The device features a set of control words, which allow the optimization of the device properties for different raw card designs. The different control words and settings are described below. Any change to these control words require some time for the device to settle. For changes to the control word setting, except for RC2 (bit DBA1 and DA3), the controller needs to wait tMRD after the last control word access, before further access to the DRAM can take place. For any changes to the clock timing (RC2: bit DBA1 and DA3) this settling may take up to tSTAB time. All chip select inputs, DCS[n:0]#, must be kept HIGH during that time. The Control Words can be accessed and written to when running within any one defined frequency band.

Control Word Decoding

The values to be programmed into each control word are presented on signals DA3, DA4, DBA0 and DBA1 simultaneously with the assertion of the control word access through DCS0# and DCS1#, or DCS2# and DCS3# in the QuadCS enabled mode, and the address of the control word on DA0, DA1, DA2 and DBA2.

The reset default state of Control Words 0 .. 15 is "0". Every time the device is reset, its default state is restored. Stopping the clocks (CK=CK#=LOW) to put the device in low-power mode will not alter the control word settings.

Table 19 – Control Word Decoding with QuadCS mode disabled

		Signal					
Control Word	**Symbol**	**DCS[1:0]#**	**DBA2**	**DA2**	**DA1**	**DA0**	**Meaning**
None	n/a	HX	X	X	X	X	No control word access
None	n/a	XH	X	X	X	X	
Control word 0	RC0	LL	L	L	L	L	Global Features Control Word
Control word 1	RC1		L	L	L	H	Clock Driver Enable Control Word
Control word 2	RC2		L	L	H	L	Timing Control Word
Control word 3	RC3		L	L	H	H	CA Signals Driver Characteristics Control Word
Control word 4	RC4		L	H	L	L	Control Signals Driver Characteristics Control Word
Control word 5	RC5		L	H	L	H	CK Driver Characteristics Control Word
Control word 6	RC6		L	H	H	L	Inphi specific
Control word 7	RC7		L	H	H	H	Inphi specific
Control word 8	RC8		H	L	L	L	Additional IBT Settings Control Word
Control word 9	RC9		H	L	L	H	Power Saving Settings Control Word
Control word 10	RC10		H	L	H	L	Encoding for RDIMM Operating Speed Control Word
Control word 11	RC11		H	L	H	H	Encoding for RDIMM Operating V_{DD} Control Word
Control word 12	RC12		H	H	L	L	Reserved for future use
Control word 13	RC13		H	H	L	H	Reserved for future use
Control word 14	RC14		H	H	H	L	Reserved for future use
Control word 15	RC15		H	H	H	H	Reserved for future use

Control Word Decoding (cont'd.)

Table 20 – Control Word Decoding with QuadCS mode enabled

		Signal					
Control Word	**Symbol**	**DCS[3:0]#**	**DBA2**	**DA2**	**DA1**	**DA0**	**Meaning**
None	n/a	HXHX	X	X	X	X	No control word access
None	n/a	HXXH	X	X	X	X	
None	n/a	XHHX	X	X	X	X	
None	n/a	XHXH	X	X	X	X	
None	n/a	HLLL	X	X	X	X	Illegal Input States
None	n/a	LHLL	X	X	X	X	
None	n/a	LLHL	X	X	X	X	
None	n/a	LLLH	X	X	X	X	
Control word 0	RC0	LLHH Or HHLL Or LLLL	L	L	L	L	Global Features Control Word
Control word 1	RC1		L	L	L	H	Clock Driver Enable Control Word
Control word 2	RC2		L	L	H	L	Timing Control Word
Control word 3	RC3		L	L	H	H	CA Signals Driver Characteristics Control Word
Control word 4	RC4		L	H	L	L	Control Signals Driver Characteristics Control Word
Control word 5	RC5		L	H	L	H	CK Driver Characteristics Control Word
Control word 6	RC6		L	H	H	L	Inphi specific
Control word 7	RC7		L	H	H	H	Inphi specific
Control word 8	RC8		H	L	L	L	Additional IBT Settings Control Word
Control word 9	RC9		H	L	L	H	Power Saving SettingsControl Word
Control word 10	RC10		H	L	H	L	Encoding for RDIMM Operating Speed Control Word
Control word 11	RC11		H	L	H	H	Encoding for RDIMM Operating V_{DD} Control Word
Control word 12	RC12		H	H	L	L	Reserved for future use
Control word 13	RC13		H	H	L	H	Reserved for future use
Control word 14	RC14		H	H	H	L	Reserved for future use
Control word 15	RC15		H	H	H	H	Reserved for future use

Control Word Decoding (cont'd.)

The following sections describe the contents of each control word.

Table 21 – RC0: Global Features Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
X	X	X	0	Output inversion	Output inversion enabled
X	X	X	1		Output inversion disabled
X	X	0	X	Float outputs (when DCSn# = HIGH, and DA4 = "1")	Float disabled (normal output drive strength as defined in RC3, 4, and 5)
X	X	1	X		Float enabled (or Weak Drive mode when RC9 [DA3]=1)
X	0	X	X	A outputs disabled (including Y1/Y1# and Y3/Y3#)	A outputs enabled
X	1	X	X		A outputs disabled
0	X	X	X	B outputs disabled (including Y0/Y0# and Y2/Y2#)	B outputs enabled
1	X	X	X		B outputs disabled

Output floating refers to allowing many A/B outputs to enter a Hi-Z state when they are not being used. This is to conserve power when the outputs are resistively terminated to a voltage (e.g., VDD, VTT, or VSS). When output floating is enabled, the following outputs (on both matching A and B outputs) are Hi-Z when not actively driven: QxA0, QxA1, QxA2, QxA3, QxA4, QxA5, QxA6, QxA7, QxA8, QxA9, QxA10/AP, QxA11, QxA12/BC, QxA13, QxA14, QxA15, QxBA0, QxBA1, QxBA2, QxRAS#, QxCAS#, and QxWE#.

A or B output disable allows the use of the INSSTE32882LV in reduced parts count applications such as DDR3(L) Mini-RDIMMs. When output disable is asserted, all outputs on the corresponding side of the register including the clock drivers remain in Hi-Z at all times.

Control Word Decoding (cont'd.)

Table 22 – RC1: Clock Driver Enable Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
X	X	X	0	Disable Y0/Y0# clock	Y0/Y0# clock enabled
X	X	X	1		Y0/Y0# clock disabled
X	X	0	X	Disable Y1/Y1# clock	Y1/Y1# clock enabled
X	X	1	X		Y1/Y1# clock disabled
X	0	X	X	Disable Y2/Y2# clock	Y2/Y2# clock enabled
X	1	X	X		Y2/Y2# clock disabled
0	X	X	X	Disable Y3/Y3# clock	Y3/Y3# clock enabled
1	X	X	X		Y3/Y3# clock disabled

Output clocks may be individually turned on or off to conserve power. The system must read the modules' SPD to determine which clock outputs are used by the module. The PLL remains locked on CK/CK# unless the system stops the clock inputs to the INSSTE32882LV to enter the lowest power mode.

Table 23 – RC2: Timing Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
X	X	X	0	Address and command-nets pre-launch (Control Signals QxCKE, QxCS, QxODT do not apply)	Standard (1/2 Clock)
X	X	X	1		Address and command nets pre-launch (3/4 Clock)
X	X	0	X	1T/3T Output Timing	1T Timing
X	X	1	X		3T Timing[1]
X	0	X	X	Input Bus Termination[2]	100 Ω
X	1	X	X		150 Ω
0	X	X	X	Frequency Band Select	Operation (Frequency Band 1)
1	X	X	X		Test Mode (Frequency Band 2)

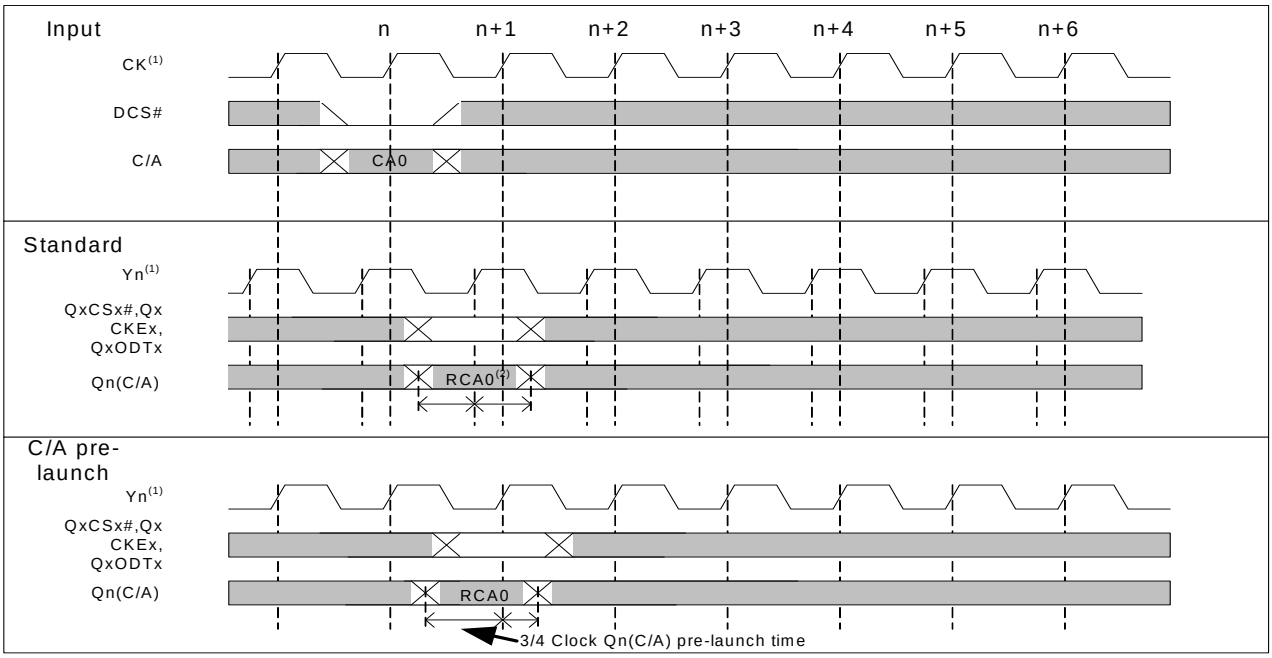
Notes:
1. There is no floating once 3T timing is activated.
2. If MIRROR is 'HIGH' then Input Bus Termination (IBT) is turned off on all inputs, except the DCSn and DODTn inputs.

The Input Bus Termination (IBT) is also located in the RC2 control word with two options of 100 Ω or 150 Ω that can be selected to adapt to different system scenarios. At power-up, the INSSTE32882LV IBT defaults to 100 Ω. The system controller can reprogram the termination resistance to 150 Ω by setting this bit. Only the DAn, DBAn, DRAS#, DCAS#, DWE#, DCSn#, DODT, DCKEn and PAR_IN inputs have the IBT. The CK, CK#, FBIN, FBIN#, RESET#, QCSEN#, and MIRROR inputs do not have IBT. If MIRROR is 'HIGH' then it is assumed the register is located on the backside of a 4 rank module where two registers are tied together on the input side. In this case, for the register on the backside, IBT is controlled by RC8 (refer to table 27).

Control Word Decoding (cont'd.)

The following diagram illustrates the pre-launch feature whereby double loaded nets in a 2-rank configuration can be driven with an earlier signal compared to output clock and control in order to compensate for the slower signal travel speed. This timing applies at all supported frequencies.

Figure 19. Standard versus Address and Command-Nets pre-launch Timing



(1) CK# and Yn# left out for better visibility
(2) RCA0 is re-driven command address signal based on input CA0

Control Word Decoding (cont'd.)

Output driver characteristics are separately controlled for outputs that are often loaded with twice as many DRAMs as other outputs. Outputs are grouped as follows:

- Command/Address (C/A) Signals =QxA0-QxAn, QxBA0-QxBAn, QxRAS#, QxCAS#, QxWE#
- Control Signals = QxCSn#, QxCKEn, QxODTn
- Clock = Y[3:0] / Y[3:0]#

Table 24 – RC3: CA Signals Driver Characteristics Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
X	X	0	0	Command/Address Driver-A Outputs	Light Drive (4 or 5 DRAM Loads)
X	X	0	1		Moderate Drive (8 or 10 DRAM Loads)
X	X	1	0		Strong Drive (16 or 20 DRAM Loads)
X	X	1	1		Reserved
0	0	X	X	Command/Address Driver-B Outputs	Light Drive (4 or 5 DRAM Loads)
0	1	X	X		Moderate Drive (8 or 10 DRAM Loads)
1	0	X	X		Strong Drive (16 or 20 DRAM Loads)
1	1	X	X		Reserved

Table 25 – RC4: Control Signal Driver Characteristics Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
X	X	0	0	Control Driver-A Outputs	Light Drive (4 or 5 DRAM Loads)
X	X	0	1		Moderate Drive (8 or 10 DRAM Loads)
X	X	1	0		Reserved
X	X	1	1		Reserved
0	0	X	X	Control Driver-B Outputs	Light Drive (4 or 5 DRAM Loads)
0	1	X	X		Moderate Drive (8 or 10 DRAM Loads)
1	0	X	X		Reserved
1	1	X	X		Reserved

Control Word Decoding (cont'd.)

Table 26 – RC5: CK Driver Characteristics Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
X	X	0	0	Clock Y1, Y1#, Y3, and Y3# Output Drivers	Light Drive (4 or 5 DRAM Loads)
X	X	0	1		Moderate Drive (8 or 10 DRAM Loads)
X	X	1	0		Strong Drive (16 or 20 DRAM Loads)
X	X	1	1		Reserved
0	0	X	X	Clock Y0, Y0#, Y2, and Y2# Output Drivers	Light Drive (4 or 5 DRAM Loads)
0	1	X	X		Moderate Drive (8 or 10 DRAM Loads)
1	0	X	X		Strong Drive (16 or 20 DRAM Loads)
1	1	X	X		Reserved

Table 27 – RC8: Additional IBT Settings Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
X	0	0	0	IBT Compatibility Settings	IBT as defined in RC2
0	X	X	X	Mirror Mode	IBT Off when MIRROR is 'HIGH'[1]
1	X	X	X		IBT On when MIRROR is 'HIGH'[2]
X	0	0	1	Input Bus Termination[1]	Reserved
X	0	1	0		200 Ω
X	0	1	1		Reserved
X	1	0	0		300 Ω
X	1	0	1		Reserved
X	1	1	0		Reserved
X	1	1	1		Off[3]

Notes:
1. If MIRROR is 'HIGH' then Input Bus Termination (IBT) is turned off on all inputs, except DCSn# and DODTn inputs
2. When DBA0 = 1, DA4 = 1, DA3 = 1, IBT on all inputs is turned off irrespective of DBA1 setting.
3. With this setting, irrespective of the logic level of the MIRROR input pin, IBT on all inputs (including DCSn# and DODTn) is turned off.

Control Word Decoding (cont'd.)

The INSSTE32882LV provides additional IBT settings for a register that is located on the backside of a 4-rank module where two registers are tied together on the input side (DCSn# and DODTn are not shared). In this case, for the register on the backside (MIRROR is HIGH), IBT is turned off on all inputs, except for DCSn# and DODTn inputs by default. However, setting RC8[DBA1] = 1 will turn on IBT for the register on the backside, allowing the use of the 200 Ω or 300 Ω settings (RC8[DBA0, DA4, DA3]) to provide a combined input termination of 100 Ω or 150 Ω respectively with the register on the frontside.

Table 28 – RC9: Weak Drive mode and Power Saving Settings Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
X	X	X	0	Weak Drive Mode[1] (when DCSn# = HIGH, DA3=1, and RC0 [DA4]=1)	"Floating Outputs" as defined in RC0 [DA4]
X	X	X	1		Weak Drive enabled (Drive Strength: 70Ω min, 100Ω nom, 120Ω max)
X	X	0	X	Reserved	Reserved
X	X	1	X		Reserved
1	0	X	X	CKE Power Down Mode	CKE power down with IBT ON, QxODT is a function of DODT
1	1	X	X		CKE power down with IBT off, QxODT held LOW
0	X	X	X	CKE Power Down Mode Enable	Disabled
1	X	X	X		Enabled

Notes:
1 When all DCS# pins are HIGH (i.e. SDRAM is in deselected state), there is no memory access to the DRAM, and the Register output can either be in a Normal Drive Mode, floated, or driven under Weak Drive Mode. A Weak Drive Mode is a mode in which CA signal output drivers (QxA0-QxAn, QxBA0-QxBAn, QxRAS#, QxCAS#, QxWE#) will be driven 2.5 to 3 times weaker than the Light Drive as specified in RC3, and the SDRAM VIL/VIH DC limit will be maintained. The Weak Drive Mode entry and exit timing is bounded by tDIS and tEN respectively.

The INSSTE32882LV features a weak drive mode, which is a variant of the floating mode set in RC0. If bit DA4 of RC0 is set to '1' then bit DA3 of RC9 selects between floating mode and weak drive mode. The weak drive strength is nominally 100 Ω.

The INSSTE32882LV register supports different power down modes. By default, the Power Down feature is disabled (RC9[DBA1]=0). The register ignores CKE Power Down mode setting when this function is disabled. If the CKE Power Down mode is enabled (RC9[DBA1]=1), then power down is invoked once both DCKE0 and DCKE1 are LOW. Bit DBA0 selects how IBT and ODT will behave.

Control Word Decoding (cont'd.)

Table 29 – RC10: Encoding for RDIMM Operating Speed

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
X	0	0	0	f ≤ 800 MTS	DDR3(L)-800 (default)
X	0	0	1	800 MTS < f ≤ 1066 MTS	DDR3(L)-1066
X	0	1	0	1066 MTS < f ≤ 1333 MTS	DDR3(L)-1333
X	0	1	1	1333 MTS < f ≤ 1600 MTS	DDR3(L)-1600
X	1	0	0	1600 MTS < f ≤ 1866 MTS	DDR3(L)-1866
X	1	0	1	Reserved	Reserved
X	1	1	0	Reserved	Reserved
X	1	1	1	Reserved	Reserved

Note:
The encoding value is used to inform the register the operating speed that it is being run at in a system. It is not an indicator of how fast or slow a register can run.

RC11 is used to inform INSSTE32882LV under what operating voltage VDD will be used. Register can use the information to optimize their functionality and performance at low voltage condition.

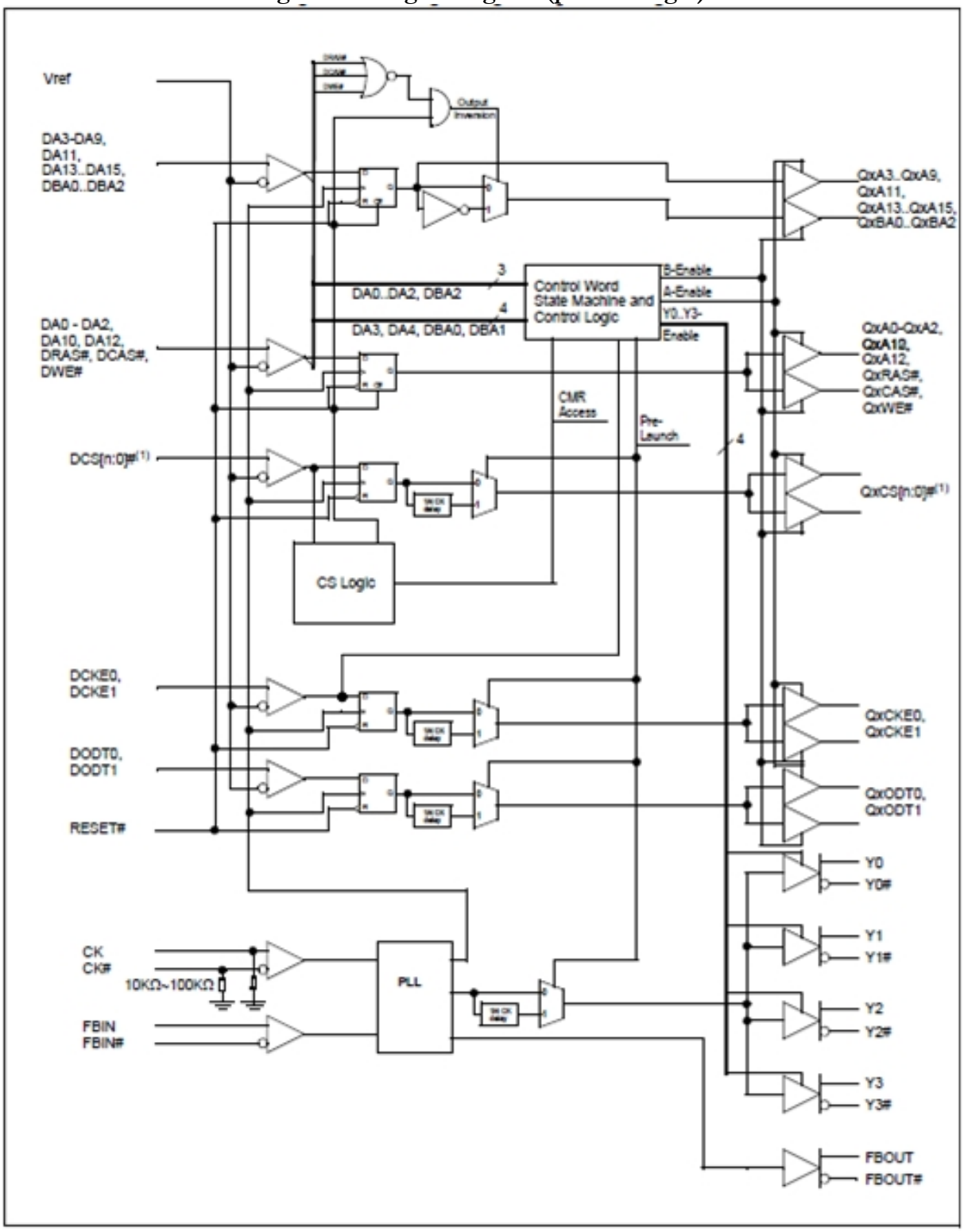
Table 30 – RC11: Operating Voltage VDD Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
X	X	0	0	Register V_{DD} Operating Voltage	DDR3 1.5V mode
X	X	0	1		DDR3L 1.35 V mode[1]
X	X	1	0		Reserved
X	X	1	1		Reserved
0	0	X	X	Reserved	Reserved
0	1	X	X		Reserved
1	0	X	X		Reserved
1	1	X	X		Reserved

Note:
1. DDR3L 1.35 V register is backward compatible and operable to DDR3 1.5 V specification. To guarantee all timings and specifications for DDR3 1.5 V specification, the register must be configured with RC11[DA4:DA3]=00b.

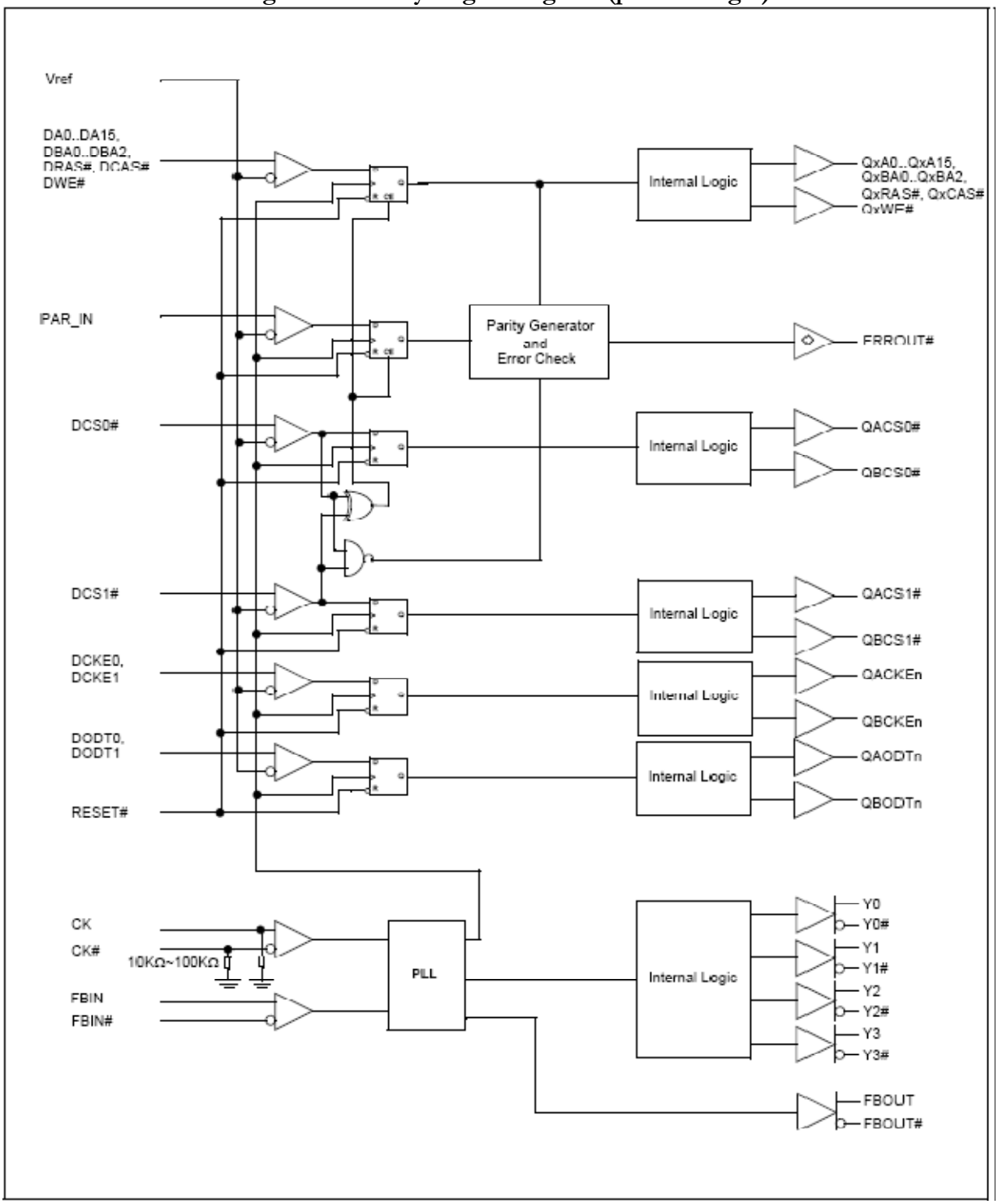
Logic Diagram

Figure 20. Logic Diagram (positive logic)



Logic Diagram (cont'd.)

Figure 21. Parity Logic Diagram (positive logic)



Absolute Maximum Ratings

Table 31

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Power Supply Voltage		-0.4	---	+1.975	V
V_I	Input Voltage Range[2, 3]	See Note 2 and 3	-0.4	---	V_{DD} +0.5	V
V_{REF}	Reference Voltage Range		-0.4	---	V_{DD} +0.5	V
V_O	Output Voltage Range[2, 3]	See Note 2 and 3	-0.4	---	V_{DD} +0.5	V
I_{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{DD}$	---	---	±50	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{DD}$	---	---	±50	mA
I_O	Continuous output current	$0 < V_O < V_{DD}$	---	---	±50	mA
I_{CCC}	Continuous current through each V_{DD} or GND pin		---	---	±100	mA
T_{STORE}	Shipping/Storage Temperature		-65	---	+150	°C

Notes:

1. Stress values beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. This value is limited to 1.975 V maximum.

DC and AC Specifications

The INSSTE32882LV parametric values are specified for the device default control word settings, unless stated otherwise. Note that the RC10 setting does not affect any parametric values.

Operating Conditions

Table 32

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	1.5V Supply voltage		1.425	1.5	1.575	V
V_{DD}	1.35 V Supply voltage		1.282	1.35	1.451	V
V_{REF}	Reference voltage		0.49 * V_{DD}	0.5 * V_{DD}	0.51 * V_{DD}	V
V_{TT}	Termination voltage		V_{REF} – 40	V_{REF}	V_{REF} + 40	mV
V_I	Input voltage		0	---	V_{DD}	V
$V_{IH\ (AC)}$	AC HIGH-level input voltage (1.5 V Operation, DDR3-800/1066/1333)	Data inputs[1]	V_{REF} + 175	---	V_{DD} + 400	mV
	AC HIGH-level input voltage (1.5 V Operation, DDR3-1600)	Data inputs[1]	V_{REF} + 150	---	V_{DD} + 400	
	AC HIGH-level input voltage (1.35 V Operation, DDR3L-800/1066/1333)	Data inputs[1]	V_{REF} + 150	---	V_{DD} + 200	
	AC HIGH-level input voltage (1.35 V Operation, DDR3L-1600)	Data inputs[1]	V_{REF} + 135	---	V_{DD} + 200	
$V_{IL\ (AC)}$	AC HIGH-level input voltage (1.5 V Operation, DDR3-800/1066/1333)	Data inputs[1]	–400	---	V_{REF} – 175	mV
	AC HIGH-level input voltage (1.5 V Operation, DDR3-1600)	Data inputs[1]	–400	---	V_{REF} – 150	
	AC HIGH-level input voltage (1.35 V Operation, DDR3L-800/1066/1333)	Data inputs[1]	–200	---	V_{REF} – 150	
	AC HIGH-level input voltage (1.35 V Operation, DDR3L-1600)	Data inputs[1]	–200	---	V_{REF} – 135	
$V_{IH\ (DC)}$	DC HIGH-level input voltage (1.5 V Operation)	Data inputs[1]	V_{REF} + 100	---	V_{DD} + 400	mV
	DC HIGH-level input voltage (1.35 V Operation)	Data inputs[1]	V_{REF} + 90	---	V_{DD} + 200	
$V_{IL\ (DC)}$	DC LOW-level input voltage (1.5 V Operation)	Data inputs[1]	–400	---	V_{REF} – 100	mV
	DC HIGH-level input voltage (1.35 V Operation)	Data inputs[1]	–200	---	V_{REF} – 90	
V_{IH}	HIGH-level input voltage	CMOS inputs[2]	0.65 * V_{DD}	---	V_{DD}	V
V_{IL}	LOW-level input voltage	CMOS inputs[2]	0	---	0.35 * V_{DD}	V
$V_{IL(static)}$	Static LOW-level input voltage[3]	CK, CK#	---	---	0.35 * V_{DD}	V
$V_{IX(AC)}$	Input differential pair cross voltage (1.5 V Operation, DDR3-800/1066/1333/1600)	CK, CK#, FBIN, FBIN#	0.5xV_{DD} - 175	0.5xV_{DD}	0.5xV_{DD} + 175	mV
			0.5xV_{DD} – 200[10]	0.5xV_{DD}	0.5xV_{DD} + 200[10]	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Input differential pair cross voltage (1.35 V Operation, DDR3L-800/1066/1333/1600)	CK, CK#, FBIN, FBIN#	$0.5xV_{DD}$ - 150	$0.5xV_{DD}$	$0.5xV_{DD}$ + 150	
			$0.5xV_{DD}$ - 180[11]	$0.5xV_{DD}$	$0.5xV_{DD}$ + 180[11]	
$V_{ID(AC)}$	Differential input range[4] (1.5 V Operation, DDR3-800/1066/1333)	CK, CK#	350	---	V_{DD}	mV
	Differential input range[4] (1.5 V Operation, DDR3-1600)	CK, CK#	300	---	V_{DD}	
	Differential input range[4] (1.35 V Operation, DDR3L-800/1066/1333)	CK, CK#	300	---	V_{DD}	
	Differential input range[4] (1.35 V Operation, DDR3L-1600)	CK, CK#	270	---	V_{DD}	
I_{OH}	HIGH-level output current[5]	All outputs except ERROUT#	---	---	-11	mA
I_{OL}	LOW-level output current[5]	All outputs except ERROUT#	11	---	---	mA
	LOW-level output current	ERROUT#	25	---	---	mA
V_{OD}	Output differential voltage[6] (1.5 V Operation)	Yn, Yn#	500	---	V_{DD}	mV
	Output differential voltage[6] (1.35 V Operation)	Yn, Yn#	450	---	V_{DD}	
V_{OX}	Output differential cross-point voltage (1.5 V Operation)	Yn, Yn#	$0.5xV_{DD}$ - 100	---	$0.5xV_{DD}$ + 100	mV
	Output differential cross-point voltage (1.35 V Operation)	Yn, Yn#	$0.5xV_{DD}$ - 90	---	$0.5xV_{DD}$ + 90	
Tj	Junction Temperature		---	---	125	°C
		DDR3(L)-800	DDR3(L)-1066	DDR3(L)-1333	DDR3(L)-1600	
$T_{CASE\ (max)}$	Case Temperature[7]	109[8,9]	108[8,9]	106[8,9]	103[8,9]	°C

Notes:

1. DCKE0/1, DODT0/1, DA0..DA15, DBA0..DBA2, DRAS#, DCAS#, DWE#, PAR_IN, DCS[1:0]# when QCSEN# = HIGH, DCS[3:0]# when QCSEN# = LOW.
2. RESET#, MIRROR, QCSEN#
3. This spec applies only when both CK and CK# are actively driven LOW. It does not apply when CK/CK# are floating.
4. VID is the magnitude of the difference between the input level on CK and the input level on CK# See Diagram (Figure 29, "Voltage waveforms; input clock")
5. Default settings
6. VOD is the magnitude of the difference between the output level on Yn and the output level on Yn# See Diagram (Figure 32, "Voltage waveforms; Address Floating")
7. Measurement procedure JESD51-2
8. This spec is meant to guarantee a Tj of 125C by the INSST32882LV device. Since Tj cannot be measured or observed by users, Tcase is specified instead. Under all thermal conditions, the Tj of INSSTE32882LV device shall not be higher than 125 °C.
9. ThetaJC=17.40 C/W, and ThetaJA=50 C/W (with zero airflow rate) for 8.00mm x 13.50 mm package. ThetaJC=17.30 C/W, and ThetaJA=47 C/W (with zero airflow rate) for 6.00mm x 15.00 mm package.
10. Extended range for VIX is only allowed for clock (CK and CK#) and if single-ended clock input signals CK and CK# are monotonic with a single-ended swing VSEL/VSEH of at least VDD/2 +/-275 mV, and when the differential slew rate of CK - CK# is larger than 4 V/ns
11. Extended range for VIX is only allowed for clock (CK and CK#) and if single-ended clock input signals CK and CK# are monotonic with a single-ended swing VSEL/VSEH of at least VDD/2 +/-243 mV, and when the differential slew rate of CK - CK# is larger than 3.6 V/ns.

DC Specifications

Table 33

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} = –11 mA	V_{DD}-0.4	---	---	V
V_{OL}	LOW-level output voltage	I_{OL} = 11 mA	---	---	0.4	V
V_{ERROL}	LOW-level output voltage (ERROUT#)	I_{ERROL} = 25 mA	---	---	0.4	V
I_I	Input current	RESET#, MIRROR, V_I = V_{DD} or GND	---	---	±5	µA
I_I	Input current	QCSEN#, V_I = V_{DD} or GND	–150	---	5	µA
I_{ID}	Input current	Data inputs[1], V_I = V_{DD} or GND	---	---	±5	µA
I_{ID}	Input current	CK, CK#[2], V_I = V_{DD} or GND	–5	---	150	µA
I_{DD}	Static standby current	RESET# = GND and CK, CK# = V_{IL}	---	---	5	mA
	Static operating current	RESET# = V_{DD}, MIRROR = V_{DD}, RC8=x111 (IBT Off), CK/CK#=Vil(static), and V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$	---	---	15	mA
I_{DDD}	Dynamic supply current, input clock only (1.5 V Operation)	RESET# = V_{DD}, MIRROR = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CK and CK# switching 50% duty cycle, I_O = 0, V_{DD} = V_{DD}(max)	---	0.150	---	mA/MHz
	Dynamic supply current, input clock only (1.35 V Operation)		---	0.135	---	
	Dynamic supply current, per each data input (1.5 V Operation)	RESET# = V_{DD}, MIRROR = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CK and CK# switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle, I_O = 0, V_{DD} = V_{DD}(max)	---	0.003	---	mA/MHz
	Dynamic supply current, per each data input (1.35 V Operation)		---	0.003	---	

Notes:
1. DCKE0/1, DODT0/1, DA0..DA15, DBA0...DBA2, DRAS#, DCAS#, DWE#, PAR_IN, DCS[1:0]# when QCSEN# = HIGH, DCS[3:0]# when QCSEN# = LOW are measured while RESET# pulled LOW.
2. The CK and CK# inputs have pull-down resistors in the range of 10 KΩ to 100 KΩ.

DC Specifications (cont'd.)

Table 34

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_I	Input capacitance, data inputs	see notes 1, 2	1.5	---	2.5	pF
	Input capacitance, CK, CK#, FBIN, FBIN#	see note 1	1.5	---	2.5	pF
$C_{I\Delta}$	Delta capacitance over all inputs		---	---	0.5	pF
C_{IR}	Input capacitance, RESET#, MIRROR, QCSEN#	$V_I = V_{DD}$ or GND; V_{DD} = 1.5V	---	---	3	pF

Notes:

1. This parameter is not subject to production test. It is verified by design and characterization. Input capacitance is measured according to JEP147 ("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER (VNA)") with VDD, VSS, AVDD, AVSS, PVDD, PVSS, VREF applied and all other pins (except the pin under test) floating. Input capacitance are measured with the device default settings when MIRROR = LOW.
2. Data inputs are DCKE0/1, DODT0/1, DA0..DA15, DBA0...DBA2, DRAS#, DCAS#, DWE#, PAR_IN DCS[1:0]# when QCSEN# = HIGH, DCS[3:0]# when QCSEN# = LOW

Timing Requirements

Table 35

Symbol	Parameter	Conditions	DDR3(L)-800/1066/1333		DDR3(L)-1600		Unit
			Min	Max	Min	Max	
f_{CLOCK}	Input clock frequency	Application frequency[1]	300	670	300	810	MHz
f_{TEST}	Input clock frequency	Test frequency[2]	70	300	70	300	MHz
t_{CH}/t_{CL}	Pulse duration	CK, CK# HIGH or LOW	0.4	---	0.4	---	t_{CK}[3]
t_{ACT}	Input active time[4] before RESET# is taken HIGH	DCKE0/1 = LOW and DCS0/1# = HIGH	8	---	8	---	t_{CK}[3]
t_{MRD}	Command word to command word programming delay	Number of clock cycles between two command programming accesses	8	---	8	---	t_{CK}[3]
t_{InDIS}	Input buffers (except for CK/CK#, DCKEn, DODTn, RESET#) disable time after DCKE[1:0] is LOW	DCKE[1:0] = LOW; RESET# = HIGH; CK/CK# = Toggling; RC9[DBA1]=1 and RC9[DBA0]= 0 or 1	1	4	1	4	t_{CK}[3]
t_{QDIS}[5]	Output buffers (except for Yn/Yn#, QxODTn, QxCKEn, FBOUT/FBOUT#) Hi-Z after QxCKEn is driven LOW	DCKE[1:0] = LOW; RESET# = HIGH; CK/CK# = toggling; RC9[DBA1]=1 and RC9[DBA0]=0 or 1	1.5	1.5	1.5	1.5	t_{CK}[3]
t_{CKoff}	Number of tCK required for both DCKE0 and DCKE1 to remain LOW before both CK/CK# are driven LOW	DCKE[1:0] = LOW; RESET# = HIGH; CK/CK# = Toggling	5	---	5	---	t_{CK}[3]
t_{CKEV}	Input buffers (DCKE0 and DCKE1) disable time after CK/CK# = LOW	DCKE[1:0] = LOW; RESET# = HIGH; CK/CK# = LOW	2	---	2	---	t_{CK}[3]
$t_{Fixedoutput}$	Static register output after DCKE0 or DCKE1 is HIGH at the input (exit from Power saving state)	RC9[DBA1]=1 and RC9[DBA0]=0 or 1	1	3	1	4	t_{CK}[3]
t_{su}	Setup time[6]	Input valid before CK/CK#	**50**	---	**30**	---	ps
t_H	Hold time[7]	Input to remain valid after CK/CK#	**0**	---	**0**	---	ps

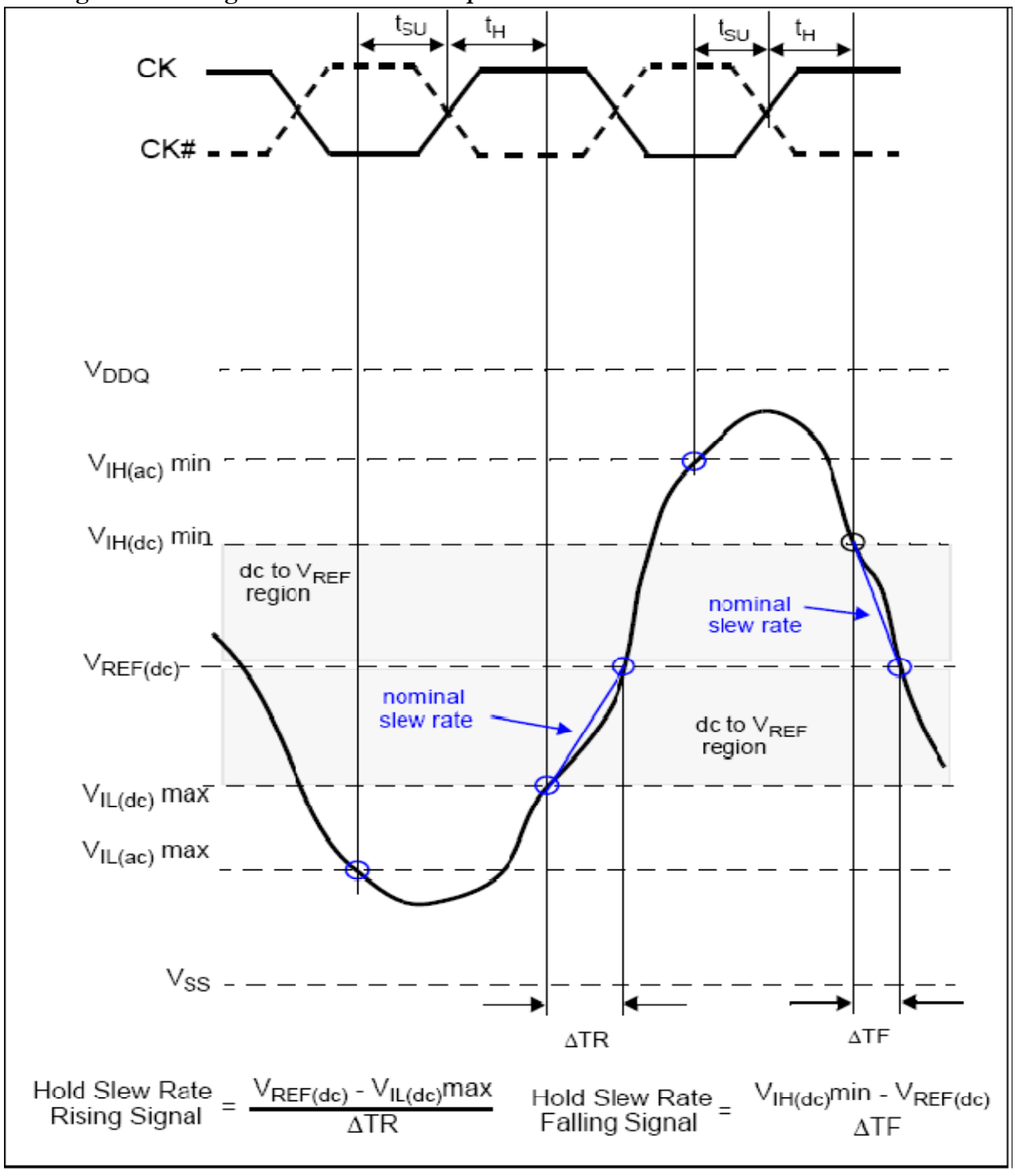
Timing Requirements (cont'd.)

Notes:

1. All specified timing parameters apply.
2. Timing parameters specified for frequency band 2 apply.
3. Clock cycle time;
4. This parameter is not necessarily production tested, see Figures 22 and 23, "Voltage Waveforms for Setup and Hold Times."
5. Currently under discussion in JEDEC.
6. Setup (tSU) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and first crossing of VIH(ac) min. Setup (tSU) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIL(ac)max, see Figure 23, "Voltage Waveforms for Setup and Hold Times – Setup Time Calculation." If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(dc) to AC region', use nominal slew rate for de-rating value. If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(dc) to AC region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for de-rating value, see Figure 23, "Voltage Waveforms for Setup and Hold Time – Setup Time Calculations."
7. Hold (tH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of VREF(dc). Hold (tH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of VREF(dc), see Figure 22, "Voltage Waveforms for Setup and Hold Times – Hold Time Calculation." If the actual signal is always later than the nominal slew rate line between shaded 'dc level to VREF(dc) region' use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to VREF(dc) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(dc) level is used for derating value, see Figure 22, "Voltage Waveforms for Setup and Hold Time – Hold Time Calculation."

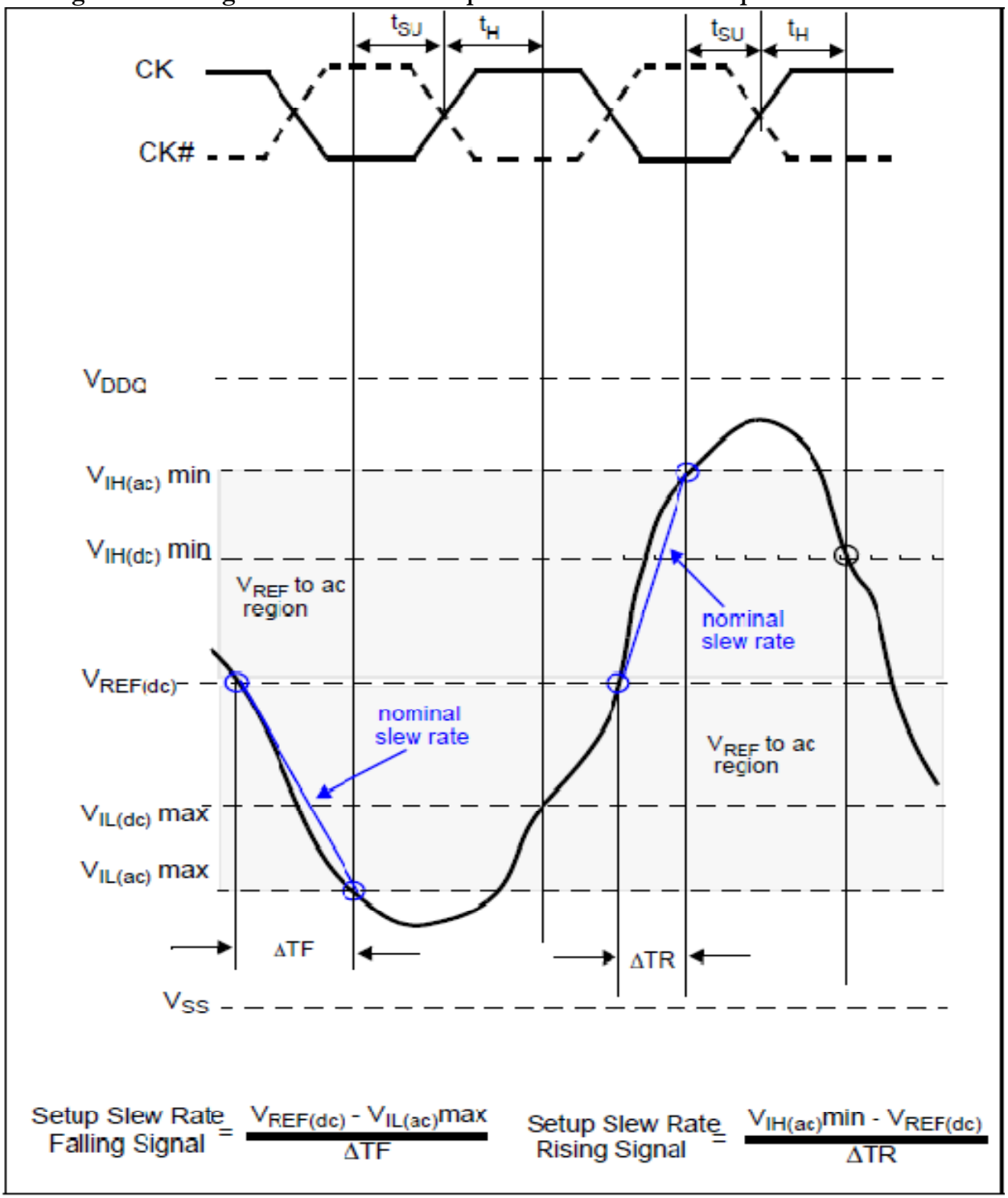
Timing Requirements (cont'd.)

Figure 22. Voltage Waveforms for Setup and Hold Times – Hold Time Calculation



Timing Requirements (cont'd.)

Figure 23. Voltage Waveforms for Setup and Hold Times – Setup Time Calculation



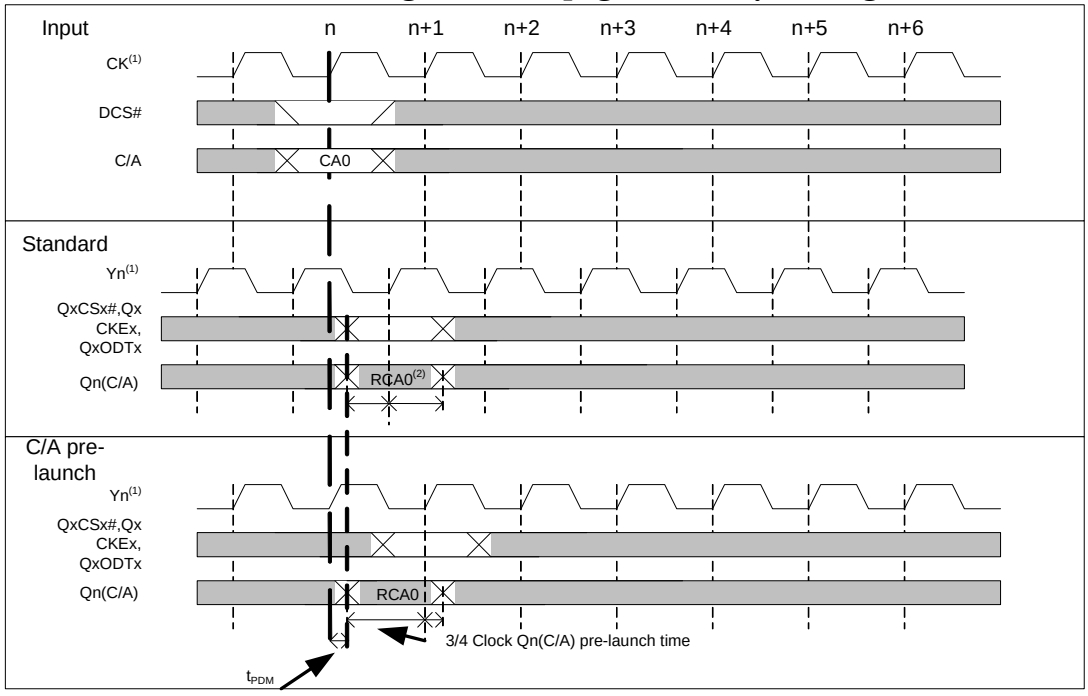
AC Specifications

Table 36 – Output timing requirements[1]

Symbol	Parameter	Conditions	DDR3(L)-800/1066/1333		DDR3(L)-1600		Unit
			Min	Max	Min	Max	
t_{PDM}	Propagation delay, single-bit switching (1.5 V Operation)	CK/CK# to output[2]	**0.75**	1.0	**0.75**	1.0	ns
	Propagation delay, single-bit switching (1.35 V Operation)		**0.85**	1.2	**0.85**	1.2	
t_{DIS}	Output disable time (1/2-Clock pre-launch)	Yn/Yn# to output float[3]	0.5 tCK + t_{Qsk1}(min)	---	0.5 tCK + t_{Qsk1}(min)	---	ps
	Output disable time (3/4 –Clock pre-launch)		0.25 tCK + t_{Qsk2}(min)	---	0.25 tCK+ t_{Qsk2}(min)	---	ps
t_{EN}	Output enable time (1/2-Clock pre-launch)	Yn/Yn# to output driving	0.5 tCK - t_{Qsk1}(max)	---	0.5 tCK - t_{Qsk1}(max)	---	ps
	Output enable time (3/4 –Clock pre-launch)		0.75 tCK - t_{Qsk2}(max)	---	0.75 tCK - t_{Qsk2}(max)	---	ps

Notes:
1. See diagram (Figure 30, "Qn and Yn circuit for propagation delay and slew measurement")
2. See diagram (Figure 24, "Propagation Delay Timing")
3. See diagram (Figure 32, "Voltage waveforms; Address Floating")

Figure 24. Propagation Delay Timing



(1) CK# and Yn# left out for better visibility
(2) RCA0 is re-driven command address signal based on input CA0

Output Buffer Characteristics

Table 37 – Output edge rates over specified operating free-air temperature range

Symbol	Parameter	Conditions	DDR3(L)-800/1066/1333		DDR3(L)-1600		Unit
			Min	Max	Min	Max	
dV/dt_r	Rising edge slew rate[1] (1.5 V Operation)	V_{DD} = 1.5 V ± 0.075 V	2	7	2	5.5	V/ns
	Rising edge slew rate[1] (1.35 V Operation)	V_{DD} = 1.35 V - 0.07 V/ + 0.10 V	1.8	5	1.8	5	
dV/dt_f	Falling edge slew rate[1] (1.5 V Operation)	V_{DD} = 1.5 V ± 0.075 V	2	7	2	5.5	V/ns
	Falling edge slew rate[1] (1.35 V Operation)	V_{DD} = 1.35 V - 0.07 V/ + 0.10 V	1.8	5	1.8	5	
dV/dt_Δ[2]	Absolute rising-falling edge slew rate difference		---	1	---	1	V/ns

Notes:
1. Measured into test load at default register setting except for RC3, RC4, and RC5 which are set according to the drive strength to be measured.
2. Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate)

Register R-on Targets for each drive strength up to DDR3(L)-1600.

Table 38 –R-on Targets

Drive Settings	Output Driver R-on Targets (Ω)		
	Min	Nom	Max
Light	22	26	30
Moderate	16	19	22
Strong	12	14	16

Input Buffer Characteristics

Table 39 – Input IBT Characteristics over specified operating free-air temperature range

Symbol	Parameter	Conditions	DDR3(L)-800/1066/1333/1600		Unit
			Min	Max	
$R_{IBT(tol)}$	Total Effective IBT Value Tolerance[1]		-10	10	%
$R_{IBT\Delta}$	Mismatch Tolerance between R_{IBT-UP} and $R_{IBT-DOWN}$[2]		---	5	%

Notes:
1. Example for 100 Ω, Min=90 Ω, Max=110 Ω
2. $|(R_{IBT-UP}/R_{IBT-DOWN} - 1)| * 100\% \leq 5\%$

Clock Driver Characteristics

Table 40 – Clock driver characteristics at application frequency (frequency band 1)

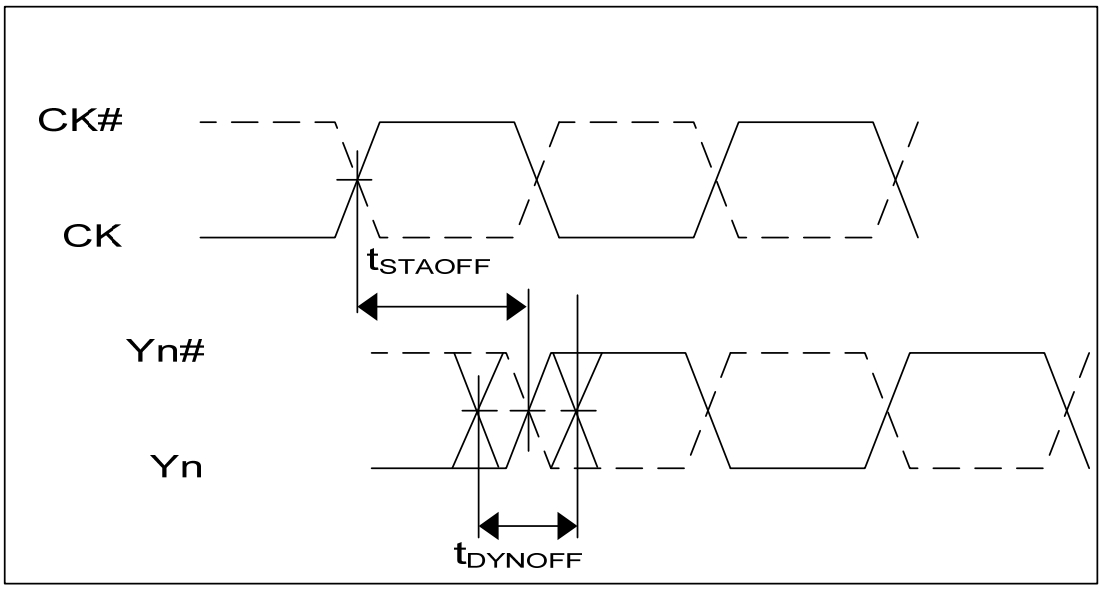
Symbol	Parameter	Conditions	DDR3(L)-800		DDR3(L)-1066		DDR3(L)-1333		DDR3(L)-1600		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{jit}(cc+)$	Cycle-to-cycle period jitter		0	**35**	0	**35**	0	**35**	0	30	ps
$t_{jit}(cc-)$	Cycle-to-cycle period jitter		**-35**	0	**-35**	0	**-35**	0	-30	0	ps
t_{STAB}	Stabilization time		-	**4**	-	**3**	-	**3**	-	**2**	µs
t_{FDYN}	Dynamic phase offset		**–35**	**35**	**–35**	**35**	**–35**	**35**	**-25**	**25**	ps
t_{CKsk}	Fractional clock output skew[1]		-	15	-	15	-	15	-	10	ps
$t_{jit}(per)$	Yn clock period jitter		**–30**	**30**	**–30**	**30**	**–30**	**30**	**-25**	**25**	ps
$t_{jit}(hper)$	Yn clock half-period jitter		**–35**	**35**	**–35**	**35**	**–35**	**35**	**-30**	**30**	ps
$t_{PWH/PWL}$	Yn pulse width HIGH/LOW duration[2]	T_{PW}=1/2 T_{CK}- |T_{JIT}(hper)min| to 1/2 tCK + |T_{JIT}(hper)max|	1.200	1.300	0.888	0.988	0.700	0.800	0.585	0.665	ns
t_{Qsk1}[3]	Qn output to Yn clock tolerance (standard ½ clock pre-launch)	Output inversion enabled	–100	200	–100	200	–100	200	-100	100	ps
		Output inversion disabled	–100	300	–100	300	–100	300	-100	200	ps
t_{Qsk2}[4]	Qn output to Yn clock tolerance (standard ¾ clock pre-launch)	Output inversion enabled	–100	200	–100	200	–100	200	-100	100	ps
		Output inversion disabled	–100	300	–100	300	–100	300	-100	-200	ps
t_{STAOFF}	Average delay through the register between the input clock and output clock[5] (1.5 V Operation)	Standard ½-Clock pre-Launch T_{STAOFF}=T_{PDM} + 1/2 T_{CK}	**2.00**	2.25	**1.69**	1.94	**1.50**	1.75	**1.38**	1.63	ns
		¾ Clock pre-Launch T_{STAOFF}=T_{PDM} + 3/4 T_{CK}	**2.63**	2.88	**2.16**	2.41	**1.87**	2.12	**1.69**	1.94	
	Average delay through the register between the input clock and output clock[5] (1.35 V Operation)	Standard ½-Clock pre-Launch T_{STAOFF}=T_{PDM} + 1/2 T_{CK}	**2.10**	2.45	**1.79**	2.14	**1.60**	1.95	**1.48**	1.83	ns
		¾ Clock pre-Launch T_{STAOFF}=T_{PDM} + 3/4 T_{CK}	**2.73**	3.08	**2.26**	2.61	**1.97**	2.32	**1.79**	2.14	

Symbol	Parameter	Conditions	DDR3(L)-800		DDR3(L)-1066		DDR3(L)-1333		DDR3(L)-1600		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{DYNOFF}[6,7]	Maximum variation in delay between the input & output clock		-	70	-	65	-	60	-	55	ps

Notes:

1. This skew represents the absolute output clock skew and contains the pad skew and package skew (See Figure 26, "Clock Output (Yn) Skew"). This parameter is specified for the clock pairs on each side of the register independently. The skew is applicable to left side clock pairs between Y0/Y0# and Y2/Y2#, as well as right side of the clock pairs between Y1/Y1# and Y3/Y3#. This is not a tested parameter and has to be considered as a design goal only.
2. This parameter is a measure of the output clock pulse width HIGH/LOW. The output clock duty cycle can be calculated based on t_{PW}.
3. This skew represents the absolute Qn skew compared to the output clock,(Yn), and contains the register pad skew, clock skew and package routing skew (See Figure 27, "Qn Output Skew for Standard 1/2-Clock Pre-Launch"). The output clock jitter is not included in this skew. The parameter includes the skew related to simultaneous switching noise (SSO). The Qn output can either be early or late. This parameter applies to each side of the register independently.
4. This skew represents the absolute Qn skew compared to the output clock (Yn), and contains the register pad skew, clock skew and package routing skew (See Figure 28, "Qn Output Skew for 3/4-Clock Pre-Launch"). The output clock jitter is not included in this skew. The parameter includes the skew related to simultaneous switching noise (SSO). The Qn output can either be early or late. This parameter applies to each side of the register independently.
5. This parameter measures the delay from the rising differential input clock which samples incoming C/A to the rising differential output clock that will be used to sample the same C/A data. t_{STAOFF} may vary by the amount of t_{DYNOFF} based on voltage and temperature as well as tracking error and jitter. Including this variation t_{STAOFF} may not exceed the limits set by the $t_{STAOFF(min)}$ and $t_{STAOFF(max)}$.
6. See Figure 25, "Definition for t_{STAOFF} and t_{DYNOFF}".
7. This includes all sources of jitter and drift (e.g. Thermal noise, supply noise, voltage/temperature drift, SSC tracking, SSO, etc) except reference clock noise.

Figure 25. Definition for t_{STAOFF} and t_{DYNOFF}



1. t_{staoff} = propagation delay for clock signal (rising CK input clock edge to rising Yn output clock edge).
2. t_{dynoff} = maximum tstaoff variation over voltage and temperature. This includes all sources of jitter and drift (e.g.Thermal noise, supply noise, voltage/temperature drift, SSC tracking, SSO, etc) except reference clock noise.

Figure 26. Clock Output (Yn) Skew

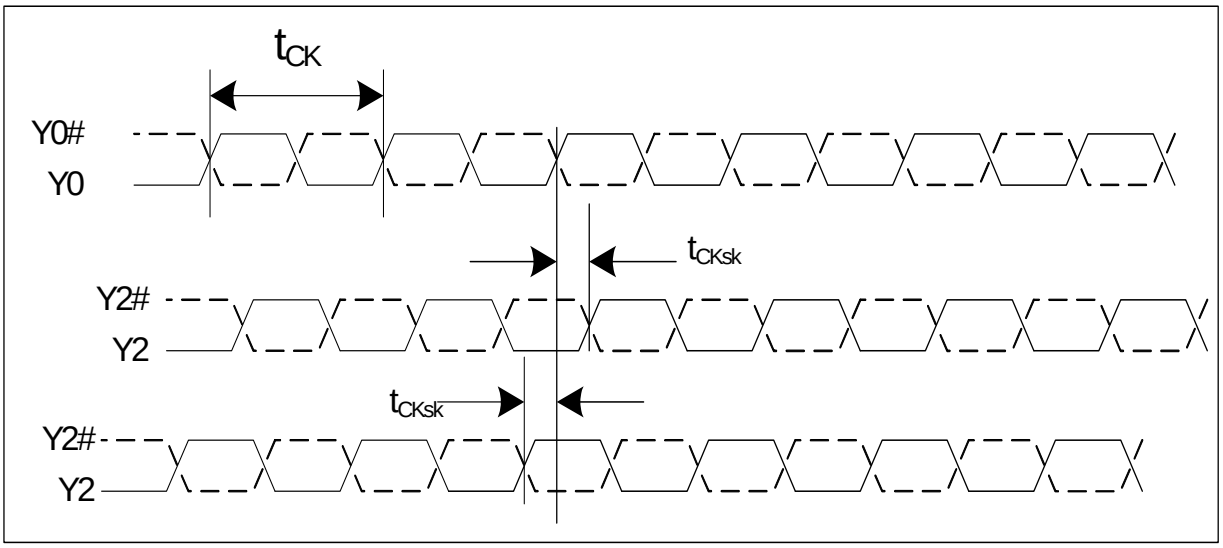


Figure 27. Qn Output Skew for Standard 1/2-Clock Pre-Launch

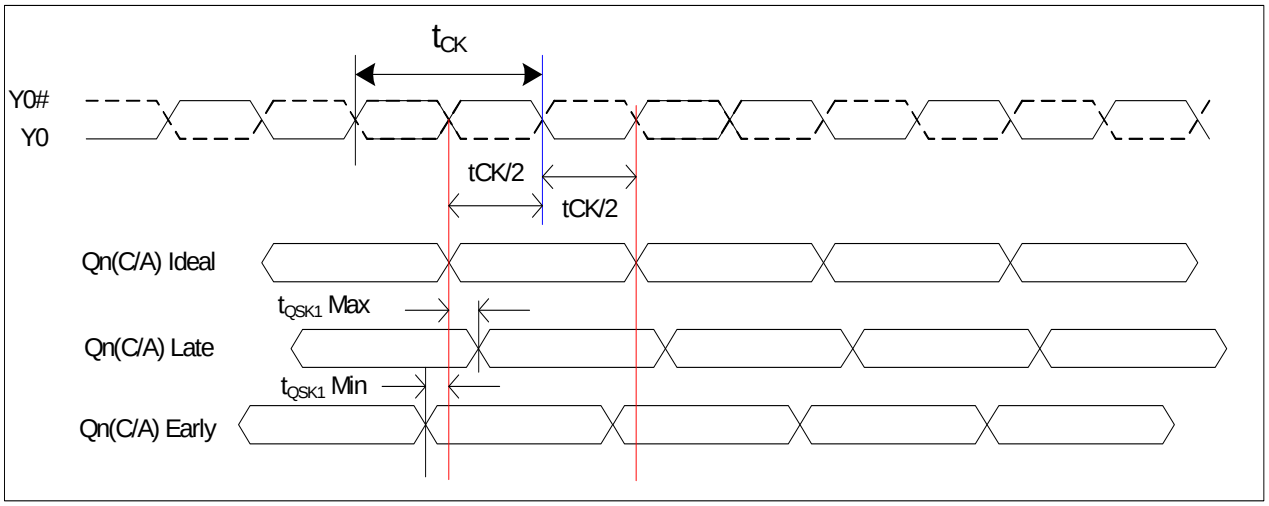
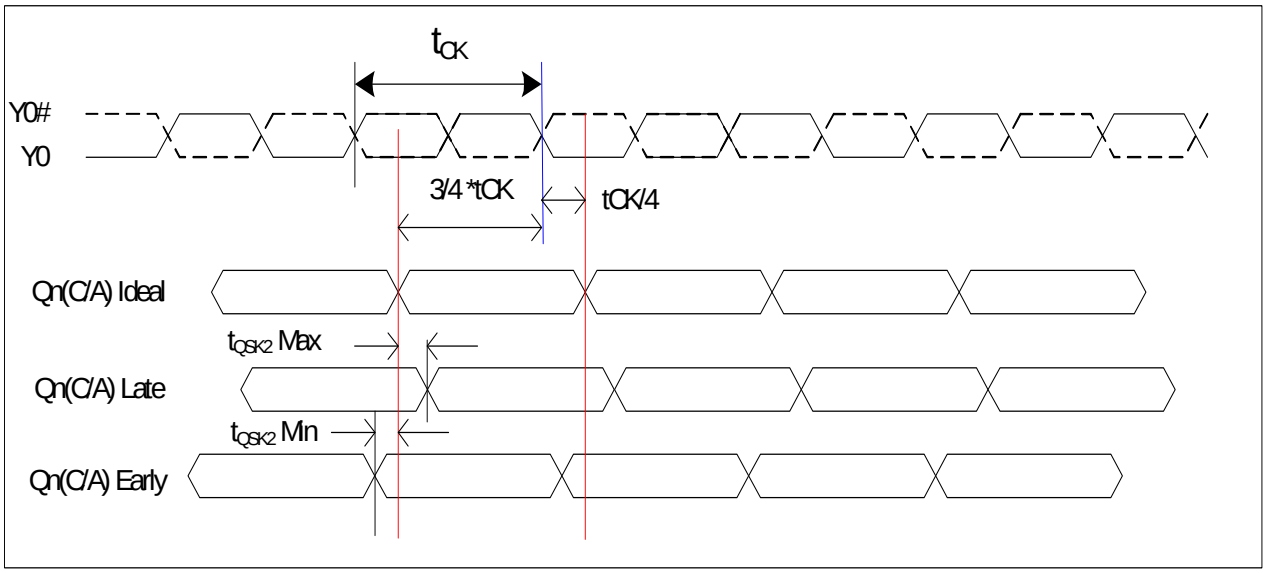


Figure 28. Qn Output Skew for Standard 3/4-Clock Pre-Launch



Clock Driver Characteristics (cont'd.)

Table 41 – Clock driver characteristics at test frequency (frequency band 2)

Symbol	Parameter	Conditions	Band2		Unit
			Min	Max	
$t_{jit}(cc)$	Cycle-to-cycle period jitter		0	120	ps
t_{STAB}	Stabilization time		---	15	us
t_{CKsk}	Fractional clock output skew[1]		---	50	ps
$t_{jit}(per)$	Yn clock period jitter		–75	75	ps
$t_{jit}(hper)$	Yn clock half-period jitter		–75	75	ps
t_{Qsk1}[2]	Qn output to clock tolerance (standard ½ clock pre-launch)	Output inversion enabled	-100	250	ps
		Output inversion disabled	-100	300	ps
t_{Qsk2}[3]	Qn output to clock tolerance (standard ¾ clock pre-launch)	Output inversion enabled	-100	250	ps
		Output inversion disabled	-100	300	ps
t_{DYNOFF}[4,5]	Maximum variation in delay between the input & output clock		---	150	ps

Notes:

1. This skew represents the absolute output clock skew and contains the pad skew and package skew (See Figure 26, "Clock Output (Yn) Skew"). This parameter is specified for the clock pairs on each side of the register independently. The skew is applicable to left side clock pairs between Y0/Y0# and Y2/Y2#, as well as right side of the clock pairs between Y1/Y1# and Y3/Y3#. This is not a tested parameter and has to be considered as a design goal only.
2. This skew represents the absolute Qn skew compared to the output clock,(Yn), and contains the register pad skew, clock skew and package routing skew (See Figure 27, "Qn Output Skew for Standard 1/2-Clock Pre-Launch"). The output clock jitter is not included in this skew. The parameter includes the skew related to simultaneous switching noise (SSO). The Qn output can either be early or late. This parameter applies to each side of the register independently.
3. This skew represents the absolute Qn skew compared to the output clock (Yn), and contains the register pad skew, clock skew and package routing skew (See Figure 28, "Qn Output Skew for 3/4-Clock Pre-Launch"). The output clock jitter is not included in this skew. The parameter includes the skew related to simultaneous switching noise (SSO). The Qn output can either be early or late. This parameter applies to each side of the register independently.
4. See Figure 25, "Definition for t_{STAOFF} and t_{DYNOFF}".
5. This includes all sources of jitter and drift (e.g. Thermal noise, supply noise, voltage/temperature drift, SSC tracking, SSO, etc) except reference clock noise.

Clock Driver Characteristics (cont'd.)

Table 42 – SSC Parameters and PLL Bandwidth

Symbol	Parameter	Conditions	DDR3(L)-800		DDR3(L)-1066		DDR3(L)-1333		DDR3(L)-1600		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
f_{SSCMOD}	SSC modulation frequency		30	33	30	33	30	33	30	33	kHz
f_{SSCDEV}	SSC clock input frequency deviation		0.00	-0.5	0.00	-0.5	0.00	-0.5	0.00	-0.5	%
f_{BW}	PLL Loop bandwidth (-3 dB from unity gain)		25[1]	-	30[1]	-	35[1]	-	40[1]	-	MHz

Note:
1. Implies a –3 dB bandwidth and jitter peaking of 3 dB.

Load Circuit and Voltage Waveforms

General Measurement Notes:

All input pulses are supplied by generators having the following characteristics:
300 ≤ PRR ≤ 810 MHz, Z_O = 50 Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).
The outputs are measured one at a time with one transition per measurement.

Figure 29. Voltage Waveforms; Input Clock

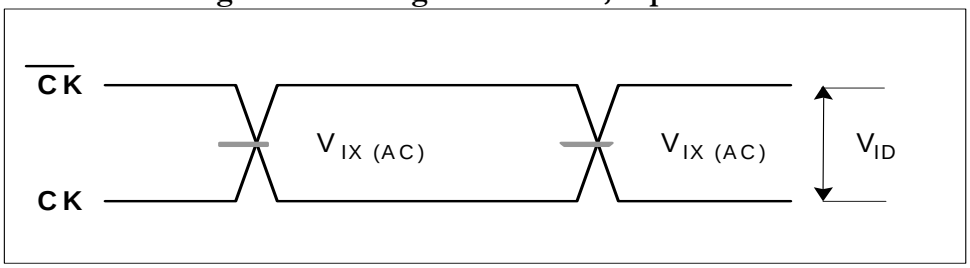
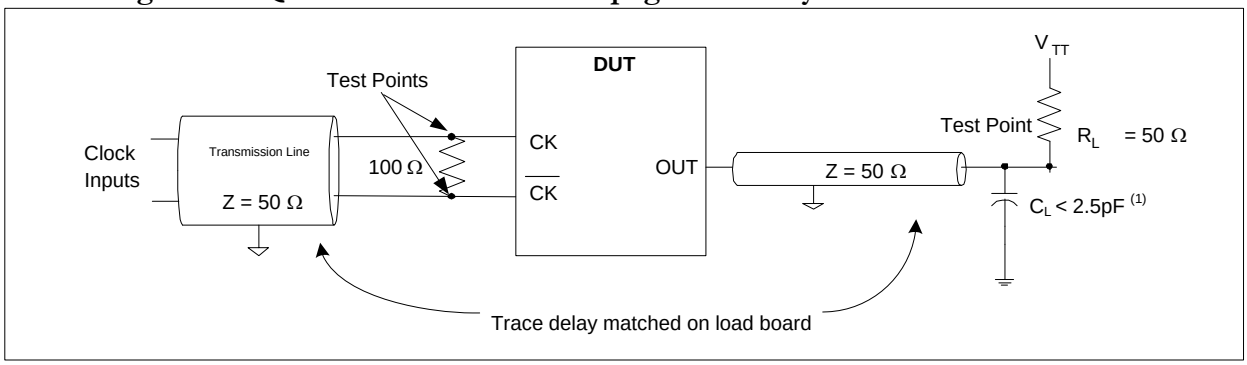
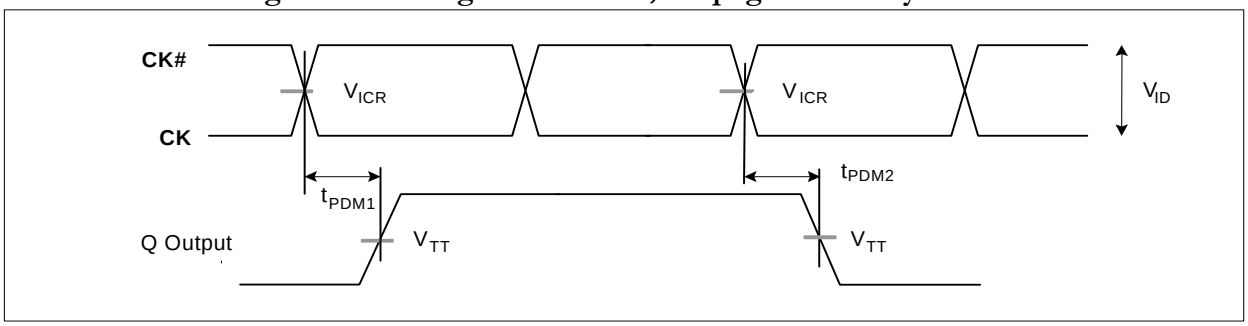


Figure 30. Qn and Yn Circuit for Propagation Delay and Slew Measurement



Notes:
1. C_L is parasitic (probe and jig capacitance)

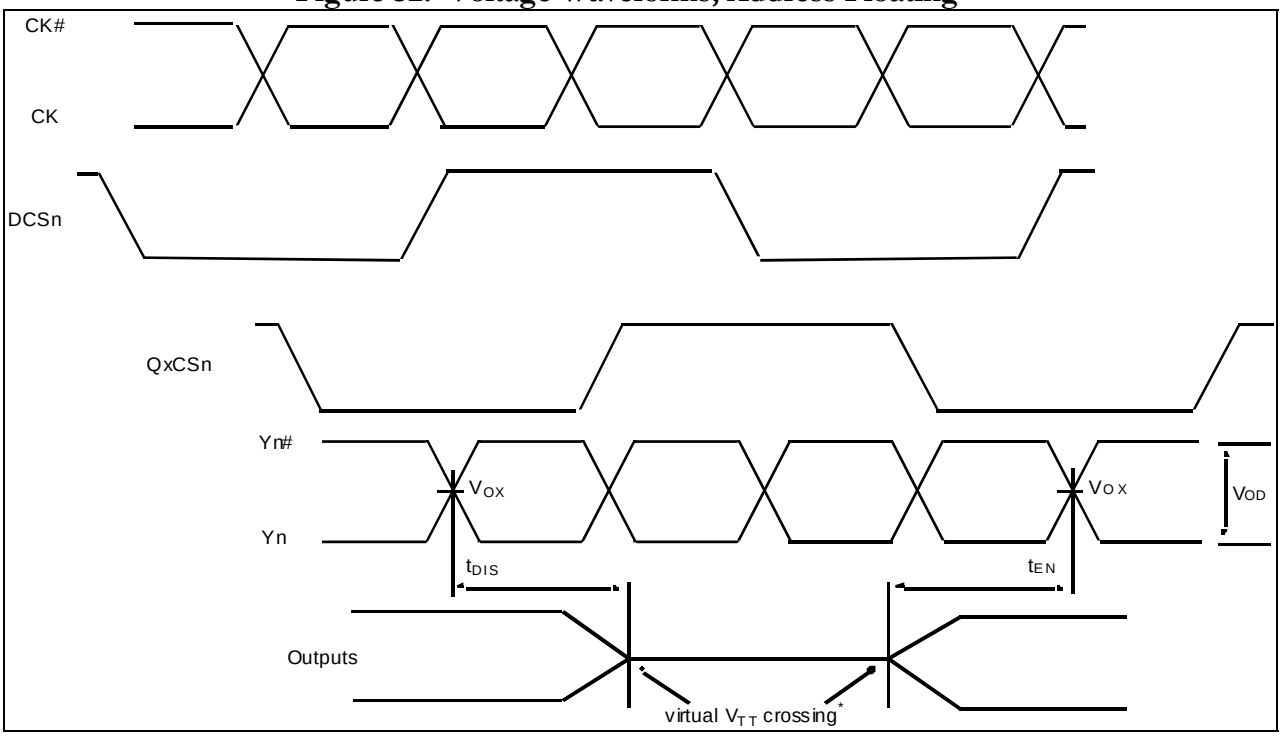
Figure 31. Voltage Waveforms; Propagation Delay Times



$V_{TT} = V_{DD}/2$

Notes:
1. V_{ICR} Cross Point Voltage
2. V_{ID}= 500 mV (1.5 V Operation) or 450 mV (1.35 V Operation)
3. t_{PDM1}, t_{PDM2} the larger number of both has to be taken when performing t_{PDM} max measurement, the smaller number of both has to be taken when performing t_{PDM} min measurement.

Figure 32. Voltage Waveforms; Address Floating

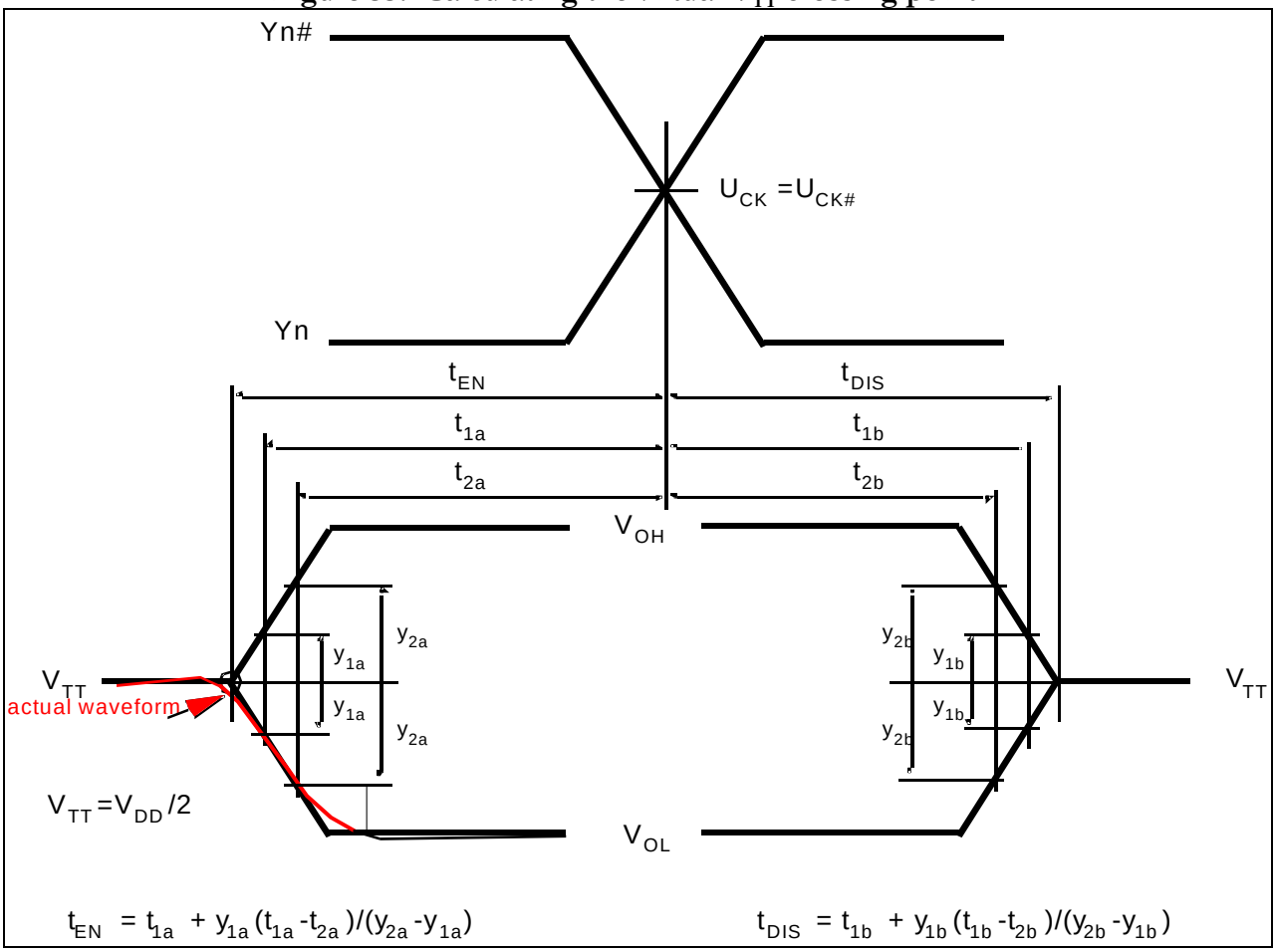


See Figure 33, "Calculating the virtual V_{TT} crossing point"

Enabling and disabling the CA outputs must not violate DRAM setup and hold time requirements. Therefore a t_{DIS} transition may not occur earlier than the earliest (HL/LH) transition and a t_{EN} transition may not occur later than the latest (HL/LH) transition. Regular transitions are measured between CK/CK# and CA/V_{TT} crossings however a V_{TT} crossing is not available in the state where the outputs are Hi-Z. To allow a correct and not overly conservative measurement a virtual V_{TT} crossing point is defined below. The calculation of the virtual V_{TT} crossing point is shown in Figure 33, "Calculating the virtual V_{TT} crossing point. The voltage levels for y_{xa} and y_{xb} are measured from V_{TT} (V_{DD}/2) and should be selected such that the region between t_1 and t_2 covers a linear range and represents a typical slope of the waveform within the transition area. They have to be used signed in the formula

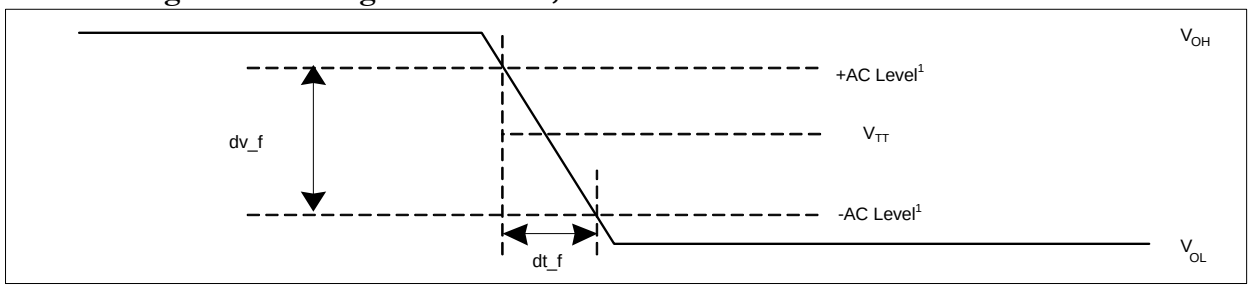
Load Circuit and Voltage Waveforms (cont'd.)

Figure 33. Calculating the virtual V_{TT} crossing point



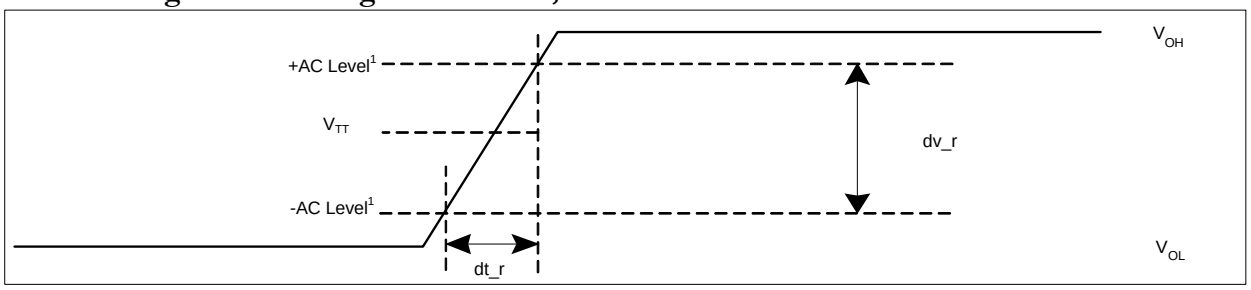
Load Circuit and Voltage Waveforms (cont'd.)

Figure 34. Voltage Waveforms; HIGH-to-LOW Slew Rate Measurement



Notes:
1. AC Level = 150 mV (1.5 V Operation) and 135 mV (1.35 V Operation)

Figure 35. Voltage Waveforms; LOW-to-HIGH Slew Rate Measurement

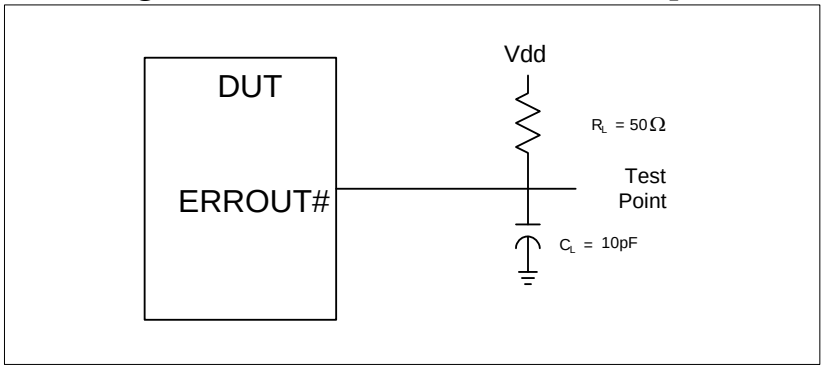


Notes:
1. AC Level = 150 mV (1.5 V Operation) and 135 mV (1.35 V Operation)

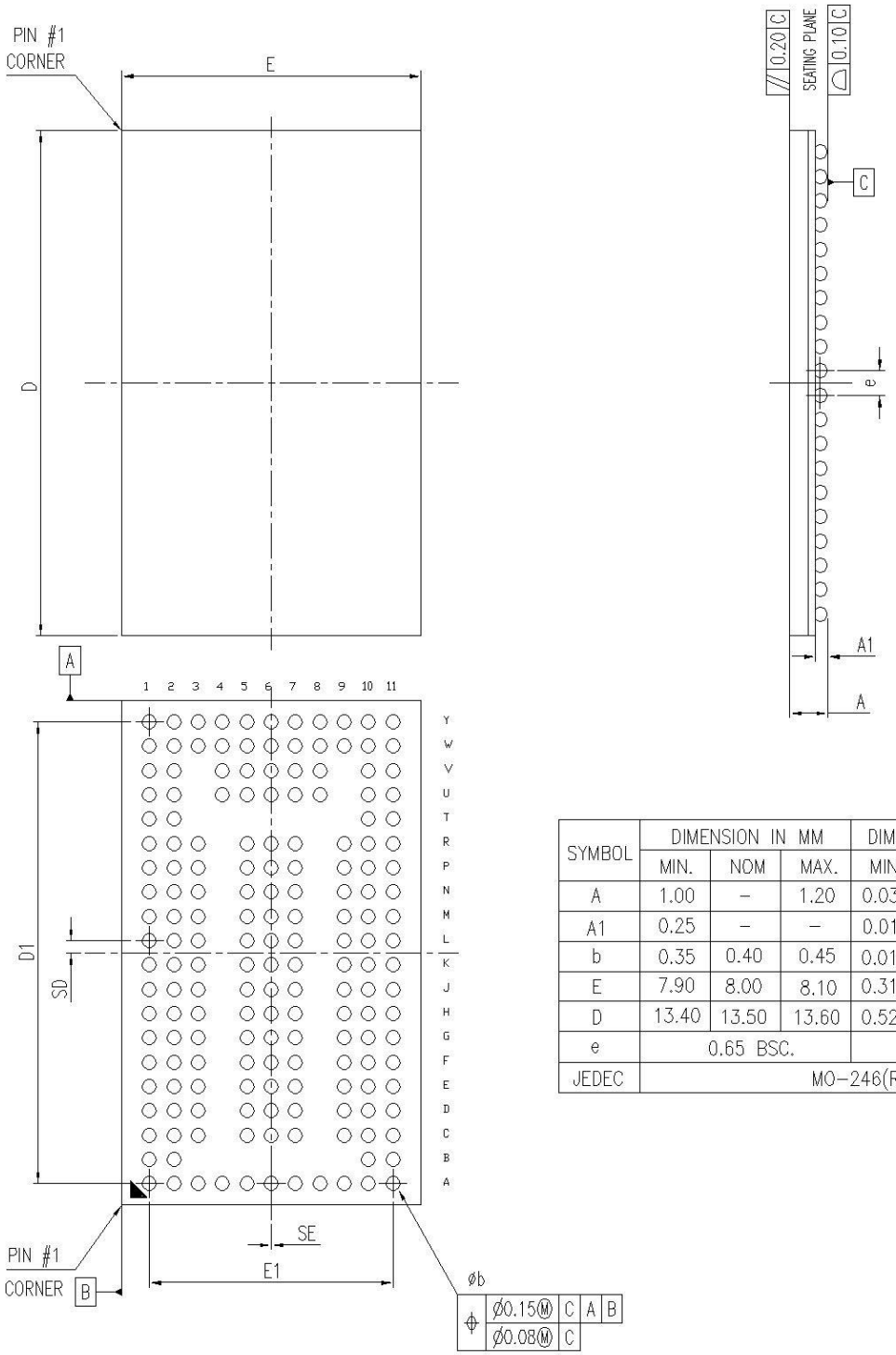
Parity Error Output Measurement Information

All input pulses are supplied by generators having the following characteristics: 300 MHz ≤ PRR ≤ 810 MHz; Zo = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified.

Figure 36. Load Circuit; ERROUT# Output



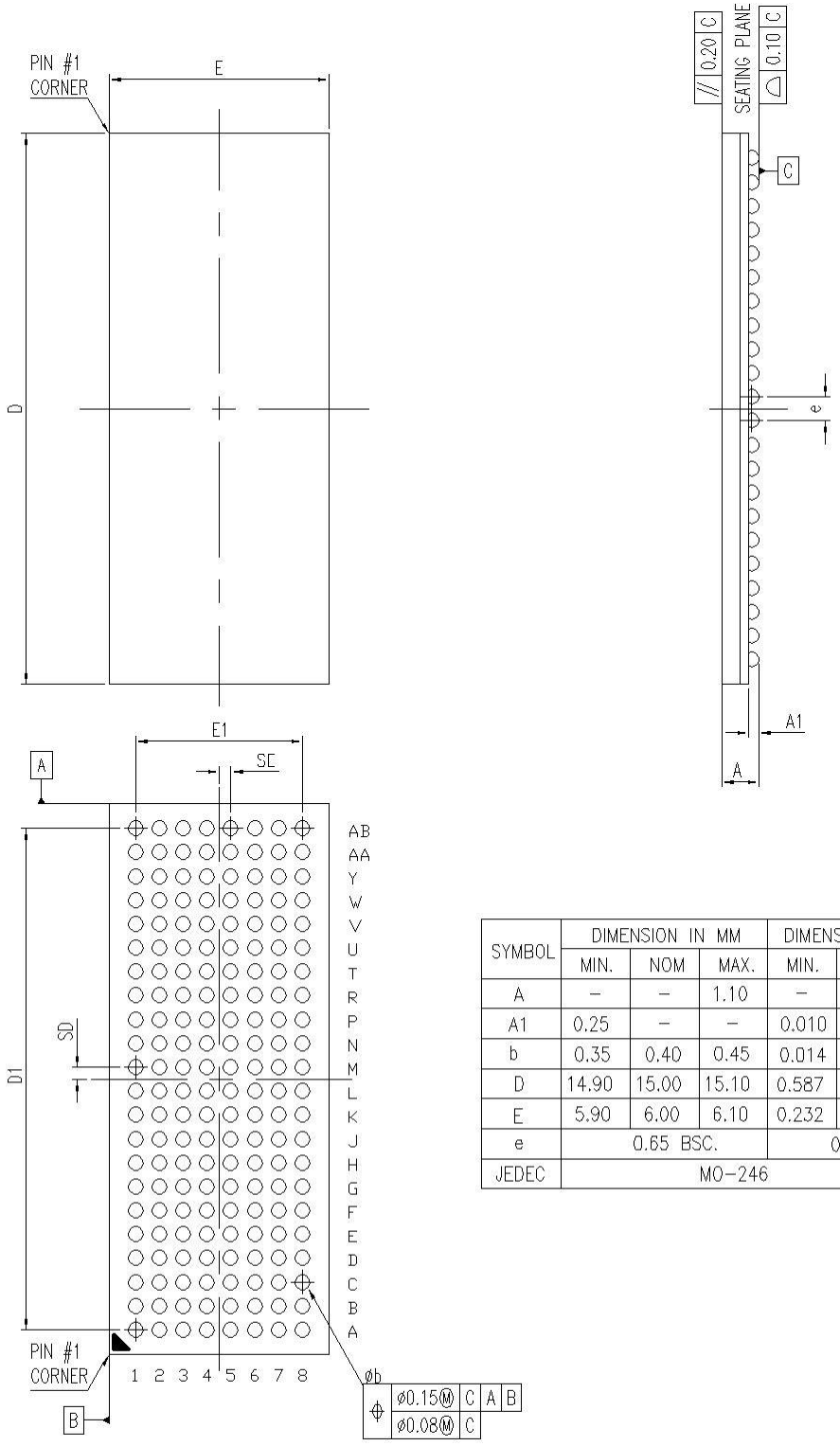
176-Ball TFBGA Package Outline Drawing (MO-246F)



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	1.00	–	1.20	0.039	–	0.047
A1	0.25	–	–	0.010	–	–
b	0.35	0.40	0.45	0.014	0.016	0.018
E	7.90	8.00	8.10	0.311	0.315	0.319
D	13.40	13.50	13.60	0.528	0.531	0.535
e	0.65 BSC.			0.026 BSC.		
JEDEC	MO-246(REF.)					

N	SD(mm)	SD (mm)	D1 (mm)	E1 (mm)	JEDEC(REF)
176	0.325 BSC.	0.00 BSC.	12.35 BSC.	6.50 BSC.	

176-Ball TFBGA Package Outline Drawing (MO-246B)



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	–	–	1.10	–	–	0.043
A1	0.25	–	–	0.010	–	–
b	0.35	0.40	0.45	0.014	0.016	0.018
D	14.90	15.00	15.10	0.587	0.591	0.594
E	5.90	6.00	6.10	0.232	0.236	0.240
e	0.65 BSC.			0.026 BSC.		
JEDEC	MO-246					

N	SE (mm)	SD (mm)	E1 (mm)	D1 (mm)	JEDEC(Ref.)
176	0.325 BSC.	0.325 BSC.	4.55 BSC.	13.65 BSC.	MO-246B

Part Number Selection Table

This register is certified for use on the Raw Cards listed below as defined in JESD21-C, DDR3(L) Registered DIMM Design Specification.

Inphi Product Part Number	RDIMM Module	Speed Bin
INSSTE32882LV-GS01	A, B, C, D, E, F, G, H, J, T, K, L, M, N, U, V, W, Y	800, 1066, 1333
INSSTE32882LV-GS02	A, B, C, D, E, F, G, H, J, T, K, L, M, N, U, V, W, Y	800, 1066, 1333, 1600

Solder Reflow Profile

These products will meet the specifications in this data sheet when manufactured in accordance with JESD22-A113D. This product must be manufactured using the lead-free solder reflow profile.
The solder ball composition is Sn 96.5-98.5 % / Ag 1.0-3.0 % / Cu 0.5 %

Patent Pending Notification

These products include technology that is covered by one or more patent applications.

Package Marking Description

Line	Description	Example Characters	Explanation
1	Manufacturer	Inphi	Manufacturer Logo
2	Product	IN SSTE32882LV G S02	Manufacturer (IN=Inphi) Product Number Material Set (N=Normal, L=Lead Free, G=Green) Inphi Internal Use
3	Lot	A BBBBB CC	Wafer Fab Site Wafer Lot Number Assembly Lot Number
4	Date	WW YY	Assembly Week Assembly Year

Ordering Information

Part No.	Description
INSSTE32882LV – GS01	DDR3(L)-800, 1066, 1333 Registering Clock Driver with Parity Checking
INSSTE32882LV – GS02	DDR3(L)-800, 1066, 1333, 1600 Registering Clock Driver with Parity Checking
INSSTE32882LV – GS02[F]	DDR3(L)-800, 1066, 1333, 1600 Registering Clock Driver with Parity Checking

All versions of the '882 register can be ordered in the following package type:

G[S0X] = Green (lead and halogen-free) 176 Ball TFBGA (8.0 mm x 13.5 mm)
G[S0X]F = Green (lead and halogen-free) 176 Ball TFBGA (6.0 mm x 15.0 mm)
For example, the ***INSSTE32882LV-GS02F*** is a 176 ball TFBGA green package version of the INSSTE32882LV

For each customer application, customer's technical experts must validate all parameters. Inphi Corporation reserves the right to change product specifications contained herein without prior notice. No liability is assumed as a result of the use or application of this product. No circuit patent licenses are implied. Contact Inphi Corporation's marketing department for the latest information regarding this product.

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- E-mail: products@inphi-corp.com

Visit us on the Internet at: http://www.inphi-corp.com

Qualification Notification

The INSSTE32882LV has passed all qualification tests required by JESD47.

Inphi Corporation will honor the full warranty as outlined in Section 5 of Inphi's Standard Customer Purchase Order Terms and Conditions.

Version Updates

Version 1.0 (dated 2008-04-14)

Initial Version

From Version 1.0 to 1.1 (dated 2009-01-12)

1. Added "Preliminary" watermark to the document.
2. Updated -GS02 part numbering throughout the document.
3. Updated DDR3-1600 and DDR3L specifications per latest JEDEC 882 pass/hold document throughout the document.
4. Updated Applications section and Features section (page 1).
5. Updated Initialization section (pages 2 and 4).
    a. Updated text, tables 1 and 2 and footnotes.
6. Updated Reset Initialization with Stable Power section, Tables 3 and 4 (page 6).
7. Updated Parity Timing Scheme Waveforms section (page 8).
8. Updated Register CKE Power Down with IBT Off section and Figure 9 footnotes (page 10 - 11).
9. Updated Register CKE Power Down with IBT On section and Figure 10 footnotes (page 11 - 12).
10. Updated Clock Stopped Power Down Mode section and footnotes (page 13-15).
11. Added Pinout Configuration for Narrow Package and Tables 8 – 12 (pages 25 – 30).
12. Updated PLL Function Table 18 (page 37).
13. Updated Control Word Decoding section, Tables 19, 20 (page 38-39).
14. Added Tables 29 and 30 (page 46).
15. Updated Absolute Maximum Ratings, Table 31, footnote 3 (page 49).
16. Updated DC and AC Specifications (pages 50 – 58).
    a. Updated Operating Conditions, Table 32.
        i. Added footnotes 9-11.
    b. Updated DC Specifications, Tables 33 - 34.
    c. Updated Timing Requirements, Table 35.
    d. Added Figure 23.
    e. Updated AC Specifications, Table 36, footnotes.
17. Updated Output Buffer Characteristics, Table 37 (page 59 - 60).
    a. Updated Table 37.
    b. Added text and Tables 38 – 39.
18. Updated Clock Driver Characteristics (page 61 – 65).
    a. Updated Table 40 and footnotes.
    b. Updated Figure 25 footnotes.
    c. Updated Table 41 and footnotes.
19. Updated Load Circuit and Voltage Waveforms section (pages 67 – 69).
    a. Added Figures 32 and 33.
20. Added 176 ball TFBGA Package Outline Drawing (MO-246B) (page 72).
21. Updated Part Number Selection table (page 73).
22. Updated Solder Reflow Profile section (page 73).
23. Added Package Marking Description section (page 74).
24. Updated Ordering Information section (page 75).
25. Removed tPDM table from Errata Notification (page 76).

From Version 1.1 to 1.2 (dated 2009-04-20)

1. Removed "Preliminary" watermark from document.
2. For 1.35 V references throughout document, changed "DDR3" to "DDR3L".
3. Updated Features section (page 1):
    a. Updated 2nd bullet and added sentence "Specifications highlighted in blue exceed JEDEC specifications." and highlighted specific specs throughout document.
    b. Changed HBM from 2000 V to 4000 V

Version Updates (cont'd.)

From Version 1.1 to 1.2 (dated 2009-04-20) (cont'd.)

4. Updated "Clock Stopped Power Down Mode" section (pages 13-14):
    a. Updated Clock Stopped Power Down Mode Exit section:
        i. Corrected typo: changed 2nd sentence from "After t_{ACT}, a frequency…" to "After that, a frequency…"
        ii. In third sentence, changed sentence from "Within t_{ACT}, after CK and CK# resumes normal operation, only the QxODTn outputs …" to "Within t_{ACT}, after CK and CK# resumes normal operation, the INSSTE32882LV outputs…"
5. Updated "Pinout Configuration" section (page 21):
    a. Added 2nd sentence that reads: "It is using mechanical outline MO-246F."
6. Corrected pinout for J2, J7, L2 and L7 in Table 11 and Table 12 (pages 29 - 30).
7. Updated Table 18: Changed Inputs column header "QEn" to "OEn"
8. Changed RC4[DA2] and RC5[DA2] states from "L" to "H" in Table 19 (page 38).
9. Updated Table 21 in Control Word Decoding section (page 40):
    a. For DBA0 Input, added "including Y1/Y1# and Y3/Y3#" to Definition column.
    b. For DBA1 Input, added "including Y0/Y0# and Y2/Y2#" to Definition column.
10. Updated RC2 description (page 41):
    a. Last sentence changed from "…, IBT is turned off on all inputs, except the DCSn# and DODTn inputs." to "…, IBT is controlled by RC8 (refer to table 27)."
11. Updated Table 28 in Control Word Decoding section (page 45):
    a. Added new paragraph for RC8.
    b. For Inputs XX0X and XX1X, added "Reserved" in Definition column.
12. Updated Table 29 in Control Word Decoding section (page 46):
    a. For Inputs X101, X110, and X111, added "Reserved" in Encoding column.
13. Updated Table 30 in Control Word Decoding section (page 46):
    a. For Inputs 00XX, 01XX, 10XX, and 11XX, added "Reserved" in Definition column.
14. Updated DC and AC Specifications (pages 50 – 58).
    a. Updated Table 32 in Operating Conditions section (page 51):
        i. For parameters I_{OH} and I_{OL}, updated Conditions by changing "ERROR#" to ERROUT#".
    b. Updated DC Specifications, Table 33 (page 52):
        i. Changed Max spec for "Input current" parameter with conditions = "Data inputs[1], V_I = V_{DD} or GND" from "TBD" to "±5 µA".
        ii. Updated "Static operating current":
            1. Expanded conditions, by adding "MIRROR = V_{DD}, RC8=x111 (IBT Off), CK/CK#=Vil(static)" as part of the conditions
            2. Updated max spec from TBD to 15 mA.
        iii. Updated I_{DDD} (input clock only):
            1. Added parameter for 1.5 V operation with typ spec = 0.150 mA/MHz
            2. Added parameter for 1.35 V operation with typ spec = 0.135 mA/MHz
        iv. Updated I_{DDD} (per each data input):
            1. Added parameter for 1.5 V operation with typ spec = 0.003 mA/MHz
            2. Added parameter for 1.35 V operation with typ spec = 0.003 mA/MHz
        v. Removed "Static operating current PLL (digital and analog) section" parameters and their specifications.
    c. Updated Timing Requirements, Table 35 (page 54):
        i. Changed Setup time parameter's min specs:
            1. For DDR3(L)-800/1066/1333, changed from 100 ps to 50 ps
            2. For DDR3(L)-1600, changed from 50 ps to 30 ps

Version Updates (cont'd.)

From Version 1.1 to 1.2 (dated 2009-04-20) (cont'd.)

ii. Changed Hold time parameter's min specs:
1. For DDR3(L) 800/1066/1333, changed from 175 ps to 0 ps
2. For DDR3(L) 1600, changed from125 ps to 0 ps

d. Updated AC Specifications, Table 36 (page 58):
i. Updated "Propagation delay, single-bit switching parameter
1. For 1.5 V Operation, changed min specs from 0.65 ns to 0.75 ns.
2. For 1.35 V Operation, changed min specs from 0.65 ns to 0.85 ns
ii. Removed footnote #4.

e. Moved Figure 24 from page 59 to page 58.

15. Updated Output Buffer Characteristics section, Table 38 (page 59):
a. Removed text and three bullets that referred to output groupings.
b. Removed all references to "Output Slew Rate" and its specifications.

16. Updated Input Buffer Characteristics, Table 39 (page 60):
a. Changed footnote 2 from "(R_{IBT-UP} and $R_{IBT-DOWN}$) * 100 ≤ |5%|" to "(1 - R_{IBT-UP} / $R_{IBT-DOWN}$) * 100 ≤ |5%|".

17. Updated Clock Driver Characteristics (pages 61 – 65)
a. Updated Table 40 (page 61):
i. Updated Cycle-to-cycle period jitter parameter (t_{jit}(cc+)):
1. For DDR3(L)-800, changed min spec from 40 ps to 35 ps.
2. For DDR3(L)-1066, changed min spec from 40 ps to 35 ps.
3. For DDR3(L)-1333, changed min spec from 40 ps to 35 ps.
ii. Updated Cycle-to-cycle period jitter parameter (t_{jit}(cc-)):
1. For DDR3(L)-800, changed min spec from -40 ps to -35 ps.
2. For DDR3(L)-1066, changed min spec from -40 ps to -35 ps.
3. For DDR3(L)-1333, changed min spec from -40 ps to -35 ps.
iii. Updated Stabilization time parameter:
1. For DDR3(L)-800:
a. Changed max spec from 6 us to 4 us.
2. For DDR3(L)-1066/1333
a. Changed max spec from 6 us to 3 us.
3. For DDR3(L)-1600:
a. Changed max spec from 6 us to 2 us.
iv. Updated Dynamic phase offset parameter:
1. For DDR3(L)-800/1066/1333:
a. Changed min and max specs from 50 ps to 35 ps.
2. For DDR3(L)-1600:
a. Changed min and max specs from 40 ps to 25 ps.
v. Updated Yn clock period jitter:
1. For DDR3(L)-800/1066/1333:
a. Changed min spec from -40 ps to -30 ps
b. Changed max spec from 40 ps to 30 ps
2. For DDR3(L)-1600:
a. Changed min spec from -30 ps to -25 ps
b. Changed max spec from 30 ps to 25 ps
vi. Updated Yn clock half-period jitter:
1. For DDR3(L)-800/1066/1333:
a. Changed min spec from -50 ps to -35 ps
b. Changed max spec from 50 ps to 35 ps

Version Updates (cont'd.)

From Version 1.1 to 1.2 (dated 2009-04-20) (cont'd.)

2. For DDR3(L)-1600:
    a. Changed min spec from -40 ps to -30 ps
    b. Changed max spec from 40 ps to 30 ps

vii. Updated t_{STAOFF}, Average delay through the register between the input clock and output clock parameters:
1. For 1.5 V Operations:
    a. For Conditions = Standard ½-Clock pre-Launch $T_{STAOFF}=T_{PDM} + 1/2 T_{CK}$:
        i. Changed min spec:
            1. For DDR3(L)-800: from 1.90 ns to 2.00 ns
            2. For DDR3(L)-1066: from 1.59 ns to 1.69 ns
            3. For DDR3(L)-1333: from 1.40 ns to 1.50 ns
            4. For DDR3(L)-1600: from 1.28 ns to 1.38 ns
    b. For Conditions = ¾ Clock pre-Launch $T_{STAOFF}=T_{PDM} + 3/4 T_{CK}$ Changed min spec:
            1. For DDR3(L)-800: from 2.53 ns to 2.63 ns
            2. For DDR3(L)-1066: from 2.06 ns to 2.16 ns
            3. For DDR3(L)-1333: from 1.77 ns to 1.87 ns
            4. For DDR3(L)-1600: from 1.59 ns to 1.69 ns
2. For 1.35 V Operations:
    a. For Conditions = Standard ½-Clock pre-Launch $T_{STAOFF}=T_{PDM} + 1/2 T_{CK}$:
        i. Changed min spec:
            1. For DDR3(L)-800: from 1.90 ns to 2.10 ns
            2. For DDR3(L)-1066: from 1.59 ns to 1.79 ns
            3. For DDR3(L)-1333: from 1.40 ns to 1.60 ns
            4. For DDR3(L)-1600: from 1.28 ns to 1.48 ns
    b. For Conditions = ¾ Clock pre-Launch $T_{STAOFF}=T_{PDM} + 3/4 T_{CK}$
        i. Changed min spec:
            1. For DDR3(L)-800: from 2.53 ns to 2.73 ns
            2. For DDR3(L)-1066: from 2.06 ns to 2.26 ns
            3. For DDR3(L)-1333: from 1.77 ns to 1.97 ns
            4. For DDR3(L)-1600: from 1.59 ns to 1.79 ns

vii. Updated t_{DYNOFF}, Maximum variation in delay between the input & output clock parameter:
1. Changed max spec:
    a. For DDR3(L) -800: from 160 ps to 70 ps
    b. For DDR3(L) -1066: from 130 ps to 65 ps
    c. For DDR3(L) -1333: from 110 ps to 60 ps
    d. For DDR3(L) -1600: from 90 ps to 55 ps

b. Updated Table 41 (page 65):
i. Removed column with DDR3-1600 min/max specs
ii. Changed column heading from "DDR3-800/1066/1333" to "Band2"
ii. Updated Cycle-to-cycle period jitter parameter:
1. Changed max spec from 160 ps to 120ps
iv. Updated Fractional clock output skew parameter:
1. Changed max spec from TBD to 50 ps
v. Updated Yn clock period jitter parameter:
1. Changed min spec from -160 ps to -75 ps
2. Changed max spec from 160 ps to 75 ps

Version Updates (cont'd.)

From Version 1.1 to 1.2 (dated 2009-04-20) (cont'd.)

vi. Updated Yn clock half-period jitter parameter:
   1. Changed min spec from -200 ps to -75 ps
   2. Changed max spec from 200 ps to 75 ps

vii. Updated Qn output to clock tolerance (standard ½ clock pre-launch) parameter:
   1. For Output inversion enabled conditions: changed max spec from TBD to 250 ps
   2. For Output inversion disabled conditions: changed max spec from TBD to 300 ps

viii. Updated Qn output to clock tolerance (standard ¾ clock pre-launch) parameter:
   1. For Output inversion enabled conditions: changed max spec from TBD to 250 ps
   2. For Output inversion disabled conditions: changed max spec from TBD to 300 ps

ix. Updated t_{DYNOFF} parameter: changed max spec from 1000 ps to 150 ps.

18. Removed the Errata Notification section because it only applied to the INSSTE32882LV-GS01, which was EOL'd.

From Version 1.2 to 1.3 (dated 2009-07-15)

1. Updated per latest JEDEC 882 pass/hold document throughout the document.
2. Added note 6, table 4 (page 6)
3. Updated 2nd paragraph (page 20)
   a. Added sentence, "During control word write, at least one DCKEn must be asserted."
   b. Changed sentence from "If register CKE power down mode is enabled, at least one DCKEn input must be HIGH for a valid access" to "If register CKE power down mode is disabled, DCKEn input is a don't care (either HIGH or LOW)."
4. Edited last sentence of 2nd paragraph (page 41)
5. Updated Figure 20 (page 47)
6. Updated footnote #9 (page 51)
   a. Changed "TBD" to "50" for theta-JA for MO-246F.
   b. Changed "TBD" to "47" for theta-JA for MO-246B.
7. Updated DC Specifications (pages 51 – 52)
   a. Updated Table 33
      i. Updated footnote #1.
   b. Updated Table 34
      i. Removed Co parameter.
      ii. Merged Input Capacitance rows for CK/CK#/FBIN/FBIN#.
      iii. Updated footnote #2.
8. Updated Output Buffer Characteristics (page 59)
   a. Updated Table 32
      i. Changed slew rate max spec from 5 V/ns to 5.5 V/ns for 1.5 V Operation.
      ii. Changed slew rate max spec from 4.5 V/ns to 5 V/ns for 1.35 V Operation.
      iii. Updated footnote #1.
9. Updated Package Marking Description (page 73)
   a. Removed "Assembly Site" marking
   b. Updated Figure

Inphi Corporation is an ISO-9001:2000 Certified Manufacturer