# JEDEC STANDARD

## Definition of the SSTE32882 Registering Clock Driver with Parity and Quad Chip Selects for DDR3/DDR3L/DDR3U RDIMM 1.5 V/1.35 V/1.25 V Applications



## JESD82-29A.01

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# DEFINITION OF THE SSTE32882 REGISTERING CLOCK DRIVER WITH PARITY AND QUAD CHIP SELECTS FOR DD3/DDR3L/DDR3U RDIMM 1.5 V, 1.35 V, OR 1.25 V APPLICATIONS

(From JEDEC Board Ballot JCB-10-55, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

## 1 Scope

This standard defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the SSTE32882 registered buffer with parity for driving address and control nets on DDR3/DDR3L/DDR3U RDIMM applications.

The purpose is to provide a standard for the SSTE32882 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE The designation SSTE32882 refers to the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

## 2 Device Standard

### 2.1 Description

This 28-bit 1:2 or 26-bit 1:2 and 4-bit 1:1 registering clock driver with parity is designed for 1.5 V, 1.35 V, or 1.25 V $V_{DD}$ operation.

All inputs are 1.5 V, 1.35 V, or 1.25 V CMOS compatible. All outputs are 1.5 V, 1.35 V, or 1.25 V CMOS drivers optimized to drive single terminated 25..50 Ohms traces in DDR3/DDR3L/DDR3U RDIMM applications. The clock outputs Yn and Yn# and control net outputs QnCKEn, QnCSn# and QnODTn can be driven with a different strength and skew to compensate for different loading and equalize signal travel speed.

The SSTE32882 has two basic modes of operation associated with the Quad Chip Select Enable (QCSEN#) input. When the QCSEN# input pin is open (or pulled HIGH), the component has two chip select inputs, DCS0# and DCS1#, and two copies of each chip select output, QACS0#, QACS1#, QBCS0# and QBCS1#. This is the "QuadCS disabled" mode. When the QCSEN# input pin is pulled LOW, the component has four chip select inputs DCS[3:0]#, and four chip select outputs, QCS[3:0]#. This is the "QuadCS enabled" mode. Through the remainder of this specification, DCS[n:0]# will indicate all of the chip select inputs, where n=1 for QuadCS disabled, and n=3 for QuadCS enabled. QxCS[n:0]# will indicate all of the chip select outputs.

The SSTE32882 operates from a differential clock (CK and CK#). Data are registered at the crossing of CK going HIGH, and CK# going LOW. The data could be either re-driven to the outputs once exactly one of the input signals DCS[n:0]# is driven LOW or it could be used to access device internal control registers when certain input conditions are met. The control word mechanism is described in more detail in 2.2.

Based on control register settings the device can change its output characteristics to match different DIMM net topologies. The timing can be changed to compensate for different flight time of signals within the target application. By disabling unused outputs the power consumption is reduced.

### 2.1.1 Initialization

The DDR3/DDR3L/DDR3U RCD (Ultra Low Voltage) SSTE32882 can be powered-on at 1.5 V, 1.35 V, or 1.25 V. After the voltage transition, stable power is provided for a minimum of 200 µs with RESET# asserted. When the reset input RESET# is LOW, all input receivers are disabled, and can be left floating. Therefore the reference voltage (VREF) doesn't need to be stable. In addition, when RESET# is LOW, all control registers are restored to their default states. The outputs QACKE0, QACKE1, QBCKE0 and QBCKE1 must drive LOW during reset. All other outputs must float. As long as the RESET# input is pulled LOW the register is in low power state and input termination is not present. A certain period of time (tACT) before the RESET# input is pulled HIGH the reference voltage needs to be stable within specification, the clock input signal must be stable, the register inputs DCS[n:0]# must be pulled HIGH to prevent accidental access to the control registers and DCKE0 as well as DCKE1 must be pulled LOW. After reset and after the stabilization time ($t_{STAB}$) the register must meet the input setup- and hold specification, as well as accept and transfer input signals to the corresponding outputs. The RESET# input must always be held at a valid logic level once the input clock is present.

To ensure defined outputs from the register before a stable clock has been supplied, the register must enter the reset state during power-up. It may leave this state only after a **LOW** to **HIGH** transition on RESET# while a stable clock signal is present on CK and CK#. In the DDR3 RDIMM application, RESET# is specified to be completely asynchronous with respect to CK and CK#. Therefore, no timing relationship can be guaranteed between the two.

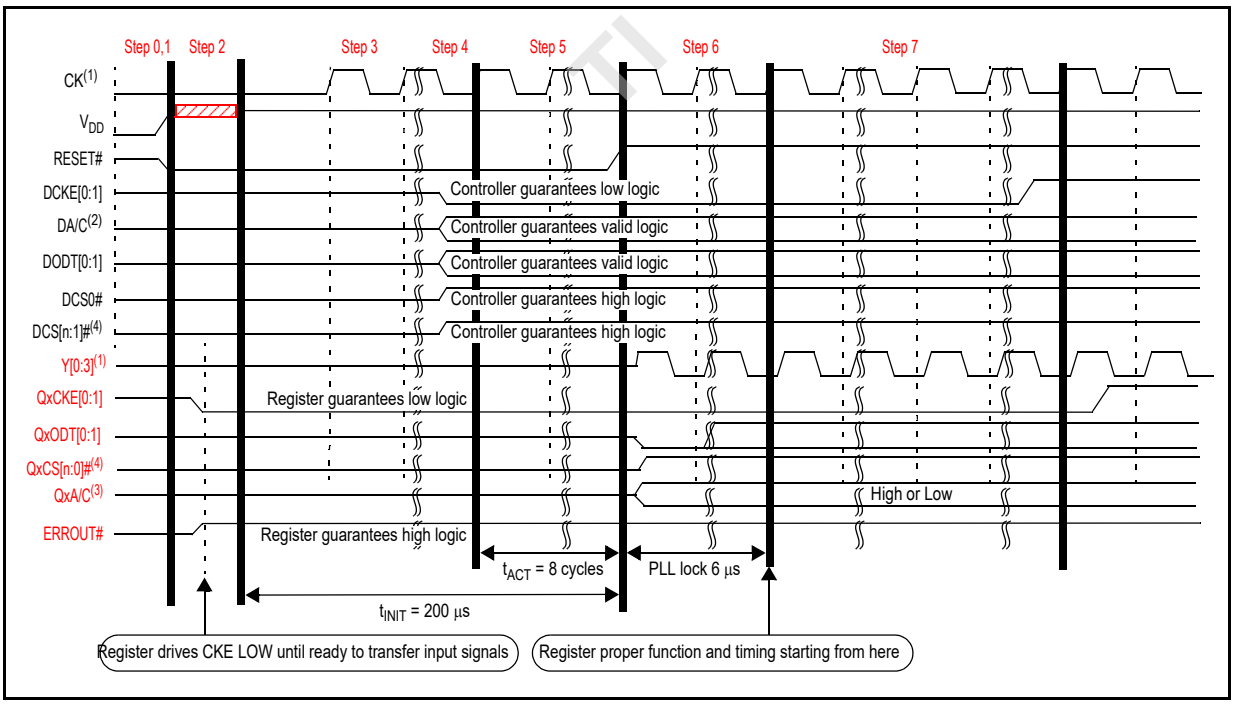



**Figure 1 — Timing of Clock and Data During Initialization Sequence**

NOTE 1 CK# is left out for better visibility

NOTE 2 DCKE0, DCKE1, DODT0, DODT1, DCS0# and DCS1# are not included in this range

NOTE 3 QxCKEn, QxODTn, QxCSn# are not included in this range.

NOTE 4 n = 1 for QuadCS disabled mode, n = 3 for QuadCS enabled mode

### 2.1.1 Initialization (cont'd)

From a device perspective, the initialization sequence must be as shown in Table 1.

**Table 1 — SSTE32882 Device Initialization Sequence[1]**

| Step | Power | Inputs: Signals Provided by the Controller | | | | | | | | Outputs: Signals Provided by the Device | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | VDD, AVDD, PVDD | RESET# | Vref | DCS# [n:0][2] | DODT [0:1] | DCKE [0:1] | DA/C | PAR_IN | CK CK# | QCS# [n:0][2] | QODT [0:1] | QCKE [0:1] | QxA/C | ERR OUT# | Y[0:3] Y#[0:3] | FB $OUT^3$ |
| 0 | 0V | X or Z | X or Z | X or Z | X or Z | X or Z | X or Z | X or Z | X or Z | Z | Z | Z | Z | Z | Z | Z |
| 1 | 0-->$V_{DD}$ | X or Z | X or Z | X or Z | X or Z | X or Z | X or Z | X or Z | L | X or Z | X or Z | X or Z | X or Z | X or Z | X or Z | X or Z |
| 2[4] | VDD<br>1.5 V-->1.35 V<br>1.35 V-->1.5 V | L | X or Z | X or Z | X or Z | X or Z | X or Z | X or Z | L | Z | Z | L[5] | Z | H5 | Z | Z |
| 3 | $V_{DD}$ | L | X or Z | X or Z | X or Z | X or Z | X or Z | X or Z | running | Z | Z | L | Z | H | Z | Z |
| 4 | $V_{DD}$ | L | X or Z | H | X or Z | L | X or Z | X or Z | running | Z | Z | L | Z | H | Z | Z |
| 5 | $V_{DD}$ | L | stable voltage | H | X | L | X | X | running | Z | Z | L | Z | H | Z | Z |
| 6 | $V_{DD}$ | H | stable voltage | H | X | L | X | X | running | H | L[6] | L | X | H | running | running |
| 7[7] | $V_{DD}$ | H | stable voltage | H | X | X | X | X | running | After Step 6 (Step 7 and beyond), the device outputs are as defined in the device Function Tables (see Table 12, Table 14 and Table 16). | | | | | | |

NOTE 1 X = Logic LOW or logic HIGH. Z = floating.
NOTE 2 n = 1 for QuadCS disabled mode, n = 3 for QuadCS enabled mode
NOTE 3 The feedback clock (FBOUT and FBOUT#) pins may or may not be actively driven by the device.
NOTE 4 The system may power up using either 1.5 V, 1.35 V or 1.25 V. The BIOS reads the SPD and adjusts the voltage if needed. Stable power is provided for a minimum of 200 µs with RESET# asserted.
NOTE 5 QxCKEn and ERROUT# will be driven to these logic states by the register after RESET# is driven LOW and VDD is 1.5 V, 1.35 V or 1.25 V (nominal).
NOTE 6 This indicates the state of QxODTx after RESET# switches from **LOW**-to-HIGH and before the rising CK edge (falling CK# edge). After the first rising CK edge, within ($t_{STAB}$ - $t_{ACT}$) µs, the state of QxODTx is a function of DODTx (HIGH or **LOW**).
NOTE 7 Step 7 is a typical usage example and is not a register requirement.

As part of the initialization all control words are reset to their default state which is "0", except for RC6 and RC7, which are vendor-defined. After initialization, the memory controller does only need to write to those control registers whose contents need to be changed.

#### 2.1.1.1 Reset Initialization with Stable Power

The timing diagram in Figure 1 depicts the initialization sequence with stable power and clock. This will apply to the situation when we have a soft reset in the system. RESET# will be asserted for minimum 100ns. This RESET# timing is based on DDR3 DRAM Reset Initialization with Stable Power requirement, and is a minimum requirement. Actual RESET# timing can vary base on specific system requirement, but it cannot be less than 100ns as required by JESD79-3.

### 2.1.1.1 Reset Initialization with Stable Power (cont'd)

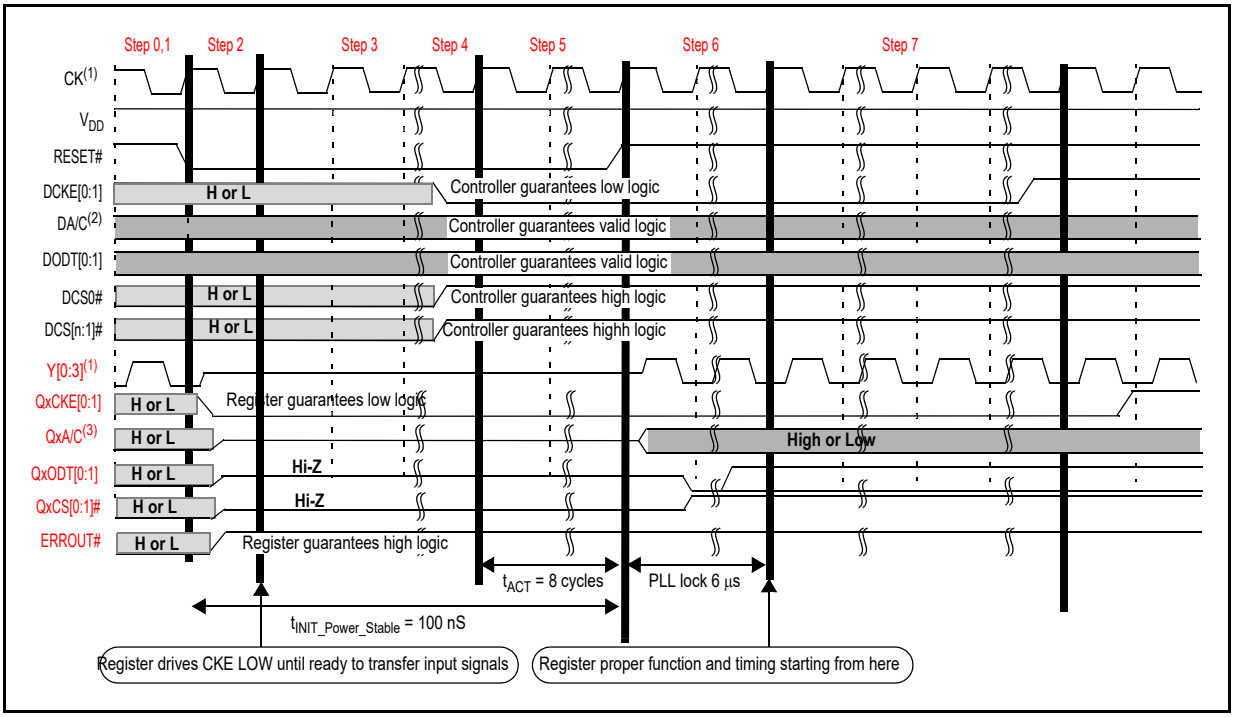



**Figure 2 — Timing of Clock and Data During Initialization Sequence with Stable Power**

NOTE 1 CK# left out for better visibility
NOTE 2 DCKE0, DCKE1, DODT0, DODT1, DCS0# and DCS1# are not included in this range
NOTE 3 QxCKEn, QxODTn, QxCSn# are not included in this range.
NOTE 4 n = 1 for QuadCS disabled mode, n = 3 for QuadCS enabled mode.

**Table 2 — SSTE32882 Device Initialization Sequence[1] when Power and Clock are Stable**

| Step | Power | Inputs: Signals provided by the controller | | | | | | | | Outputs: Signals provided by the device | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | VDD, AVDD, PVDD | RESET# | Vref | DCS# [n:1][2] | DODT [0:1] | DCKE [0:1] | DA/C | PAR_IN | CK CK# | QCS# [0:1] | QODT [0:1] | QCKE [0:1] | QxA/C | ERR OUT# | Y[0:3] Y#[0:3] | FB OUT[3] |
| 0 | VDD | H | stable voltage | X | X | X | X | X | running | X | X | X | X | X | running | running |
| 1 | VDD | H | stable voltage | X | X | X | X | X | running | X | X | X | X | X | running | running |
| 2 | VDD | L | stable voltage | X | X | X | X | X | running | Z | Z | L[4] | Z | H[4] | Z | Z |
| 3 | VDD | L | stable voltage | X | X | X | X | X | running | Z | Z | L | Z | H | Z | Z |
| 4 | VDD | L | stable voltage | H | X | L | X | X | running | Z | Z | L | Z | H | Z | Z |
| 5 | VDD | L | stable voltage | H | X | L | X | X | running | Z | Z | L | Z | H | Z | Z |
| 6 | VDD | H | stable voltage | H | X | L | X | X | running | H | L[5] | L | X | H | running | running |
| 7 | VDD | H | stable voltage | H | X | X | X | X | running | After Step 6 (Step 7 and beyond), the device outputs are as defined in the device Function Tables (see Table 12, Table 14, and Table 16). | | | | | | |

NOTE 1 X = Logic LOW or logic HIGH. Z = floating.
NOTE 2 n = 1 for QuadCS disabled mode, n = 3 for QuadCS enabled mode
NOTE 3 The feedback clock (FBOUT and FBOUT#) pins may or may not be actively driven by the device.
NOTE 4 QxCKEn and ERROUT# will be driven to these logic states by the register after RESET# is driven LOW and $V_{DD}$ is nominal.
NOTE 5 This indicates the state of QxODTx after RESET# switches from LOW-to-HIGH and before the rising CK edge (falling CK# edge). After the first rising CK edge, within ($t_{STAB}$ - $t_{ACT}$) µs, the state of QxODTx is a function of DODTx (HIGH or LOW).

### 2.1.2 Parity

The SSTE32882 includes a parity checking function. The SSTE32882 accepts a parity bit from the memory controller at its input pin PAR_IN one cycle after the corresponding data input, compares it with the data received on the D-inputs and indicates on its open-drain ERROUT# pin (active **LOW**) whether a parity error has occurred. The computation only takes place for data which is qualified by at least one of the DCS[n:0]# signals being **LOW**.

If an error occurs, and ERROUT# is driven LOW with the third input clock edge after the corresponding data on the D-inputs. It becomes high impedance with the 5th input clock cycle after the data corresponding with a parity error. In case of consecutive errors ERROUT# becomes high impedance with the 5th input clock cycle after the last data corresponding with a parity error. The DIMM-dependent signals (DCKE0, DCKE1, DCS0#, DCS1#, DODT0 and DODT1) are not included in the parity check computations.

#### 2.1.2.1 Parity Timing Scheme Waveforms

The PAR_IN signal arrives one input clock cycle after the corresponding data input signals. ERROUT# is generated three input clock cycles after the corresponding data is registered. If ERROUT# goes **LOW**, it stays LOW for a minimum of two input clock cycles or until RESET# is driven **LOW**. Figure 3 shows the parity diagram with single parity-error occurrence and assumes the occurrence of only one parity error when data is clocked in at the n input clock cycle (PAR_IN clocked in on the n+1 input clock cycle).

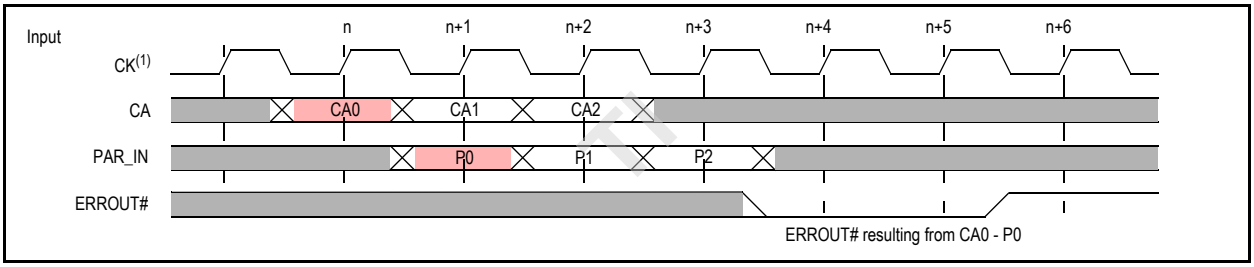



**Figure 3 — Timing of Clock, Data, and Parity Signals**

NOTE 1 CK# left out for better visibility

Figure 4 shows the parity diagram with two consecutive parity-error occurrences and assumes the occurrence of both parity errors when data is clocked in at the n and n+1 input clock cycles (PAR_IN clocked in on the n+1 and n+2 input clock cycles).

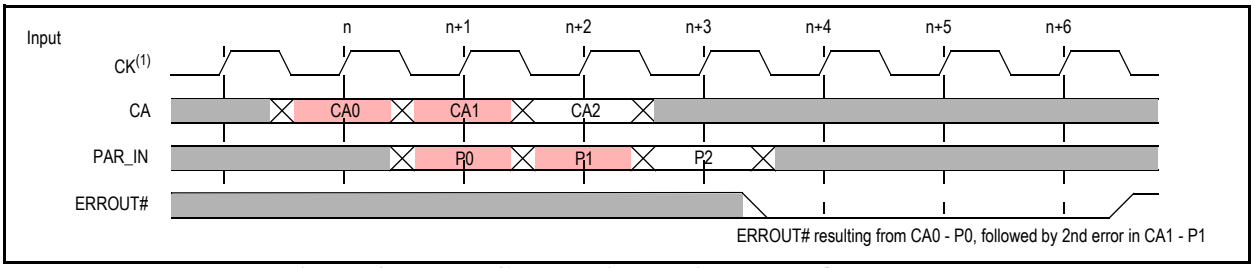



**Figure 4 — Two Consecutive Parity-Error Occurrences**

NOTE 1 CK# left out for better visibility

### 2.1.2.1 Parity Timing Scheme Waveforms (cont'd)

Figure 5 shows the parity diagram with two parity-error occurrences separated by a clock cycle with no error occurrence. The diagram assumes the occurrence of two parity errors when data is clocked in at the n and n+2 input clock cycles (PAR_IN clocked in on the n+1 and n+3 input clock cycles).

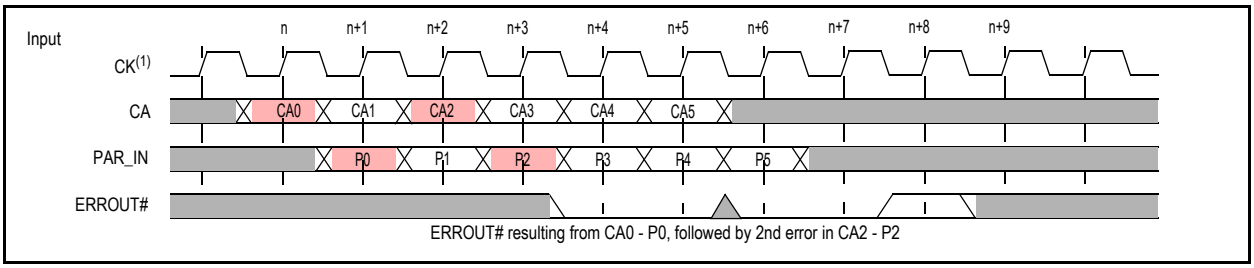



**Figure 5 — Two Parity-Error Occurrences Separated by a Clock Cycle of No Error Occurrence**

NOTE 1 CK# left out for better visibility

Figure 6 shows the parity diagram with two parity-error occurrences separated by two input clock cycles with no error occurrence. The diagram assumes the occurrence of two parity errors when data is clocked in at the n and n+3 input clock cycles (PAR_IN clocked in on the n+1 and n+4 input clock cycles).

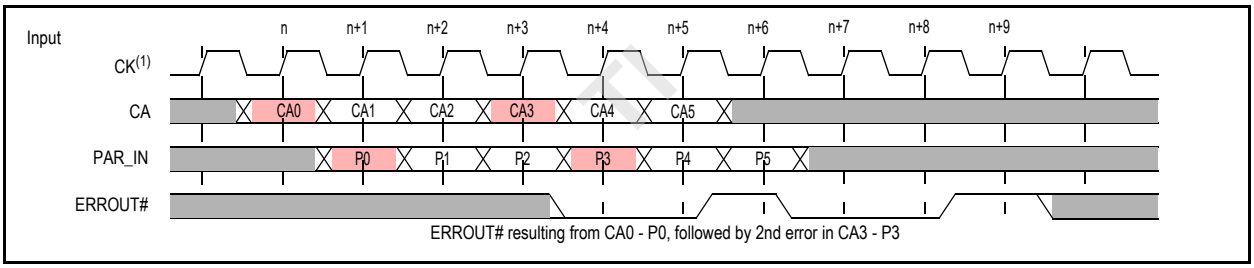



**Figure 6 — Two Parity-Error Occurrences Separated by Two Clock Cycle of No Error Occurrence**

NOTE 1 CK# left out for better visibility

Figure 7 shows the parity diagram with two parity-error occurrences; during chip-select and chip-deselect modes. The diagram assumes the occurrence of both parity errors when data is clocked in at the n and n+1 input clock cycles (PAR_IN clocked in on the n+1 and n+2 input clock cycles). Parity error in the chip-select mode is detected, but parity error in the chip-deselect mode is ignored.

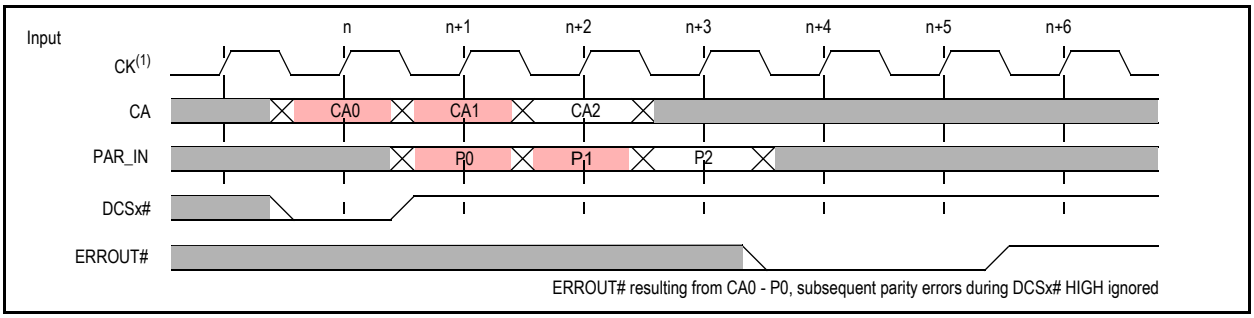



**Figure 7 — Parity-Error Occurrence in Chip-Deselect Mode**

NOTE 1 CK# left out for better visibility

### 2.1.2.1 Parity Timing Scheme Waveforms (cont'd)

Figure 8 shows the parity diagram with two parity-error occurrences; during normal operation and during control register programming. The diagram assumes the occurrence of both parity errors when data is clocked in at the n and n+3 input clock cycles (PAR_IN clocked in on the n+1 and n+4 input clock cycles). The data on the n+3 input clock pulse is intended for the control mode register. Parity error during control mode register programming is detected and the parity functionality is the same as during normal operation. If a parity error occurs, the command is ignored.

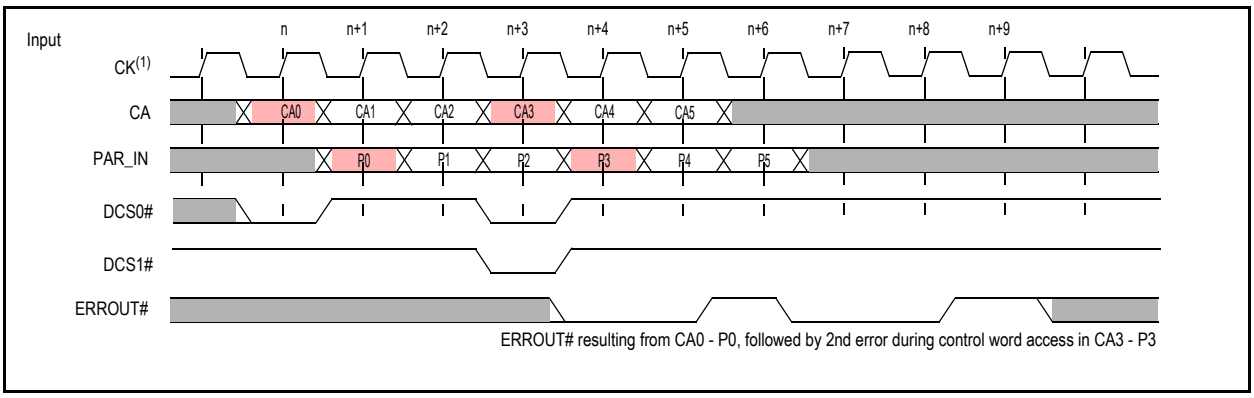



**Figure 8 — Parity-Error Occurrences During Control Word Programming**

NOTE 1 CK# left out for better visibility

### 2.1.3 Power Saving Modes

The device supports different power saving mechanisms.

When both inputs CK and CK# are being held LOW the device stops operation and enters low-power static and standby operation. It stops its PLL and floats all outputs except QACKE0, QACKE1, QBCKE0 and QBCKE1 which are kept driven **LOW**. Before the device is taken out of standby operation by applying a stable input clock signal, the register inputs DCS[n:0]# must be pulled HIGH to prevent accidental access to the control registers and DCKE0 as well as DCKE1 must be pulled LOW for a certain period of time ($t_{ACT}$). The input clock must be stable for a time ($t_{STAB}$) before any access to the device takes place. Stopping the clocks (CK=CK#=**LOW**) will only put the SSTE32882 in the low-power mode and will not clear the content of the Control Words. The command mode registers will reset only when RESET# is driven **LOW**.

A float feature can be enabled by setting the corresponding bit in the control register. This causes the device to monitor all the DCS[n:0]# inputs and to float all outputs corresponding with the chip select gated inputs when all the DCS[n:0]# inputs are HIGH. If any one of the DCS[n:0]# input is **LOW**, the Qn outputs will function normally.

Once all the DCS[n:0]# inputs are HIGH, the gated address command inputs to the register can float to conserve input termination power. DCKE0, DCKE1, DODT0 and DODT1 need to be driven by the system all the time.

The RESET# input has priority over all other power saving mechanisms. When RESET# is driven **LOW**, it will force the Qn outputs to float, the ERROUT# output HIGH, the QACKE0, QACKE1, QBCKE0 and QBCKE1 outputs LOW and disables Input Bus Termination (IBT).

### 2.1.4 Register CKE Power Down

The SSTE32882 monitors both DCKEn input signals and enters into power saving state when it latches LOW on both DCKEn inputs and at least one of the DCKEn input has transitioned from HIGH to **LOW**. If either input Chip Select signal, DCS[n:0]#, is asserted together with DCKEn, the SSTE32882 transfers the corresponding command to its outputs together with QxCKEn **LOW**.

There are two modes of CKE Power Down selected by control word RC9. Bit DBA0 in RC9 indicates whether register turns off IBT or keeps IBT on.

#### 2.1.4.1 Register CKE Power Down with IBT Off

Upon entry into CKE Power Down mode with IBT off, all register input buffers are disabled except for CK/CK#, DCKEn, FBIN/FBIN# and RESET#. Upon entry into CKE Power Down mode with IBT off, IBT will be off on all inputs except DCKEn.. The SSTE32882 disables input buffers within $t_{InDIS}$ clocks after latching both DCKEn **LOW**. In order to eliminate any false parity check error, the PAR_IN input buffer has to be kept active for 1 tCK after the Address and Command input buffers are disabled. After $t_{InDIS}$, the register can tolerate floating input except for CK/CK#, DCKEn and RESET#. The SSTE32882 also disables all its output buffers except for Yn/Yn#, QxODTn, QxCKEn and FBOUT/FBOUT#. The Yn/Yn# and FBOUT/FBOUT# outputs continue to drive a valid phase accurate clock signal. The QxODTn and QxCKEn outputs are driven **LOW**. The register output buffers are hi-z $t_{QDIS}$ clock after QxCKEn is driven **LOW**. This is shown in Figure 9.

### 2.1.4.1 Register CKE Power Down with IBT Off (cont'd)

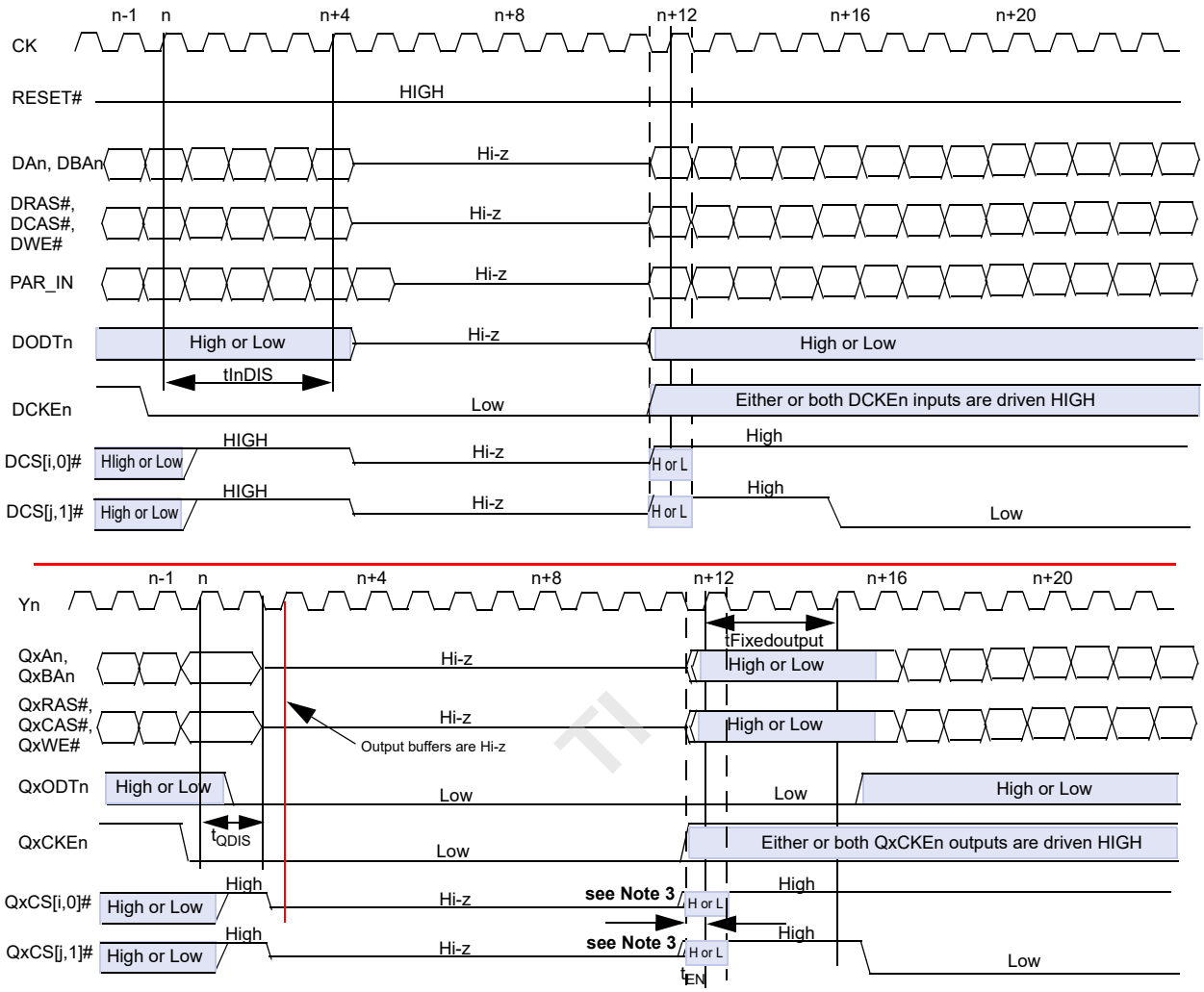



**Figure 9 — Power Down Mode Entry and Exit with IBT Off**

NOTE 1 i, j only apply for QuadCS capable register. When QuadCS is enabled, i = 2, j = 3

NOTE 2 QuadCS disabled: During CKE Power Down Entry/Exit, driving DCS[1:0]# LOW is illegal as it will force SSTE32882 into Register Control Word access mode.

NOTE 3 Upon CKE Power Down exit, QxCSn# may follow DCSn# inputs for maximum of 1 tCK, or be held HIGH for tFIXEDOUTPUT regardless of what DCSn# input level is. For all other operation QxCSn# outputs will follow DCSn# inputs.

To re-enable the register from this power saving state, valid logic levels are required at all register inputs when either or both DCKEn input are driven HIGH. Upon either DCKE0 or DCKE1 input going HIGH, the register immediately starts driving HIGH on the appropriate QxCKEn signal. The QxCSn# signals are driven HIGH and QxODTn signals are driven **LOW**. Other output signals QxRAS#, QxCAS#, QxWE# and QxAddr are driven either HIGH or LOW to ensure stable valid logic on all register outputs when QxCKEn goes HIGH. The register drives output signals to these levels for $t_{Fixedoutput}$ to allow input receivers to be stabilized. After the input receivers are stabilized, the register output follow their corresponding input levels. When exiting CKE power down mode, either one of the Chip select register inputs DCSn# can be asserted for 1 tCK. For QuadCS capable register, when working in quad rank mode, either two of the Chip select register inputs DCSn# can be asserted for 1 tCK. The register guarantees that input receivers are stabilized within $t_{Fixedoutput}$ clocks after DCKEn input is driven HIGH. This is shown in Figure 9.

### 2.1.4.2 Register CKE Power Down with IBT On

Upon entry into CKE Power Down mode with IBT on, all register input buffers are disabled except for CK/CK#, DCKEn, DODTn, FBIN/FBIN# and RESET#. Upon entry into CKE Power Down mode with IBT on, IBT will remain on for all inputs. The SSTE32882 disables input buffers within $t_{InDIS}$ clocks after latching both DCKEn **LOW**. In order to eliminate any false parity check error, the PAR_IN input buffer has to be kept active for 1 tCK after the Address and Command input buffers are disabled. After $t_{InDIS}$, the register can tolerate floating input except for CK/CK#, DCKEn, DODTn and RESET#. The SSTE32882 also disables all its output buffers except for Yn/Yn#, QxODTn, QxCKEn and FBOUT/FBOUT#. The Yn/Yn# and FBOUT/FBOUT# outputs continue to drive a valid phase accurate clock signal. The QxCKEn outputs are driven **LOW**. The register output buffers are hi-z $t_{QDIS}$ clock after QxCKEn is driven **LOW**. This is shown in Figure 10.

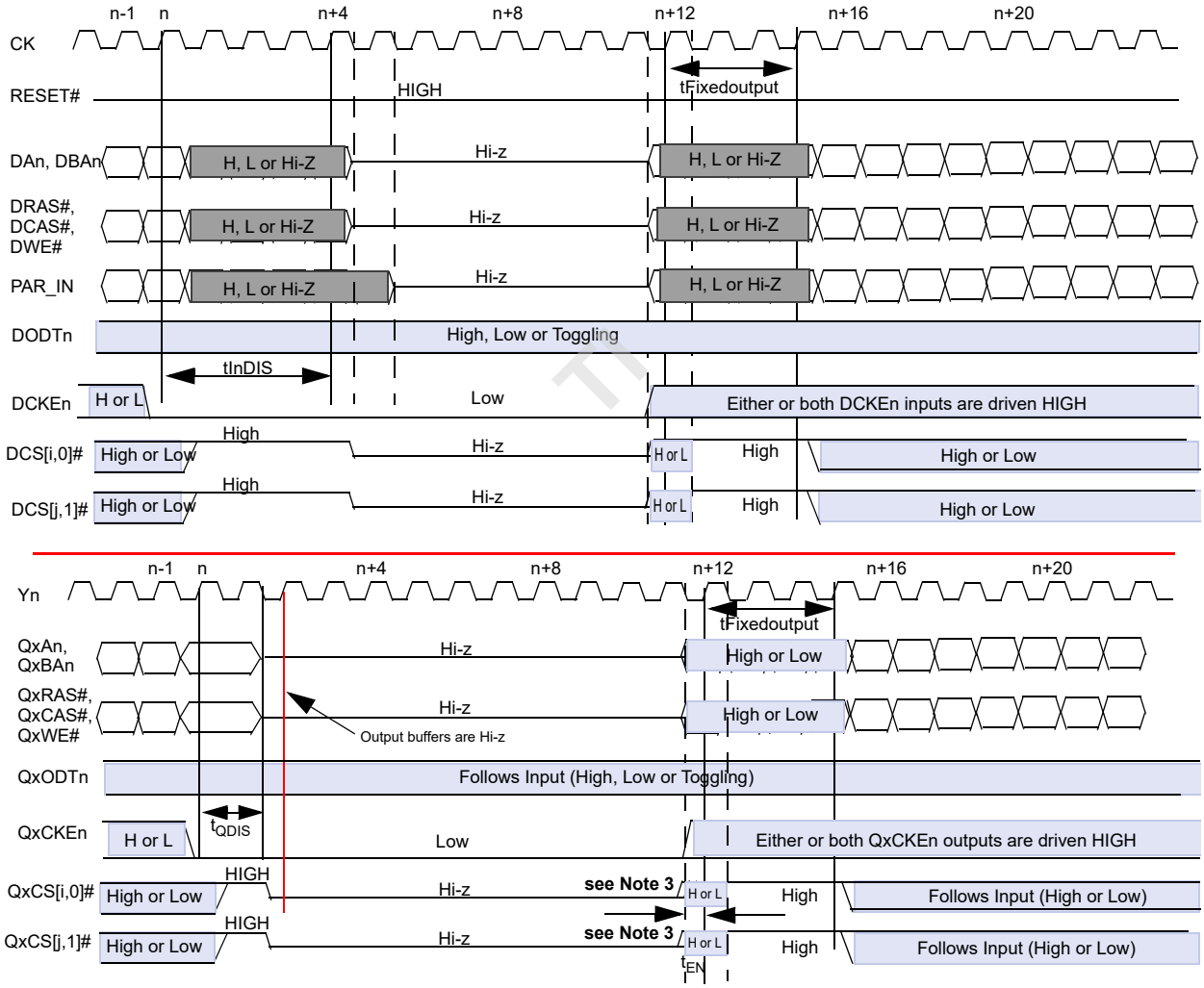



**Figure 10 — Power Down Mode Entry and Exit with IBT On**

NOTE 1 i, j only apply for QuadCS capable register. When QuadCS is enabled, i = 2, j = 3

NOTE 2 QuadCS disabled: During CKE Power Down Entry/Exit, driving DCS[1:0]# LOW is illegal as it will force SSTE32882 into Register Control Word access mode.

NOTE 3 Upon CKE Power Down exit, QxCSn# may follow DCSn# inputs for maximum of 1 tCK, or be held HIGH for tFIXEDOUTPUT regardless of what DCSn# input level is. For all other operation QxCSn# outputs will follow DCSn# inputs.

#### 2.1.4.2 Register CKE Power Down with IBT On (cont'd)

To re-enable the SSTE32882 from this Power Down Mode with IBT on, valid logic levels are required at all device inputs when either or both DCKEn inputs are driven HIGH. Upon either DCKE0 or DCKE1 input going HIGH, the SSTE32882 immediately starts driving HIGH on the appropriate QxCKEn signals. The QxCSn# signals are driven HIGH and the QxODTn signals follow the inputs. Other output signals QxRAS#, QxCAS#, QxWE# and QxAddr are driven either HIGH or LOW to ensure stable valid logic on all device outputs when QxCKEn goes HIGH. The device drives output signals to these levels for $t_{Fixedoutput}$ to allow input receivers to be stabilized. After the input receivers are stabilized, the register output follow their corresponding input levels. When exiting CKE power down mode, either one of the Chip select register inputs DCSn# can be asserted for 1 tCK. For QuadCS capable register, when working in quad rank mode, either two of the Chip select register inputs DCSn# can be asserted for 1 tCK. The device guarantees that input receivers are stabilized within $t_{Fixedoutput}$ clocks after DCKEn input is driven HIGH. This is shown in Figure 10**.**

### 2.1.5 Clock Stopped Power Down Mode

To support S3 Power Management mode or any other operation that allows Yn clocks to float, the SSTE32882 supports a Clock Stopped power down mode. When both inputs CK and CK# are being held LOW ($V_{IL\ (static)}$) or float (will eventually settle at LOW because of the (10K-100K Ohm) pulldown resistor in the CK/CK# input buffer), the device stops operation and enters low-power static and standby operation. The corresponding timing requirement are shown in Figure 11, "Clock Stopped Power Down Entry and Exit with IBT On" and Figure 12, "Clock Stopped Power Down Entry and Exit with IBT Off". The register device will stop its PLL and floats all outputs except QACKE0, QACKE1, QBCKE0 and QBCKE1, which must be kept driven LOW. The Clock Stopped power down mode can only be utilized once the DRAM received a self refresh command. In this state, the DRAM ignores all inputs except CKE. Hence, all register outputs besides QxCKE0 and QxCKE1 can be disabled.

#### 2.1.5.1 Clock Stopped Power Down Mode Entry

To enter Clock Stopped Power Down mode, the register will first enter CKE power down mode. Once in CKE power down mode, DCKEn will continue be deasserted for a minimum of one tCKoff before pulling CK and CK# LOW. After holding CK and CK# LOW ($V_{IL\ (static)}$) for at least one tCKEV, both CK and CK# can be floated (because of the (10K-100K Ohm) pulldown resistor in the CK/CK# input buffer, CK/CK# will stay at LOW even though they are not being driven). The register is now in Clock Stopped Power Down mode. After CK and CK# are pulled LOW, DCKEn will remain LOW for at least one tCKEV before it can floated (if needed to be float). At this point, all input receivers and input termination of the SSTE32882 are disabled. The only active input circuits are CK and CK#, which are required to detect the wake up request from the host.

#### 2.1.5.2 Clock Stopped Power Down Mode Exit

To wake up the register after entering Clock Stopped Power Down, the register inputs DCS[n:0]# must be driven to HIGH (to prevent accidental access to the control registers), and DCKEn to LOW. After that, a frequency and phase accurate input clock signal must be applied. Within tACT after CK and CK# resumed normal operation, the SSTE32882 outputs start becoming a function of their corresponding inputs. The state of the DCS[n:0]# inputs must not be changed before the end of tSTAB. The input clock CK and CK# must be stable for a time equal or greater than tSTAB before any access to the SSTE32882 can take place.

### 2.1.5 Clock Stopped Power Down Mode (cont'd)

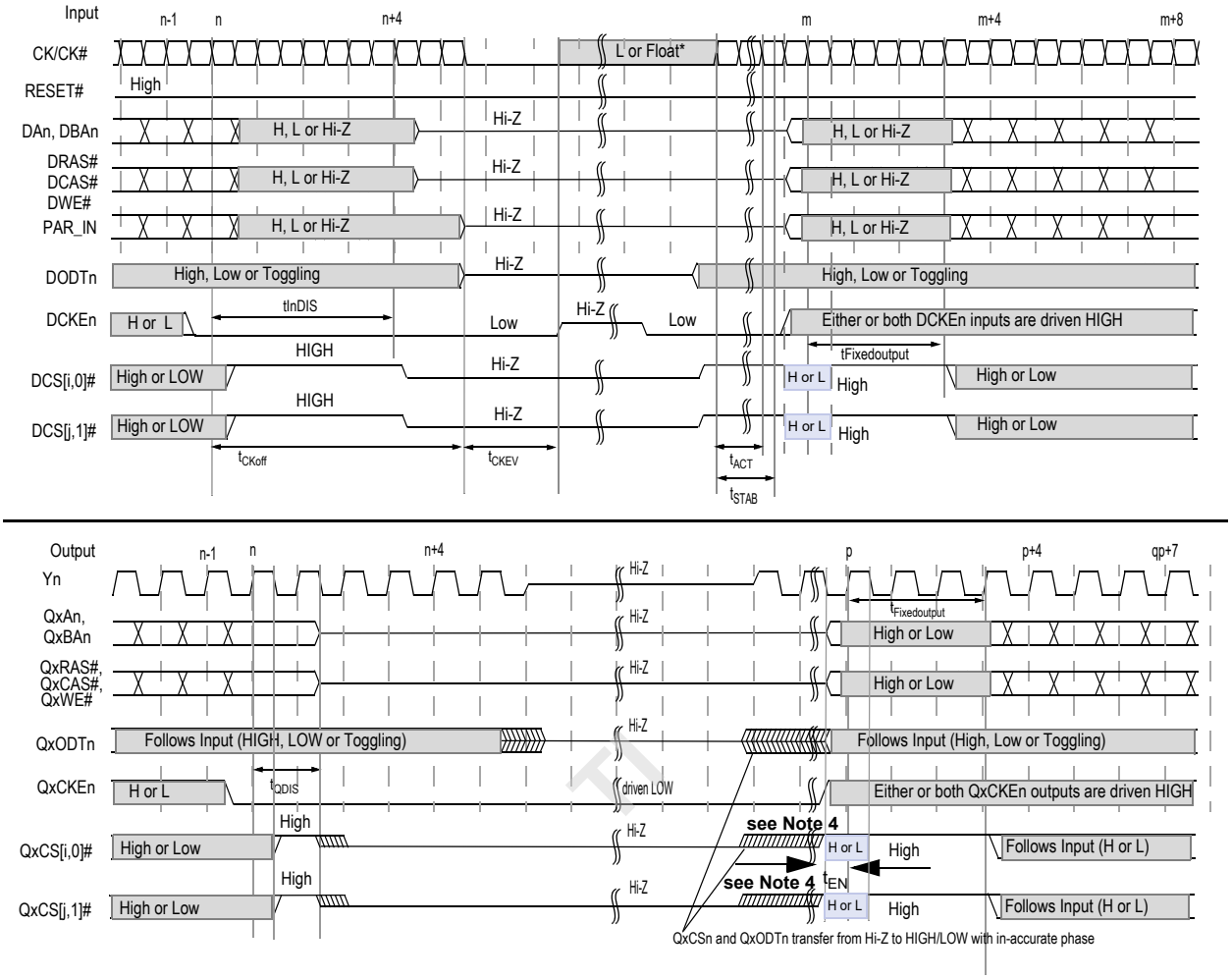



**Figure 11 — Clock Stopped Power Down Entry and Exit with IBT On**

NOTE 1 i, j only apply for QuadCS capable register. When QuadCS is enabled, i = 2, j = 3
NOTE 2 With RC9 DBA0='0'
NOTE 3 When CK/CK# inputs are floated, CK/CK# inputs are pulled LOW by the (10K-100K Ohm) pulldown resistor in the CK/CK# input buffer.
NOTE 4 Upon CKE Power Down exit, QxCSn# may follow DCSn# inputs for maximum of 1 tCK, or be held HIGH for tFIXEDOUTPUT regardless of what DCSn# input level is. For all other operation QxCSn# outputs will follow DCSn# inputs.

### 2.1.5 Clock Stopped Power Down Mode (cont'd)

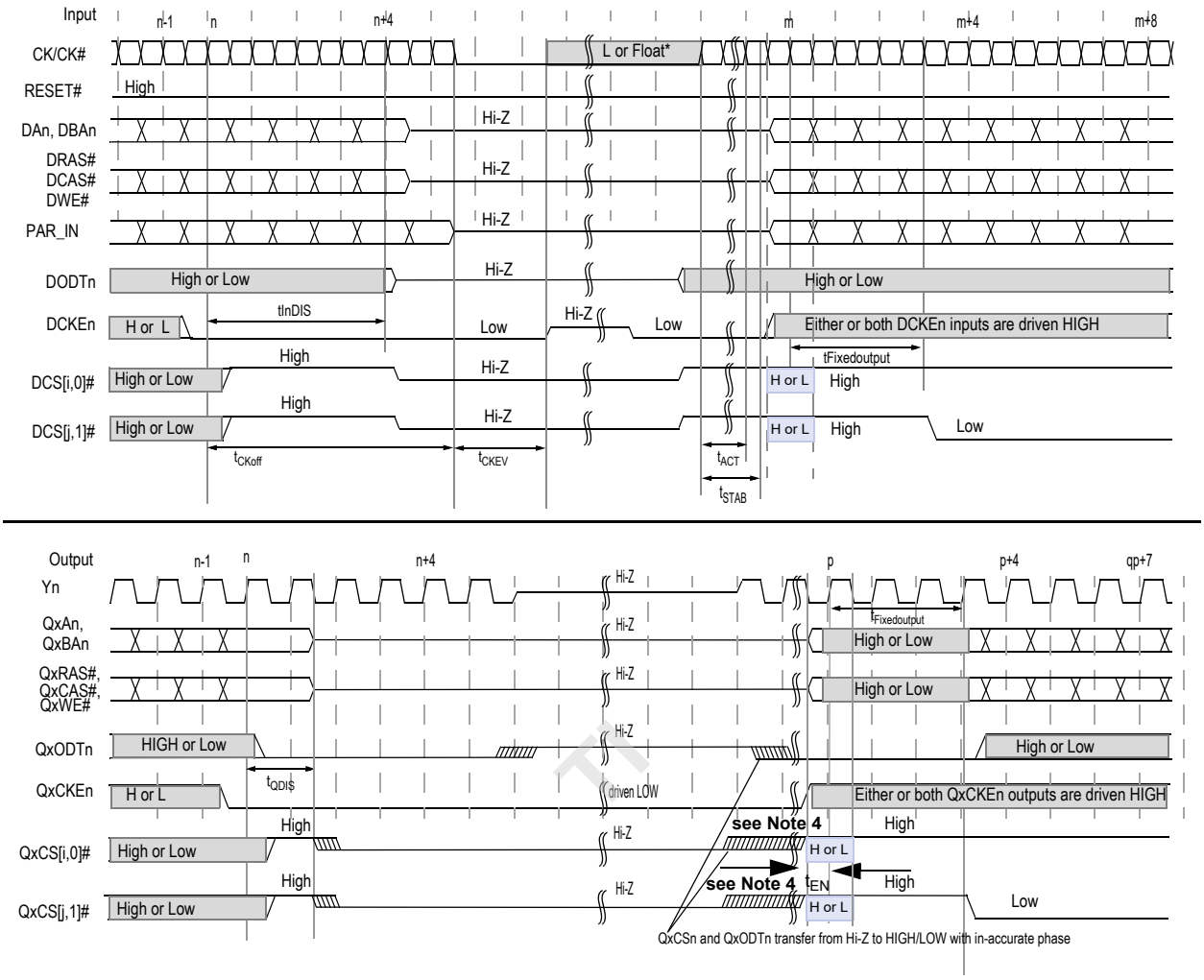



**Figure 12 — Clock Stopped Power Down Entry and Exit with IBT Off**

NOTE1 i, j only apply for QuadCS capable register. When QuadCS is enabled, i = 2, j = 3
NOTE 2 With RC9 DBA0='1'
NOTE 3 When CK/CK# inputs are floated, CK/CK# inputs are pulled LOW by the (10K-100K Ohm) pulldown resistor in the CK/CK# input buffer.
NOTE 4 Upon CKE Power Down exit, QxCSn# may follow DCSn# inputs for maximum of 1 tCK, or be held HIGH for tFIXEDOUTPUT regardless of what DCSn# input level is. For all other operation QxCSn# outputs will follow DCSn# inputs.

### 2.1.6 Dynamic 1T/3T Timing Transaction and Output Inversion Enabling/Disabling

Output Inversion is always enabled by default, after RESET# is de-asserted, to conserve power and reduce simultaneous output switching current. All A-outputs will follow the equivalent inputs, however the following B-outputs will be driven to the complement of the matching A-outputs: QBA3 - QBA9, QBA11, QBA13 - QBA15, QBBA0 - QBBA2.

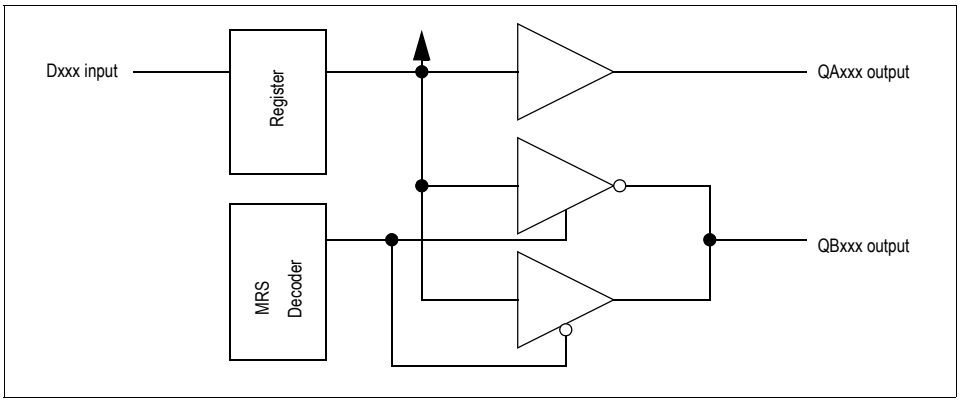



**Figure 13 — Output Inversion Functional Diagram**

The Output Inversion feature is not used during DRAM MRS command access. When Output Inversion is disabled, all corresponding A and B output drivers of the SSTE32882 are driven to the same logic levels. Output Inversion must be disabled when the MRS and EMRS commands must be issued to the DRAMs, for example, to assure that the same programming is issued to all DRAMs in a rank.

With Output Inversion disabled during MRS access, in order to allow correct DRAM accesses with the consequently increased simultaneous switching propagation delay the devices supports 3T timing. If this feature is invoked the device drives the received data on its outputs for thee cycles instead of one. The only exception are the QxCS[n:0]# outputs, which are the QACS0#, QACS1#, QBCS0# and QBCS1# outputs in the QuadCS disabled mode and are QCS[3:0]# in the QuadCS enabled mode.

When the device decodes the MRS command (DRAS#=0, DCAS#=0, DWE=0 and only one DCSn#=0), it will disable the Output Inversion function and pass the DRAM MRS command with an additional (one) clock delay on the appropriate QnCSx# signal to the DRAM. Back-to-back MRS command via the SSTE32882 must have a minimum of three clock delays. The SSTE32882 will automatically enable Output Inversion if there is no DRAM MRS command three clocks after the previous MRS command.

The inputs and outputs relationships for 1T timing and 3T timing are shown in Figure 14, Figure 15 and Figure 16**.**

### 2.1.6 Dynamic 1T/3T Timing Transaction and Output Inversion Enabling/Disabling (cont'd)

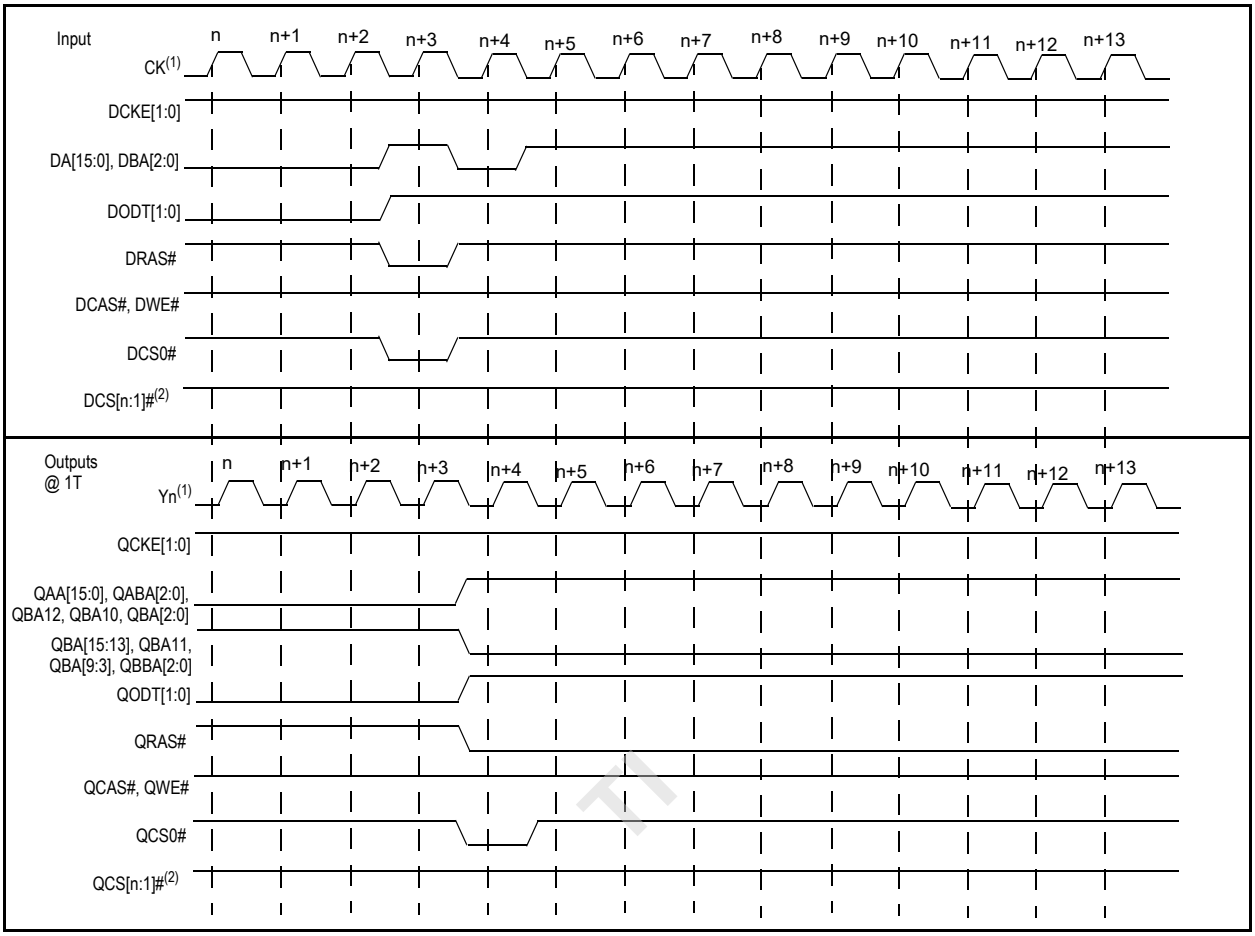



**Figure 14 — 1T Timing During Normal Operation**

NOTE 1 CK# and Yn# left out for better visibility
NOTE 2 n=1 for QuadCS disabled, n=3 for QuadCS enabled

### 2.1.6 Dynamic 1T/3T Timing Transaction and Output Inversion Enabling/Disabling (cont'd)

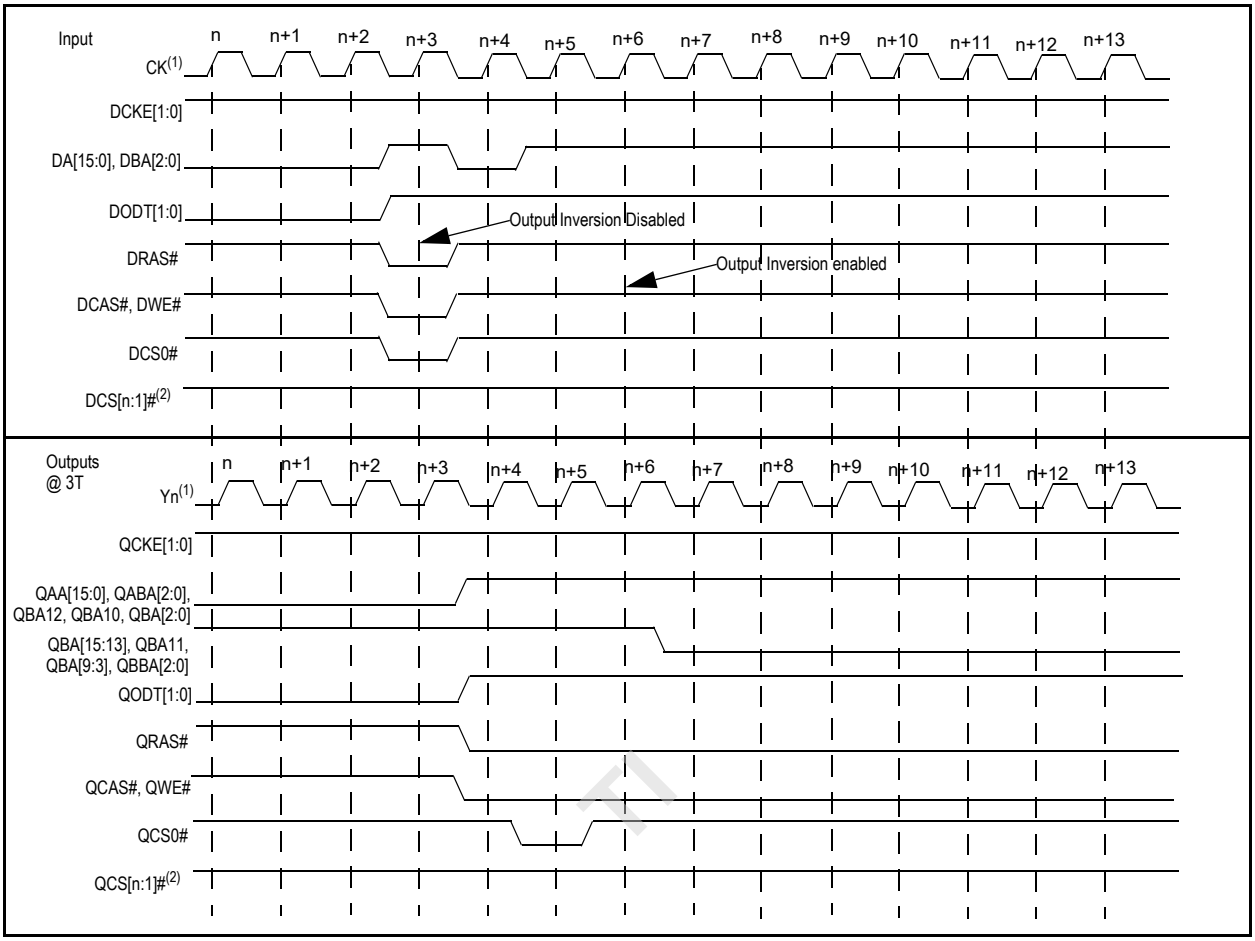



**Figure 15 — 3T Timing During DRAM MRS Command**

NOTE 1 CK# and Yn# left out for better visibility
NOTE 2 n=1 for QuadCS disabled, n=3 for QuadCS enabled

### 2.1.6 Dynamic 1T/3T Timing Transaction and Output Inversion Enabling/Disabling (cont'd)

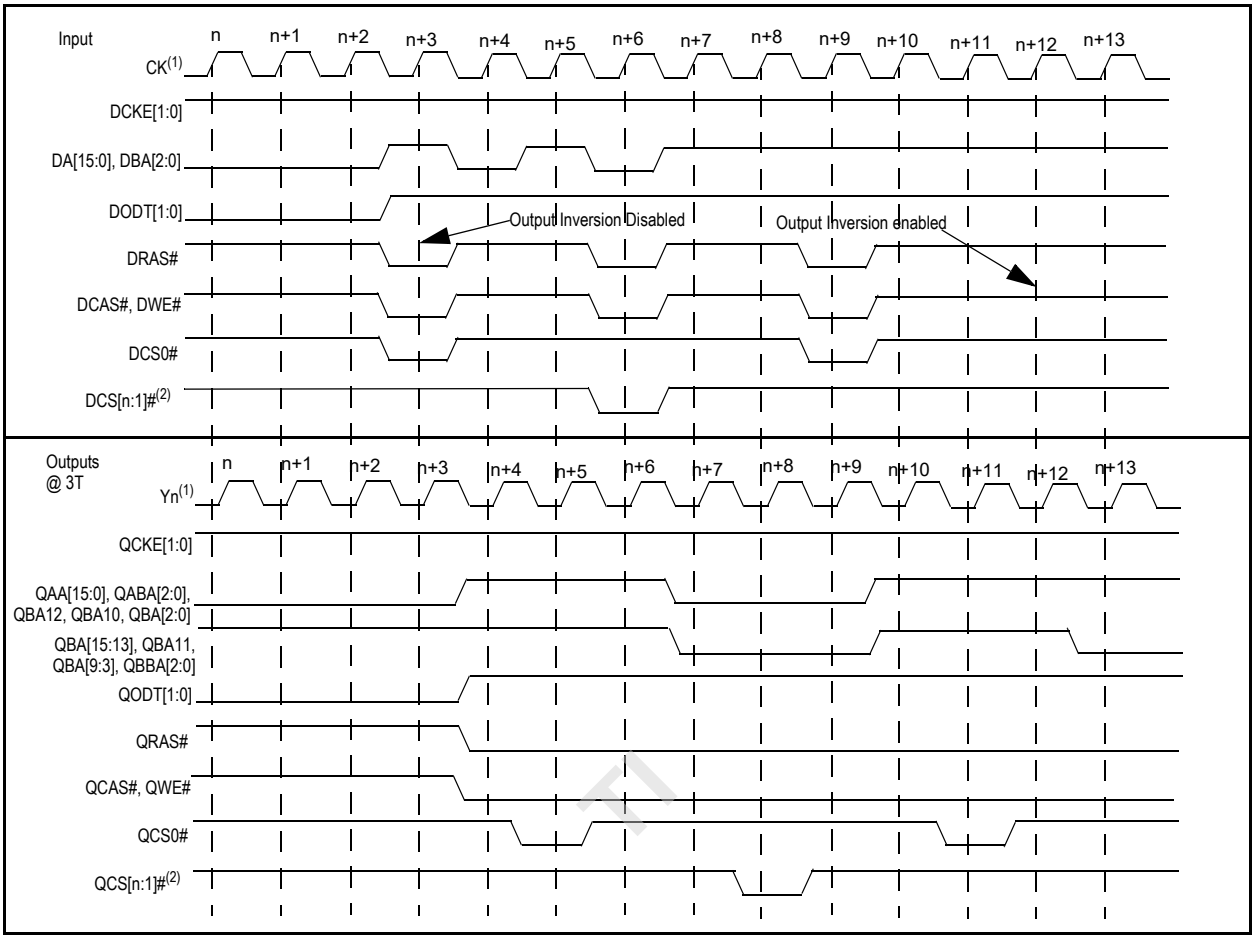



**Figure 16 — 3T Timing During Multiple DRAM MRS Commands**

NOTE 1 CK# and Yn# left out for better visibility
NOTE 2 n=1 for QuadCS disabled, n=3 for QuadCS enabled

## 2.2 Control Words

The SSTE32882 registers have internal control bits for adapting the configuration of certain device features. The control bits are accessed by the simultaneous assertion of both DCS0# and DCS1# in the QuadCS disabled mode. In the QuadCS enable mode, the simultaneous assertion of both DCS2# and DCS3# during normal operation, and the assertion of all four DCS[3:0]# inputs also result in control word access. However, assertion of any three DCS[3:0]# inputs is not legal. Register Qn outputs including QxCKE0, QxCKE1, QxODT0 and QxODT1 remain in their previous state. Select signals QxCS[n:0]# are set to HIGH during control word access.

The SSTE32882 allocates decoding for up to 16 words of control bits, RC0 through RC15. Selection of each word of control bits is presented on inputs DA0 through DA2 and DBA2. Data to be written into the configuration registers need to be presented on DA3, DA4, DBA0 and DBA1. Bits DA[15:5] must be LOW and at least one DCKEn input must be HIGH for a valid access. During control word write, at least one DCKEn must be asserted. If register CKE power down feature is disabled, DCKEn input is a don't care (either HIGH or LOW). **T**he inputs on DRAS#, DCAS#, DWE# and DODT[1:0] can be either HIGH or LOW and are ignored by the register during control word access. In all cases Address and command parity is checked during control word write operations. ERROUT# is asserted and the command is ignored if a parity error is detected. Using this mechanism, controllers may use the SSTE32882 to validate the address and command bus signal integrity to the module as long as one or more of the parity checked input signals DA3...DA15, DBA0, DBA1, DRAS#, DCAS#, and DWE# are kept HIGH.

Control word access must be possible at any defined frequency independent of the current setting of RC2[DBA1] control registers.

## 2.3 Pinout Configuration

Package options include 176-ball Thin-Profile Fine-Pitch BGA (TFBGA) with 0.65 mm ball pitch, 11 x 20 grid, 8.0 mm x 13.5 mm. It is using the mechanical outline MO-246 variation F. The device pinout supports outputs on the outer two left and right columns to support easy DIMM signal routing. Corresponding inputs are placed in a way that two devices can be placed back to back for 4 Rank modules while the data inputs share the same vias. Each input and output is located close to an associated no ball position or on the outer two rows to allow low cost via technology combined with the small 0.65 mm ball pitch.

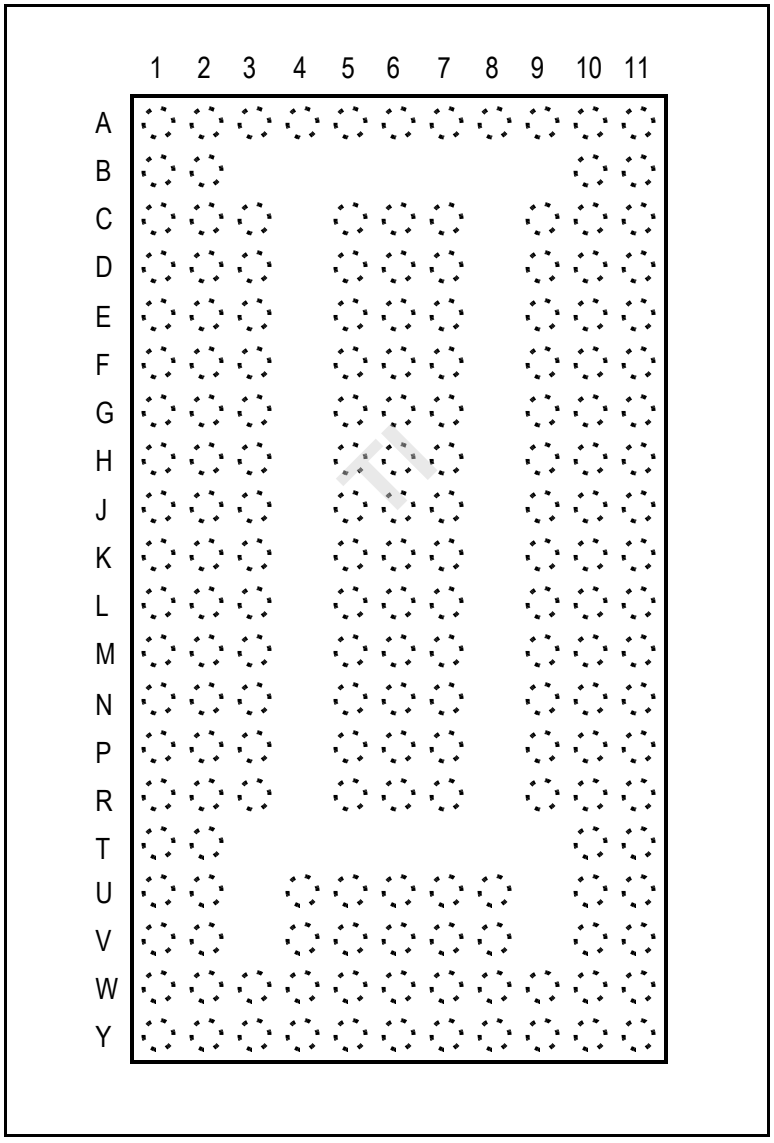



**Figure 17 — Pinout Configuration**

### 2.3.1 Pinout Top View for 176-ball TFBGA (Front Configuration, QuadCS Mode Disabled)

176-ball, 11 × 20 grid, TOP VIEW

Table 3 specifies the pinout for SSTE32882 in front configuration with QuadCS mode disabled. The device has symmetric pinout with inputs at the south side and outputs to east and west sides. This allows back to back mounting on both sides of the PCB if more than one device is needed.

**Table 3 — Ball Assignment; MIRROR=LOW, QCSEN#=HIGH (or Float)**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | QAA13 | QAA8 | QCSEN# | VSS | RESET# | MIRROR | ERROUT# | VSS | RSVD | QBA8 | QBA13 |
| **B** | QAA14 | QAA7 | | | | | | | | QBA7 | QBA14 |
| **C** | QAA9 | QAA6 | VDD | | VDD | VDD | VDD | | VDD | QBA6 | QBA9 |
| **D** | QAA11 | QAA5 | VSS | | VSS | VSS | VSS | | VSS | QBA5 | QBA11 |
| **E** | QAA2 | QAA4 | VDD | | VDD | VDD | VDD | | VDD | QBA4 | QBA2 |
| **F** | QAA1 | QAA3 | VSS | | VSS | VSS | VSS | | VSS | QBA3 | QBA1 |
| **G** | QAA0 | QABA1 | VDD | | VDD | VDD | VDD | | VDD | QBBA1 | QBA0 |
| **H** | QAA12 | QABA0 | VSS | | VSS | VSS | VSS | | VSS | QBBA0 | QBA12 |
| **J** | QABA2 | QACS1# | VDD | | VDD | VDD | VDD | | VDD | QBCS1# | QBBA2 |
| **K** | QAA15 | QACKE0 | VSS | | VSS | VSS | VSS | | VSS | QBCKE0 | QBA15 |
| **L** | QAWE# | QACS0# | VDD | | VDD | VDD | VDD | | VDD | QBCS0# | QBWE# |
| **M** | QAA10 | QACKE1 | VSS | | VSS | VSS | VSS | | VSS | QBCKE1 | QBA10 |
| **N** | QACAS# | QAODT0 | VDD | | VDD | VDD | VDD | | VDD | QBODT0 | QBCAS# |
| **P** | QARAS# | QAODT1 | DA3 | | VSS | VSS | VSS | | DA4 | QBODT1 | QBRAS# |
| **R** | DCKE1 | DA14 | DA15 | | DA5 | RSVD | DA2 | | DA1 | DA10 | DODT1 |
| **T** | DCKE0 | DCS0# | | | | | | | | DCS1# | DODT0 |
| **U** | DA12 | DBA2 | | Y1# | PVSS | VDD | PVDD | Y0# | | DA13 | DCAS# |
| **V** | DA9 | DA11 | | Y1 | PVSS | VSS | PVDD | Y0 | | DRAS# | DWE# |
| **W** | DA8 | DA6 | FBIN# | Y3# | AVSS | CK# | RSVD | Y2# | FBOUT# | DA0 | DBA0 |
| **Y** | DA7 | RSVD | FBIN | Y3 | AVDD | CK | VREFCA | Y2 | FBOUT | PAR_IN | DBA1 |

NOTE 1 Pins A9 and W7 are reserved for future functions -- must not be connected on system
NOTE 2 Pins Y2 and R6 are reserved for DCS2# and DCS3# in the QuadCS mode and must not be connected on system, the device design needs to tolerate this floating pin
NOTE 3 Blank space indicates no ball is populated at that gridpoint -- vias on the module may be located in these areas

### 2.3.2 Pinout Top View for 176-ball TFBGA (Back Configuration, QuadCS Mode Disabled)

Table 4 specifies the pinout for SSTE32882 in back configuration with QuadCS mode disabled.

**Table 4 — Ball Assignment; MIRROR=HIGH, QCSEN#=HIGH (or Float)**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | QAA13 | QAA8 | QCSEN# | VSS | RESET# | MIRROR | ERROUT# | VSS | RSVD | QBA8 | QBA13 |
| **B** | QAA14 | QAA7 | | | | | | | | QBA7 | QBA14 |
| **C** | QAA9 | QAA6 | VDD | | VDD | VDD | VDD | | VDD | QBA6 | QBA9 |
| **D** | QAA11 | QAA5 | VSS | | VSS | VSS | VSS | | VSS | QBA5 | QBA11 |
| **E** | QAA2 | QAA4 | VDD | | VDD | VDD | VDD | | VDD | QBA4 | QBA2 |
| **F** | QAA1 | QAA3 | VSS | | VSS | VSS | VSS | | VSS | QBA3 | QBA1 |
| **G** | QAA0 | QABA1 | VDD | | VDD | VDD | VDD | | VDD | QBBA1 | QBA0 |
| **H** | QAA12 | QABA0 | VSS | | VSS | VSS | VSS | | VSS | QBBA0 | QBA12 |
| **J** | QABA2 | QACS1# | VDD | | VDD | VDD | VDD | | VDD | QBCS1# | QBBA2 |
| **K** | QAA15 | QACKE0 | VSS | | VSS | VSS | VSS | | VSS | QBCKE0 | QBA15 |
| **L** | QAWE# | QACS0# | VDD | | VDD | VDD | VDD | | VDD | QBCS0# | QBWE# |
| **M** | QAA10 | QACKE1 | VSS | | VSS | VSS | VSS | | VSS | QBCKE1 | QBA10 |
| **N** | QACAS# | QAODT0 | VDD | | VDD | VDD | VDD | | VDD | QBODT0 | QBCAS# |
| **P** | QARAS# | QAODT1 | DA4 | | VSS | VSS | VSS | | DA3 | QBODT1 | QBRAS# |
| **R** | DODT1 | DA10 | DA1 | | DA2 | RSVD | DA5 | | DA15 | DA14 | DCKE1 |
| **T** | DODT0 | DCS1# | | | | | | | | DCS0# | DCKE0 |
| **U** | DCAS# | DA13 | | Y1# | PVSS | VDD | PVDD | Y0# | | DBA2 | DA12 |
| **V** | DWE# | DRAS# | | Y1 | PVSS | VSS | PVDD | Y0 | | DA11 | DA9 |
| **W** | DBA0 | DA0 | FBIN# | Y3# | AVSS | CK# | RSVD | Y2# | FBOUT# | DA6 | DA8 |
| **Y** | DBA1 | PAR_IN | FBIN | Y3 | AVDD | CK | VREFCA | Y2 | FBOUT | RSVD | DA7 |

NOTE 1 Pins A9 and W7 are reserved for future functions -- must not be connected on system
NOTE 2 Pin Y10 and R6 are reserved for DCS2# and DCS3# in the QuadCS mode and must not be connected on system, the device design needs to tolerate this floating pin
NOTE 3 Blank space indicate no ball is populated at that gridpoint -- vias on the module may be located in these areas

### 2.3.3 Pinout Top View for 176-ball TFBGA (fRont Configuration, QuadCS Mode Enabled)

Table 5 specifies the pinout for SSTE32882 in front configuration with QuadCS mode enabled.

**Table 5 — Ball Assignment; MIRROR=LOW, QCSEN#=LOW**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | QAA13 | QAA8 | QCSEN# | VSS | RESET# | MIRROR | ERROUT# | VSS | RSVD | QBA8 | QBA13 |
| **B** | QAA14 | QAA7 | | | | | | | | QBA7 | QBA14 |
| **C** | QAA9 | QAA6 | VDD | | VDD | VDD | VDD | | VDD | QBA6 | QBA9 |
| **D** | QAA11 | QAA5 | VSS | | VSS | VSS | VSS | | VSS | QBA5 | QBA11 |
| **E** | QAA2 | QAA4 | VDD | | VDD | VDD | VDD | | VDD | QBA4 | QBA2 |
| **F** | QAA1 | QAA3 | VSS | | VSS | VSS | VSS | | VSS | QBA3 | QBA1 |
| **G** | QAA0 | QABA1 | VDD | | VDD | VDD | VDD | | VDD | QBBA1 | QBA0 |
| **H** | QAA12 | QABA0 | VSS | | VSS | VSS | VSS | | VSS | QBBA0 | QBA12 |
| **J** | QABA2 | QCS1# | VDD | | VDD | VDD | VDD | | VDD | QCS3# | QBBA2 |
| **K** | QAA15 | QACKE0 | VSS | | VSS | VSS | VSS | | VSS | QBCKE0 | QBA15 |
| **L** | QAWE# | QCS0# | VDD | | VDD | VDD | VDD | | VDD | QCS2# | QBWE# |
| **M** | QAA10 | QACKE1 | VSS | | VSS | VSS | VSS | | VSS | QBCKE1 | QBA10 |
| **N** | QACAS# | QAODT0 | VDD | | VDD | VDD | VDD | | VDD | QBODT0 | QBCAS# |
| **P** | QARAS# | QAODT1 | DA3 | | VSS | VSS | VSS | | DA4 | QBODT1 | QBRAS# |
| **R** | DCKE1 | DA14 | DA15 | | DA5 | DCS3# | DA2 | | DA1 | DA10 | DODT1 |
| **T** | DCKE0 | DCS0# | | | | | | | | DCS1# | DODT0 |
| **U** | DA12 | DBA2 | | Y1# | PVSS | VDD | PVDD | Y0# | | DA13 | DCAS# |
| **V** | DA9 | DA11 | | Y1 | PVSS | VSS | PVDD | Y0 | | DRAS# | DWE# |
| **W** | DA8 | DA6 | FBIN# | Y3# | AVSS | CK# | RSVD | Y2# | FBOUT# | DA0 | DBA0 |
| **Y** | DA7 | DCS2# | FBIN | Y3 | AVDD | CK | VREFCA | Y2 | FBOUT | PAR_IN | DBA1 |

NOTE 1 Pins A9 and W7 are reserved for future functions -- must not be connected on system
NOTE 2 Blank space indicate no ball is populated at that gridpoint -- vias on the module may be located in these areas

### 2.3.4 Pinout Top View for 176-ball TFBGA (Back Configuration, QuadCS Mode Enabled)

Table 6 specifies the pinout for SSTE32882 in back configuration with QuadCS mode enabled.

**Table 6 — Ball Assignment; MIRROR=HIGH, QCSEN#=LOW**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | QAA13 | QAA8 | QCSEN# | VSS | RESET# | MIRROR | ERROUT# | VSS | RSVD | QBA8 | QBA13 |
| **B** | QAA14 | QAA7 | | | | | | | | QBA7 | QBA14 |
| **C** | QAA9 | QAA6 | VDD | | VDD | VDD | VDD | | VDD | QBA6 | QBA9 |
| **D** | QAA11 | QAA5 | VSS | | VSS | VSS | VSS | | VSS | QBA5 | QBA11 |
| **E** | QAA2 | QAA4 | VDD | | VDD | VDD | VDD | | VDD | QBA4 | QBA2 |
| **F** | QAA1 | QAA3 | VSS | | VSS | VSS | VSS | | VSS | QBA3 | QBA1 |
| **G** | QAA0 | QABA1 | VDD | | VDD | VDD | VDD | | VDD | QBBA1 | QBA0 |
| **H** | QAA12 | QABA0 | VSS | | VSS | VSS | VSS | | VSS | QBBA0 | QBA12 |
| **J** | QABA2 | QCS1# | VDD | | VDD | VDD | VDD | | VDD | QCS3# | QBBA2 |
| **K** | QAA15 | QACKE0 | VSS | | VSS | VSS | VSS | | VSS | QBCKE0 | QBA15 |
| **L** | QAWE# | QCS0# | VDD | | VDD | VDD | VDD | | VDD | QCS2# | QBWE# |
| **M** | QAA10 | QACKE1 | VSS | | VSS | VSS | VSS | | VSS | QBCKE1 | QBA10 |
| **N** | QACAS# | QAODT0 | VDD | | VDD | VDD | VDD | | VDD | QBODT0 | QBCAS# |
| **P** | QARAS# | QAODT1 | DA4 | | VSS | VSS | VSS | | DA3 | QBODT1 | QBRAS# |
| **R** | DODT1 | DA10 | DA1 | | DA2 | DCS3# | DA5 | | DA15 | DA14 | DCKE1 |
| **T** | DODT0 | DCS1# | | | | | | | | DCS0# | DCKE0 |
| **U** | DCAS# | DA13 | | Y1# | PVSS | VDD | PVDD | Y0# | | DBA2 | DA12 |
| **V** | DWE# | DRAS# | | Y1 | PVSS | VSS | PVDD | Y0 | | DA11 | DA9 |
| **W** | DBA0 | DA0 | FBIN# | Y3# | AVSS | CK# | RSVD | Y2# | FBOUT# | DA6 | DA8 |
| **Y** | DBA1 | PAR_IN | FBIN | Y3 | AVDD | CK | VREFCA | Y2 | FBOUT | DCS2# | DA7 |

NOTE 1 Pins A9 and W7 are reserved for future functions -- must not be connected on system
NOTE 2 Blank space indicates no ball is populated at that gridpoint -- vias on the module may be located in these areas

## 2.4 Pinout Configuration Narrow Package[1]

Optional the device is available as 176-ball Thin-Profile Fine-Pitch BGA (TFBGA) with 0.65 mm ball pitch, 8 x 22 grid, 6.0 mm x 15 mm. It is using the mechanical outline MO-246 variation B. Equivalent to the 11 x 20 grid configuration the device pinout supports outputs on the outer two left and right columns. Corresponding inputs are placed in a way that two devices can be placed back to back for 4 Rank modules while the data inputs share the same vias.

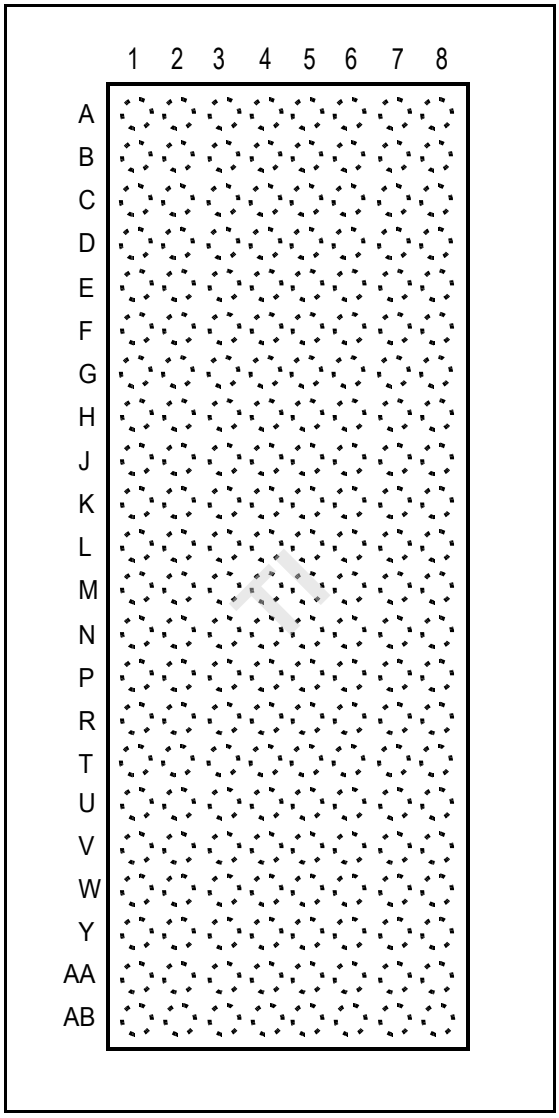



**Figure 18 — Pinout Configuration**

NOTE 1 This package may only be used in new DIMM designs. It is not intended for use in the existing DIMM's.

### 2.4.1 Pinout Top View for 176-ball TFBGA (Front Configuration, QuadCS Mode Disabled)

176-ball, 8 x 22 grid, TOP VIEW

Table 7 specifies the pinout for SSTE32882 in front configuration with QuadCS mode disabled. The device has symmetric pinout with inputs at the south side and outputs to east and west sides. This allows back to back mounting on both sides of the PCB if more than one device is needed.

**Table 7 — Ball Assignment; MIRROR=LOW, QCSEN#=HIGH (or Float)**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| **A** | QAA13 | QAA8 | QCSEN# | RESET# | ERROUT# | RSVD | QBA8 | QBA13 |
| **B** | QAA14 | QAA7 | VSS | VSS | MIRROR | VSS | QBA7 | QBA14 |
| **C** | QAA9 | QAA6 | VDD | VDD | VDD | VDD | QBA6 | QBA9 |
| **D** | QAA11 | QAA5 | VSS | VSS | VSS | VSS | QBA5 | QBA11 |
| **E** | QAA2 | QAA4 | VDD | VDD | VDD | VDD | QBA4 | QBA2 |
| **F** | QAA1 | QAA3 | VSS | VSS | VSS | VSS | QBA3 | QBA1 |
| **G** | QAA0 | QABA1 | VDD | VDD | VDD | VDD | QBBA1 | QBA0 |
| **H** | QAA12 | QABA0 | VSS | VSS | VSS | VSS | QBBA0 | QBA12 |
| **J** | QABA2 | QACS1# | VDD | VDD | VDD | VDD | QBCS1# | QBBA2 |
| **K** | QAA15 | QACKE0 | VSS | VSS | VSS | VSS | QBCKE0 | QBA15 |
| **L** | QAWE# | QACS0# | VDD | VDD | VDD | VDD | QBCS0# | QBWE# |
| **M** | QAA10 | QACKE1 | VSS | VSS | VSS | VSS | QBCKE1 | QBA10 |
| **N** | QACAS# | QAODT0 | VDD | VDD | VDD | VDD | QBODT0 | QBCAS# |
| **P** | QARAS# | QAODT1 | VSS | VSS | VSS | VSS | QBODT1 | QBRAS# |
| **R** | DA14 | DCKE1 | VDD | VDD | VDD | VDD | DODT1 | DA10 |
| **T** | DCS0# | DCKE0 | VSS | VSS | VSS | VSS | DODT0 | DCS1# |
| **U** | DA12 | DA3 | Y1# | PVSS | PVDD | Y0# | DA4 | DCAS# |
| **V** | DA5 | DA9 | Y1 | PVSS | PVDD | Y0 | DWE# | DA2 |
| **W** | DA8 | DA15 | Y3# | PVSS | PVDD | Y2# | DA1 | DBA0 |
| **Y** | DA7 | DBA2 | Y3 | AVSS | AVDD | Y2 | DA13 | DBA1 |
| **AA** | DA11 | RSVD | FBIN# | CK# | RSVD | FBOUT# | PAR_IN | DRAS# |
| **AB** | DA6 | RSVD | FBIN | CK | VREFCA | FBOUT | RSVD | DA0 |

NOTE Pins A6, AA2, AA5, AB2, and AB7 are reserved for future functions must not be connected on system. The system must provide a solder pad for these pins. The device design needs to tolerate floating on these pins. A3 may be left floating since it has an internal pull-up resistor.

### 2.4.2 Pinout Top View for 176-ball TFBGA (Back Configuration, QuadCS Mode Disabled)

Table 8 specifies the pinout for SSTE32882 in back configuration with QuadCS mode disabled.

**Table 8 — Ball Assignment; MIRROR=HIGH, QCSEN#=HIGH (or Float)**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| **A** | QAA13 | QAA8 | QCSEN# | RESET# | ERROUT# | RSVD | QBA8 | QBA13 |
| **B** | QAA14 | QAA7 | VSS | VSS | MIRROR | VSS | QBA7 | QBA14 |
| **C** | QAA9 | QAA6 | VDD | VDD | VDD | VDD | QBA6 | QBA9 |
| **D** | QAA11 | QAA5 | VSS | VSS | VSS | VSS | QBA5 | QBA11 |
| **E** | QAA2 | QAA4 | VDD | VDD | VDD | VDD | QBA4 | QBA2 |
| **F** | QAA1 | QAA3 | VSS | VSS | VSS | VSS | QBA3 | QBA1 |
| **G** | QAA0 | QABA1 | VDD | VDD | VDD | VDD | QBBA1 | QBA0 |
| **H** | QAA12 | QABA0 | VSS | VSS | VSS | VSS | QBBA0 | QBA12 |
| **J** | QABA2 | QACS1# | VDD | VDD | VDD | VDD | QBCS1# | QBBA2 |
| **K** | QAA15 | QACKE0 | VSS | VSS | VSS | VSS | QBCKE0 | QBA15 |
| **L** | QAWE# | QACS0# | VDD | VDD | VDD | VDD | QBCS0# | QBWE# |
| **M** | QAA10 | QACKE1 | VSS | VSS | VSS | VSS | QBCKE1 | QBA10 |
| **N** | QACAS# | QAODT0 | VDD | VDD | VDD | VDD | QBODT0 | QBCAS# |
| **P** | QARAS# | QAODT1 | VSS | VSS | VSS | VSS | QBODT1 | QBRAS# |
| **R** | DA10 | DODT1 | VDD | VDD | VDD | VDD | DCKE1 | DA14 |
| **T** | DCS1# | DODT0 | VSS | VSS | VSS | VSS | DCKE0 | DCS0# |
| **U** | DCAS# | DA4 | Y1# | PVSS | PVDD | Y0# | DA3 | DA12 |
| **V** | DA2 | DWE# | Y1 | PVSS | PVDD | Y0 | DA9 | DA5 |
| **W** | DBA0 | DA1 | Y3# | PVSS | PVDD | Y2# | DA15 | DA8 |
| **Y** | DBA1 | DA13 | Y3 | AVSS | AVDD | Y2 | DBA2 | DA7 |
| **AA** | DRAS# | PAR_IN | FBIN# | CK# | RSVD | FBOUT# | RSVD | DA11 |
| **AB** | DA0 | RSVD | FBIN | CK | VREFCA | FBOUT | RSVD | DA6 |

NOTE Pins A6, AA5, AA7, AB2, and AB7 are reserved for future functions must not be connected on system. The system must provide a solder pad for these pins. The device design needs to tolerate floating on these pins. A3 may be left floating since it has an internal pull-up resistor.

### 2.4.3 Pinout Top View for 176-ball TFBGA (Front Configuration, QuadCS Mode Enabled)

Table 9 specifies the pinout for SSTE32882 in front configuration with QuadCS mode enabled.

**Table 9 — Ball Assignment; MIRROR=LOW, QCSEN#=LOW**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| **A** | QAA13 | QAA8 | QCSEN# | RESET# | ERROUT# | RSVD | QBA8 | QBA13 |
| **B** | QAA14 | QAA7 | VSS | VSS | MIRROR | VSS | QBA7 | QBA14 |
| **C** | QAA9 | QAA6 | VDD | VDD | VDD | VDD | QBA6 | QBA9 |
| **D** | QAA11 | QAA5 | VSS | VSS | VSS | VSS | QBA5 | QBA11 |
| **E** | QAA2 | QAA4 | VDD | VDD | VDD | VDD | QBA4 | QBA2 |
| **F** | QAA1 | QAA3 | VSS | VSS | VSS | VSS | QBA3 | QBA1 |
| **G** | QAA0 | QABA1 | VDD | VDD | VDD | VDD | QBBA1 | QBA0 |
| **H** | QAA12 | QABA0 | VSS | VSS | VSS | VSS | QBBA0 | QBA12 |
| **J** | QABA2 | QCS1# | VDD | VDD | VDD | VDD | QCS3# | QBBA2 |
| **K** | QAA15 | QACKE0 | VSS | VSS | VSS | VSS | QBCKE0 | QBA15 |
| **L** | QAWE# | QCS0# | VDD | VDD | VDD | VDD | QCS2# | QBWE# |
| **M** | QAA10 | QACKE1 | VSS | VSS | VSS | VSS | QBCKE1 | QBA10 |
| **N** | QACAS# | QAODT0 | VDD | VDD | VDD | VDD | QBODT0 | QBCAS# |
| **P** | QARAS# | QAODT1 | VSS | VSS | VSS | VSS | QBODT1 | QBRAS# |
| **R** | DA14 | DCKE1 | VDD | VDD | VDD | VDD | DODT1 | DA10 |
| **T** | DCS0# | DCKE0 | VSS | VSS | VSS | VSS | DODT0 | DCS1# |
| **U** | DA12 | DA3 | Y1# | PVSS | PVDD | Y0# | DA4 | DCAS# |
| **V** | DA5 | DA9 | Y1 | PVSS | PVDD | Y0 | DWE# | DA2 |
| **W** | DA8 | DA15 | Y3# | PVSS | PVDD | Y2# | DA1 | DBA0 |
| **Y** | DA7 | DBA2 | Y3 | AVSS | AVDD | Y2 | DA13 | DBA1 |
| **AA** | DA11 | DCS2# | FBIN# | CK# | RSVD | FBOUT# | PAR_IN | DRAS# |
| **AB** | DA6 | RSVD | FBIN | CK | VREFCA | FBOUT | DCS3# | DA0 |

NOTE Pins A6, AA5, and AB2 are reserved for future functions must not be connected on system. The system must provide a solder pad for these pins. The device design needs to tolerate floating on these pins. A3 must be tied LOW for this configuration.

### 2.4.4 Pinout Top View for 176-ball TFBGA (Back Configuration, QuadCS Mode Enabled)

Table 10 specifies the pinout for SSTE32882 in back configuration with QuadCS mode enabled.

**Table 10 — Ball Assignment; MIRROR=HIGH, QCSEN#=LOW)**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| **A** | QAA13 | QAA8 | QCSEN# | RESET# | ERROUT# | RSVD | QBA8 | QBA13 |
| **B** | QAA14 | QAA7 | VSS | VSS | MIRROR | VSS | QBA7 | QBA14 |
| **C** | QAA9 | QAA6 | VDD | VDD | VDD | VDD | QBA6 | QBA9 |
| **D** | QAA11 | QAA5 | VSS | VSS | VSS | VSS | QBA5 | QBA11 |
| **E** | QAA2 | QAA4 | VDD | VDD | VDD | VDD | QBA4 | QBA2 |
| **F** | QAA1 | QAA3 | VSS | VSS | VSS | VSS | QBA3 | QBA1 |
| **G** | QAA0 | QABA1 | VDD | VDD | VDD | VDD | QBBA1 | QBA0 |
| **H** | QAA12 | QABA0 | VSS | VSS | VSS | VSS | QBBA0 | QBA12 |
| **J** | QABA2 | QCS1# | VDD | VDD | VDD | VDD | QCS3# | QBBA2 |
| **K** | QAA15 | QACKE0 | VSS | VSS | VSS | VSS | QBCKE0 | QBA15 |
| **L** | QAWE# | QCS0# | VDD | VDD | VDD | VDD | QCS2# | QBWE# |
| **M** | QAA10 | QACKE1 | VSS | VSS | VSS | VSS | QBCKE1 | QBA10 |
| **N** | QACAS# | QAODT0 | VDD | VDD | VDD | VDD | QBODT0 | QBCAS# |
| **P** | QARAS# | QAODT1 | VSS | VSS | VSS | VSS | QBODT1 | QBRAS# |
| **R** | DA10 | DODT1 | VDD | VDD | VDD | VDD | DCKE1 | DA14 |
| **T** | DCS1# | DODT0 | VSS | VSS | VSS | VSS | DCKE0 | DCS0# |
| **U** | DCAS# | DA4 | Y1# | PVSS | PVDD | Y0# | DA3 | DA12 |
| **V** | DA2 | DWE# | Y1 | PVSS | PVDD | Y0 | DA9 | DA5 |
| **W** | DBA0 | DA1 | Y3# | PVSS | PVDD | Y2# | DA15 | DA8 |
| **Y** | DBA1 | DA13 | Y3 | AVSS | AVDD | Y2 | DBA2 | DA7 |
| **AA** | DRAS# | PAR_IN | FBIN# | CK# | RSVD | FBOUT# | DCS2# | DA11 |
| **AB** | DA0 | RSVD | FBIN | CK | VREFCA | FBOUT | DCS3# | DA6 |

NOTE Pins A6, AA5, and AB2 are reserved for future functions must not be connected on system. The system must provide a solder pad for these pins. The device design needs to tolerate floating on these pins. A3 must be tied LOW for this configuration.

## 2.5 Terminal Functions

**Table 11 — Terminal Functions**

| Signal Group | Signal Name | Type | Description |
|---|---|---|---|
| Ungated inputs | DCKE0/1, DODT0/1 | 1.5 V, 1.35 V, or 1.25 V CMOS Inputs[1] | DRAM corresponding register function pins not associated with Chip Select. |
| Chip Select gated inputs | DA0..DA15, DBA0..DBA2, DRAS#, DCAS#, DWE# | 1.5 V, 1.35 V, or 1.25 V CMOS Inputs[1] | DRAM corresponding register inputs, re-driven only when either chip select is LOW. If both chip selects are LOW the register maintains the state of the previous input clock cycle at its outputs |
| Chip Select inputs | DCS0#, DCS1# | 1.5 V, 1.35 V, or 1.25 V CMOS Inputs[1] | DRAM corresponding register Chip Select signals. These pins initiate DRAM address/command decodes, and as such exactly one will be LOW when a valid address/command is present which should be re-driven. |
| | DCS2#, DCS3# | 1.5 V, 1.35 V, or 1.25 V CMOS Inputs[1] | DRAM corresponding register Chip Select signals when QuadCS mode is enabled. DCS2# and DCS3# inputs are disabled when QuadCS mode is disabled. |
| Re-driven outputs | QxA0..QxA15, QxBA0..QxBA2, QxCS0/1#, QxCKE0/1, QxODT0/1, QxRAS#, QxCAS#, QxWE# | 1.5 V, 1.35 V, or 1.25 V CMOS Outputs[2] | Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. x is A or B; outputs are grouped as A or B and may be enabled or disabled via RC0. |
| Parity input | PAR_IN | 1.5 V, 1.35 V, or 1.25 V CMOS Input[1] | Input parity is received on pin PAR_IN and should maintain parity across the Chip Select Gated inputs (see above), at the rising edge of the input clock, one input clock cycle after corresponding data and one or both chip selects are LOW. |
| Parity error output | ERROUT# | Open drain | When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs. ERROUT# will be active for two clock cycles, and delayed by 3 clock cycles to the corresponding input data |
| Clock inputs | CK, CK# | 1.5 V, 1.35 V, or 1.25 V CMOS Inputs[1] | Differential main clock input pair to the PLL; has weak internal pull-down resistors (10 KΩ ~ 100 KΩ ). |
| Clock Outputs | Y0, Y0#.. Y3, Y3# | 1.5 V, 1.35 V, or 1.25 V CMOS Outputs | Re-driven Clock |
| Feedback inputs | FBIN, FBIN# | 1.5 V, 1.35 V, or 1.25 V CMOS Inputs[1] | Differential feedback inputs |
| Feedback outputs | FBOUT, FBOUT# | 1.5 V, 1.35 V, or 1.25 V CMOS Outputs | Differential feedback outputs |
| Miscellaneous inputs | RESET# | CMOS[3] | Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float. Once RESET# becomes HIGH the outputs get enabled and are driven LOW until the first access has been performed. RESET# also resets the ERROUT# signal. |
| | MIRROR | CMOS<Addt'l Footnote>c | Selects between two different ballouts for front or back operation. When the MIRROR input is HIGH, the device input bus termination (IBT) is turned off on all inputs, except the DCSn# and DODTn inputs. |
| | QCSEN# | CMOS[3] | Enables the QuadCS mode. The QCSEN# input has a weak internal pullup resistor (10 KΩ ~ 100 KΩ). |
| | VREFCA[1] | VDD/2 | Input reference voltage for the data inputs. |
| | VDD | Power Input | Power supply voltage |
| | VSS | Ground Input | Ground |
| | AVDD | Analog Power | Analog supply voltage |
| | AVSS | Analog Ground | Analog ground |
| | PVDD | Clock Driver Output Power | Clock logic and clock output driver power supply |
| | PVSS | Clock Driver Output Ground | Clock logic and clock output driver ground |
| | RSVD | I/O | Reserved pins, must be left floating |

NOTE 1 1.5 V, 1.35 V, or 1.25 V CMOS inputs uses VREFCA as the switching point reference for these receivers.
NOTE 2 These outputs are optimized for memory applications to drive DRAM inputs to 1.5 V, 1.35 V, or 1.25 V signaling levels
NOTE 3 Voltage levels according standard JESD8-11A, wide range, non terminated logic

## 2.6 Function Tables

**Table 12 — Function Table (Each Flip Flop) with QuadCS Mode Disabled**

| Inputs | | | | | | | | Outputs | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET# | DCS0# | DCS1# | CK[1] | CK#[1] | ADDR[2] | CMD[3] | CTRL[4] | Qn | QxCS0# | QxCS1# | QxODTn | QxCKEn |
| H | L | L | ↑ | ↓ | Control Word | Control Word | Control Word | No change | H | H | No change | No change |
| H | X | X | L or H | H or L | X | X | X | No change | No change | No change | No change | No change |
| H | L | H | ↑ | ↓ | X | X | X | Follows Input | L | H | Follows Input | Follows Input |
| H | X | X | L | L | X | X | X | Float | Float | Float | Float | L |
| H | H | L | ↑ | ↓ | X | X | X | Follows Input | H | L | Follows Input | Follows Input |
| H | H | H | ↑ | ↓ | X or Float | X or Float | X | No change or Float[5] | H | H | Follows Input | Follows Input |
| L | X or Float | X or Float | X or Float | X or Float | X or Float | X or Float | X or Float | Float | Float | Float | Float | L |

NOTE 1 It is illegal to hold both the CK and CK# inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when RESET# is driven HIGH.
NOTE 2 ADDR = DA[15:0], DBA[2:0]
NOTE 3 CMD = DRAS#, DCAS#, DWE#
NOTE 4 CTRL = DODTn, DCKEn
NOTE 5 Depending on Control Word RC0 Bit DA4. If RC0 DA4 is cleared, previous state is maintained. Address floating is disabled independent of control word RC0 once 3T timing is activated

**Table 13 — Function Table (Each Flip Flop) with QuadCS Mode Enabled**

| Inputs | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|
| RESET# | DCS[3:0]# | CK[1] | CK#[1] | A/C/E[2] | Qn | QCS[3:0]# | QxODTn | QxCKEn |
| H | LLHH | ↑ | ↓ | Control Word | No change | HHHH | No change | No change |
| H | HHLL | | | | | | | |
| H | LLLL | | | | | | | |
| H | XXXX | L or H | H or L | X | No change | No change | No change | No change |
| H | LHHH | ↑ | ↓ | Dn | Dn | LHHH | DODTn | DCKEn |
| H | HLHH | ↑ | ↓ | Dn | Dn | HLHH | DODTn | DCKEn |
| H | HHLH | ↑ | ↓ | Dn | Dn | HHLH | DODTn | DCKEn |
| H | HHHL | ↑ | ↓ | Dn | Dn | HHHL | DODTn | DCKEn |
| H | LHLH | ↑ | ↓ | Dn | Dn | LHLH | DODTn | DCKEn |
| H | HLLH | ↑ | ↓ | Dn | Dn | HLLH | DODTn | DCKEn |
| H | LHHL | ↑ | ↓ | Dn | Dn | LHHL | DODTn | DCKEn |
| H | HLHL | ↑ | ↓ | Dn | Dn | HLHL | DODTn | DCKEn |
| H | XXXX | L | L | X | float | float | float | L |
| H | HHHH | ↑ | ↓ | X | No change or float[3] | HHHH | DODTn | DCKEn |
| H | LLLH | ↑ | ↓ | X | Illegal Input States | | | |
| H | LLHL | | | | | | | |
| H | LHLL | | | | | | | |
| H | HLLL | | | | | | | |
| L | X or float | X or float | X or float | X or float | float | float | float | L |

NOTE 1 It is illegal to hold both the CK and CK# inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when RESET# is driven HIGH.
NOTE 2 A/C/E = DA0..DA15, DBA0..DBA2, DRAS#, DCAS#, DWE#, DODTn, DCKEn
NOTE 3 Depending on Control Word RC0 Bit DA4. If RC0 DA4 is cleared, previous state is maintained. Address floating is disabled independent of control word RC0 once 3T timing is activated

## 2.6 Function Tables (cont'd)

**Table 14 — Parity, LOW Power, and Standby Function Table with QuadCS Mode Disabled**

| Inputs | | | | | | | Output |
|---|---|---|---|---|---|---|---|
| **RESET#** | **DCS0#** | **DCS1#** | **CK**[1] | **CK#**[1] | **Σ of A/C**[2] | **PAR_IN**[3] | **ERROUT#**[4] |
| H | L | X | ↑ | ↓ | Even | L | H |
| H | L | X | ↑ | ↓ | Odd | L | L |
| H | L | X | ↑ | ↓ | Even | H | L |
| H | L | X | ↑ | ↓ | Odd | H | H |
| H | X | L | ↑ | ↓ | Even | L | H |
| H | X | L | ↑ | ↓ | Odd | L | L |
| H | X | L | ↑ | ↓ | Even | H | L |
| H | X | L | ↑ | ↓ | Odd | H | H |
| H | H | H | ↑ | ↓ | X | X | H[5] |
| H | X | X | L or H | H or L | X | X | ERROUT#$n_0$ |
| H | X | X | L | L | X | X | H[6] |
| L | X or floating | X or floating | X or floating | X or floating | X or floating | X or floating | H |

NOTE 1 It is illegal to hold both the CK and CK# inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when RESET# is driven HIGH.

NOTE 2 A/C = DA0...DA15, DBA0...DBA2, DRAS#, DCAS#, DWE#. Inputs DCKE0, DCKE1, DODT0, DODT1, DCS[1:0]# when QCSEN# = HIGH, DCS[3:0]# when QCSEN# = LOW are not included in this range. This column represents the sum of the number of A/C signals that are electrically HIGH.

NOTE 3 PAR_IN arrives one clock cycle after data to which it applies, ERROUT# is issued 3 clock cycles after the failing data.

NOTE 4 This transition assumes ERROUT# is HIGH at the crossing of CK going HIGH and CK# going **LOW**. If ERROUT# is **LOW**, it stays latched LOW for exactly two clock cycles or until RESET# is driven **LOW**.

NOTE 5 Same 3 cycle delay for ERROUT# is valid for the de-select phase (see diagram)

NOTE 6 The system is not allowed to pull CK and CK# LOW while ERROUT# is asserted.

## 2.6 Function Tables (cont'd)

**Table 15 — Parity, LOW Power, and Standby Function Table with QuadCS Mode Enabled**

| Inputs | | | | | | Output |
|---|---|---|---|---|---|---|
| **RESET#** | **DCS[3:0]#** | **CK**[1] | **CK#**[1] | **Σ of A/C**[2] | **PAR_IN**[3] | **ERROUT#**[4] |
| H | LXXX<br>XLXX<br>XXLX<br>XXXL | ↑ | ↓ | Even | L | H |
| H | LXXX<br>XLXX<br>XXLX<br>XXXL | ↑ | ↓ | Odd | L | L |
| H | LXXX<br>XLXX<br>XXLX<br>XXXL | ↑ | ↓ | Even | H | L |
| H | LXXX<br>XLXX<br>XXLX<br>XXXL | ↑ | ↓ | Odd | H | H |
| H | HHHH | ↑ | ↓ | X | X | H[5] |
| H | XXXX | L or H | H or L | X | X | ERROUT#$n_0$ |
| H | XXXX | L | L | X | X | H[6] |
| L | X or floating | X or floating | X or floating | X or floating | X or floating | H |

NOTE 1 It is illegal to hold both the CK and CK# inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when RESET# is driven HIGH.

NOTE 2 A/C = DA0...DA15, DBA0...DBA2, DRAS#, DCAS#, DWE#. Inputs DCKE0, DCKE1, DODT0, DODT1, DCS[1:0]# when QCSEN# = HIGH, DCS[3:0]# when QCSEN# = LOW are not included in this range. This column represents the sum of the number of A/C signals that are electrically HIGH.

NOTE 3 PAR_IN arrives one clock cycle after data to which it applies, ERROUT# is issued 3 clock cycles after the failing data.

NOTE 4 This transition assumes ERROUT# is HIGH at the crossing of CK going HIGH and CK# going LOW. If ERROUT# is LOW, it stays latched LOW for exactly two clock cycles or until RESET# is driven LOW.

NOTE 5 Same 3 cycle delay for ERROUT# is valid for the de-select phase (see diagram)

NOTE 6 The system is not allowed to pull CK and CK# LOW while ERROUT# is asserted.

## 2.6 Function Tables (cont'd)

**Table 16 — PLL Function Table**

| Inputs | | | | | Outputs | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **RESET#** | **AVDD** | **OEn** [1] | **CK** [2] | **CK#** [2] | **Yn** | **Yn#** | **FBOUT** | **FBOUT#** | **PLL** |
| L | X | X | X | X | Float | Float | Float | Float | Off |
| H | **VDD** nominal | L | L | H | L | H | L | H | On |
| H | **VDD** nominal | L | H | L | H | L | H | L | On |
| H | **VDD** nominal | H | L | H | Float | Float | L | H | On |
| H | **VDD** nominal | H | H | L | Float | Float | H | L | On |
| H | **VDD** nominal | X | L | L | Float | Float | Float | Float | Off |
| H | **GND**[3] | L | L | H | L | H | L | H | Bypass/Off |
| H | **GND**<Addt'l Footnote>c | L | H | L | H | L | H | L | Bypass/Off |
| H | **GND**<Addt'l Footnote>c | H | L | H | Float | Float | L | H | Bypass/Off |
| H | **GND**<Addt'l Footnote>c | H | H | L | Float | Float | H | L | Bypass/Off |
| H | **GND**<Addt'l Footnote>c | X | L | L | Float | Float | Float | Float | Bypass/Off |
| H | X | X | H | H | Reserved | | | | |

NOTE 1 The Output Enable (OEn) to disable the output buffer is not an input signal to the SSTE32882, but an internal signal from the PLL powerdown control and test logic. It is controlled by setting or clearing the corresponding bit in the Clock Driver mode register.

NOTE 2 It is illegal to hold both the CK and CK# inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when RESET# is driven HIGH.

NOTE 3 This is a device test mode and all register timing parameter are not guaranteed.

## 2.7 Control Words

The device features a set of control words, which allow the optimization of the device properties for different raw card designs. The different control words and settings are described below. Any change to these control words require some time for the device to settle. For changes to the control word setting, except for RC2 (bit DBA1 and DA3) and RC10, the controller needs to wait $t_{MRD}$ after the last control word access, before further access to the DRAM can take place. For any changes to the clock timing (RC2: bit DBA1 and DA3, and RC10) this settling may take up to $t_{STAB}$ time. All chip select inputs, DCS[n:0]#, must be kept HIGH during that time. The Control Words can be accessed and written to when running within any one defined frequency band.

### 2.7.1 Control Word Decoding

The values to be programmed into each control word are presented on signals DA3, DA4, DBA0 and DBA1 simultaneously with the assertion of the control word access through DCS0# and DCS1#, or DCS2# and DCS3# in the QuadCS enabled mode, and the address of the control word on DA0, DA1, DA2, and DBA2.

The reset default state of Control Words 0 ... 5 and Control Words 8 ... 15 is “0”. The reset default state for Control Words 6 and 7 is Vendor Specific. Every time the device is reset, its default state is restored. Stopping the clocks (CK=CK#=**LOW**) to put the device in low-power mode will not alter the control word settings.

**Table 17 — Control Word Decoding with QuadCS Mode Disabled**

| | | Signal | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Control Word** | **Symbol** | **DCS0#** | **DCS1#** | **DBA2** | **DA2** | **DA1** | **DA0** | **Meaning** |
| None | n/a | H | X | X | X | X | X | No control word access |
| None | n/a | X | H | X | X | X | X | No control word access |
| Control word 0 | RC0 | L | L | L | L | L | L | Global Features Control word |
| Control word 1 | RC1 | L | L | L | L | L | H | Clock Driver Enable Control word |
| Control word 2 | RC2 | L | L | L | L | H | L | Timing Control word |
| Control word 3 | RC3 | L | L | L | L | H | H | CA Signals Driver Characteristics Control word |
| Control word 4 | RC4 | L | L | L | H | L | L | Control Signals Driver Characteristics Control word |
| Control word 5 | RC5 | L | L | L | H | L | H | CK Driver Characteristics Control word |
| Control word 6 | RC6 | L | L | L | H | H | L | Reserved, free to use by vendor |
| Control word 7 | RC7 | L | L | L | H | H | H | Reserved, free to use by vendor |
| Control word 8 | RC8 | L | L | H | L | L | L | Additional IBT Settings Control Word |
| Control word 9 | RC9 | L | L | H | L | L | H | Power Saving Settings Control Word |
| Control word 10 | RC10 | L | L | H | L | H | L | Encoding for RDIMM Operating Speed |
| Control word 11 | RC11 | L | L | H | L | H | H | Encoding for RDIMM Operating VDD |
| Control word 12 | RC12 | L | L | H | H | L | L | Reserved for future use |
| Control word 13 | RC13 | L | L | H | H | L | H | Reserved for future use |
| Control word 14 | RC14 | L | L | H | H | H | L | Reserved for future use |
| Control word 15 | RC15 | L | L | H | H | H | H | Reserved for future use |

### 2.7.1 Control Word Decoding (cont'd)

**Table 18 — Control Word Decoding with QuadCS Mode Enabled**

| | | Signal | | | | | |
|---|---|---|---|---|---|---|---|
| **Control Word** | **Symbol** | **DCS[3:0]#** | **DBA2** | **DA2** | **DA1** | **DA0** | **Meaning** |
| None | n/a | HXHX | X | X | X | X | No control word access |
| None | n/a | HXXH | X | X | X | X | |
| None | n/a | XHHX | X | X | X | X | |
| None | n/a | XHXH | X | X | X | X | |
| None | n/a | HLLL | X | X | X | X | Ilegal Input States |
| None | n/a | LHLL | X | X | X | X | |
| None | n/a | LLHL | X | X | X | X | |
| None | n/a | LLLH | X | X | X | X | |
| Control word 0 | RC0 | LLHH or HHLL or LLLL | L | L | L | L | Global Features Control word |
| Control word 1 | RC1 | | L | L | L | H | Clock Driver Enable Control word |
| Control word 2 | RC2 | | L | L | H | L | Timing Control word |
| Control word 3 | RC3 | | L | L | H | H | CA Signals Driver Characteristics Control word |
| Control word 4 | RC4 | | L | H | L | L | Control Signals Driver Characteristics Control word |
| Control word 5 | RC5 | | L | H | L | H | CK Driver Characteristics Control word |
| Control word 6 | RC6 | | L | H | H | L | Reserved, free to use by vendor |
| Control word 7 | RC7 | | L | H | H | H | Reserved, free to use by vendor |
| Control word 8 | RC8 | | H | L | L | L | Additional IBT Settings Control Word |
| Control word 9 | RC9 | | H | L | L | H | Power Saving Settings Control Word |
| Control word 10 | RC10 | | H | L | H | L | Encoding for RDIMM Operating Speed |
| Control word 11 | RC11 | | H | L | H | H | Encoding for RDIMM Operating VDD |
| Control word 12 | RC12 | | H | H | L | L | Reserved for future use |
| Control word 13 | RC13 | | H | H | L | H | Reserved for future use |
| Control word 14 | RC14 | | H | H | H | L | Reserved for future use |
| Control word 15 | RC15 | | H | H | H | H | Reserved for future use |

### 2.7.2 Control Word Functions

The following clauses describe the contents of each control word.

**Table 19 — RC0: Global Features Control Word**

| Input | | | | Definition | Encoding |
|---|---|---|---|---|---|
| DBA1 | DBA0 | DA4 | DA3 | | |
| x | x | x | 0 | Output Inversion | Output Inversion enabled |
| x | x | x | 1 | | Output Inversion disabled |
| x | x | 0 | x | Floating Outputs (when DCSn# = HIGH, and DA4 = "1") | Float disabled **(normal output drive strength as defined in RC3, 4, and 5)** |
| x | x | 1 | x | | Float enabled **(or Weak Drive mode when RC9 [DA3=1])** |
| x | 0 | x | x | A outputs disabled | A outputs enabled |
| x | 1 | x | x | | A outputs disabled |
| 0 | x | x | x | B outputs disabled | B outputs enabled |
| 1 | x | x | x | | B outputs disabled |

Output floating refers to allowing many A/B outputs to enter a hi-Z state when they are not being used. This is to conserve power when the outputs are resistively terminated to a voltage (e.g., VDD, VTT, or VSS). When output floating is enabled, the following outputs (on both matching A and B outputs) are hi-Z when not actively driven: QxA0, QxA1, QxA2, QxA3, QxA4, QxA5, QxA6, QxA7, QxA8, QxA9, QxA10/AP, QxA11, QxA12/BC, QxA13, QxA14, QxA15, QxBA0, QxBA1, QxBA2, QxRAS#, QxCAS#, and QxWE#.

A or B output disable allows the use of the SSTE32882 in reduced parts count applications such as DDR3 Mini-RDIMMs. When output disable is asserted, all outputs on the corresponding side of the register including the clock drivers remain in Hi-Z at all times.

**Table 20 — RC1: Clock Driver Enable Control Word**

| Input | | | | Definition | Encoding |
|---|---|---|---|---|---|
| DBA1 | DBA0 | DA4 | DA3 | | |
| x | x | x | 0 | Disable Y0/Y0# clock | Y0/Y0# clock enabled |
| x | x | x | 1 | | Y0/Y0# clock disabled |
| x | x | 0 | x | Disable Y1/Y1# clock | Y1/Y1# clock enabled |
| x | x | 1 | x | | Y1/Y1# clock disabled |
| x | 0 | x | x | Disable Y2/Y2# clock | Y2/Y2# clock enabled |
| x | 1 | x | x | | Y2/Y2# clock disabled |
| 0 | x | x | x | Disable Y3/Y3# clock | Y3/Y3# clock enabled |
| 1 | x | x | x | | Y3/Y3# clock disabled |

### 2.7.2 Control Word Functions (cont'd)

Output clocks may be individually turned on or off to conserve power. The system must read the module SPD to determine which clock outputs are used by the module. The PLL remains locked on CK/CK# unless the system stops the clock inputs to the SSTE32882 to enter the lowest power mode.

**Table 21 — RC2: Timing Control Word**

| Input | | | | Definition | Encoding |
|---|---|---|---|---|---|
| DBA1 | DBA0 | DA4 | DA3 | | |
| x | x | x | 0 | Address- and command-nets pre-launch (Control Signals QxCKE, QxCS, QxODT do not apply) | Standard (1/2 Clock) |
| x | x | x | 1 | | Address and command nets pre-launch (3/4 Clock) (Optional)[1] |
| x | x | 0 | x | 1T/3T Output timing | 1T timing |
| x | x | 1 | x | | 3T timing[2] (Optional)<Addt'l Footnote>a |
| x | 0 | x | x | Input Bus Termination[3] | 100 Ohm |
| x | 1 | x | x | | 150 Ohm |
| 0 | x | x | x | Frequency Band Select | Operation (Frequency Band 1) |
| 1 | x | x | x | | Test Mode (Frequency Band 2) |

NOTE 1 Support for (optional) features is vendor specific. Refer to vendor datasheet for supportability
NOTE 2 There is no floating once 3T timing is activated.
NOTE 3 If MIRROR is 'HIGH' then Input Bus Termination (IBT) is turned off on all inputs, except the DCSn# and DODTn inputs.

The Input Bus Termination (IBT) is also located in this control word with two options of 100 ohms or 150 ohms which can be selected to adapt to different system scenarios. At power-up, the SSTE32882 IBT defaults to 100 ohms. The system controller can reprogram the termination resistance to 150 ohms by setting this bit. Only the DAn, DBAn, DRAS#, DCAS#, DWE#, DCSn#, DODT, DCKEn, and PAR_IN inputs have the IBT. The CK, CK#, FBIN, FBIN#, RESET#, and MIRROR inputs do not have IBT.

If MIRROR is 'HIGH', then it is assumed the register is located on the back side of a module where two registers are tied together on the input side. In this case, for the register on the back side, IBT are turned off on all inputs, except the DCSn# and DODTn inputs.

Figure 19 illustrates the pre-launch feature whereby double loaded nets in a 2-rank configuration can be driven with an earlier signal compared to output clock and control in order to compensate for the slower signal travel speed. This timing applies at all supported frequencies.

### 2.7.2 Control Word Functions (cont'd)

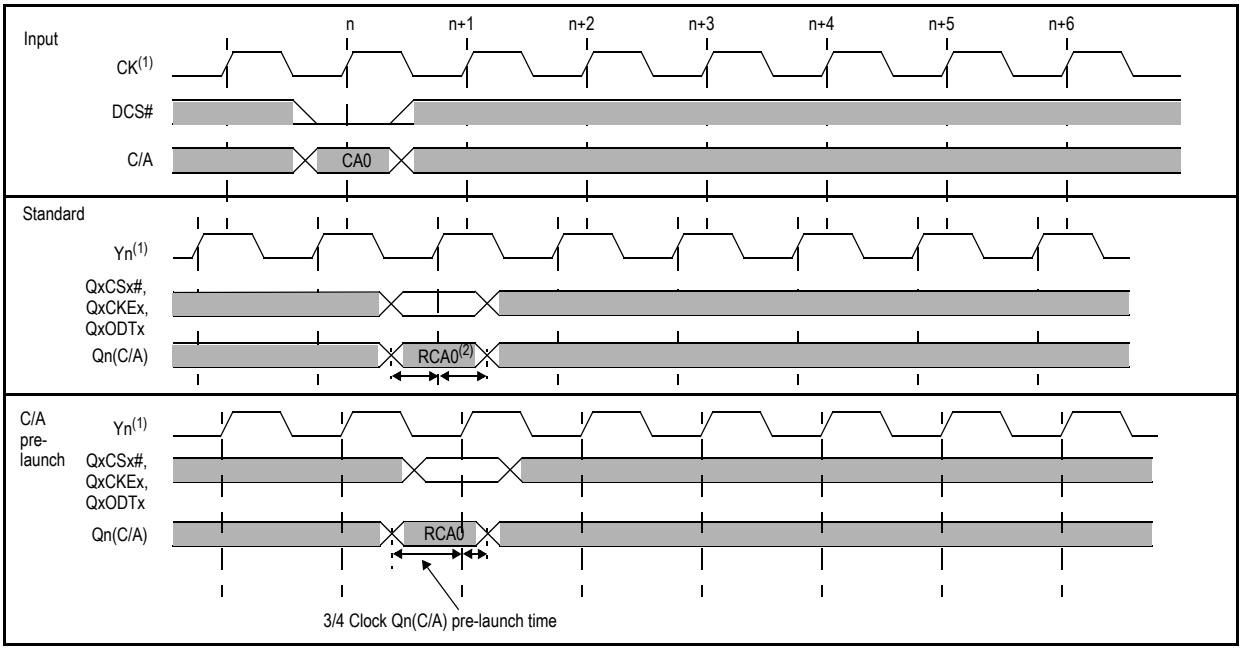



**Figure 19 — Standard versus Address and Command-Nets Pre-launch Timing**

NOTE1 CK# and Yn# left out for better visibility
NOTE 2 RCA0 is re-driven command address signal based on input CA0

Output driver characteristics are separately controlled for outputs that are often loaded with twice as many DRAMs as the other outputs. Outputs are grouped as follows:

- CA Signals =QxA0-QxAn, QxBA0-QxBAn, QxRAS#, QxCAS#, QxWE#
- Control Signals = QxCSn#, QxCKEn, QxODTn
- CK = Yn ... Yn#

## 2.8 Register R-on Targets for Each Drive Strength

**Table 22 — Output R-on Targets**

| Drive Settings | Output Driver R-on Targets (ohms) | | |
|---|---|---|---|
| | Min | Nom | Max |
| Light | 22 | 26 | 30 |
| Moderate | 16 | 19 | 22 |
| Strong | 12 | 14 | 16 |

## 2.8 Register R-on Targets for Each Drive Strength (cont'd)

**Table 23 — RC3: CA Signals Driver Characteristics Control Word**

| Input | | | | Definition | Encoding |
|---|---|---|---|---|---|
| DBA1 | DBA0 | DA4 | DA3 | | |
| x | x | 0 | 0 | Command/Address Driver-A Outputs | Light Drive (4 or 5 DRAM Loads) |
| x | x | 0 | 1 | | Moderate Drive (8 or 10 DRAM Loads) |
| x | x | 1 | 0 | | Strong Drive (16 or 20 DRAM Loads) |
| x | x | 1 | 1 | | Reserved |
| 0 | 0 | x | x | Command/Address Driver-B Outputs | Light Drive (4 or 5 DRAM Loads) |
| 0 | 1 | x | x | | Moderate Drive (8 or 10 DRAM Loads) |
| 1 | 0 | x | x | | Strong Drive (16 or 20 DRAM Loads) |
| 1 | 1 | x | x | | Reserved |

**Table 24 — RC4: Control Signals Driver Characteristics Control Word**

| Input | | | | Definition | Encoding |
|---|---|---|---|---|---|
| DBA1 | DBA0 | DA4 | DA3 | | |
| x | x | 0 | 0 | Control Driver-A Outputs | Light Drive (4 or 5 DRAM Loads) |
| x | x | 0 | 1 | | Moderate Drive (8 or 10 DRAM Loads) |
| x | x | 1 | 0 | | Reserved |
| x | x | 1 | 1 | | Reserved |
| 0 | 0 | x | x | Control Driver-B Outputs | Light Drive (4 or 5 DRAM Loads) |
| 0 | 1 | x | x | | Moderate Drive (8 or 10 DRAM Loads) |
| 1 | 0 | x | x | | Reserved |
| 1 | 1 | x | x | | Reserved |

**Table 25 — RC5: CK Driver Characteristics Control Word**

| Input | | | | Definition | Encoding |
|---|---|---|---|---|---|
| DBA1 | DBA0 | DA4 | DA3 | | |
| x | x | 0 | 0 | Clock Y1, Y1#, Y3, and Y3# Output Drivers | Light Drive (4 or 5 DRAM Loads) |
| x | x | 0 | 1 | | Moderate Drive (8 or 10 DRAM Loads) |
| x | x | 1 | 0 | | Strong Drive (16 or 20 DRAM Loads) |
| x | x | 1 | 1 | | Reserved |
| 0 | 0 | x | x | Clock Y0, Y0#, Y2, and Y2# Output Drivers | Light Drive (4 or 5 DRAM Loads) |
| 0 | 1 | x | x | | Moderate Drive (8 or 10 DRAM Loads) |
| 1 | 0 | x | x | | Strong Drive (16 or 20 DRAM Loads) |
| 1 | 1 | x | x | | Reserved |

## 2.8 Register R-on Targets for Each Drive Strength (cont'd)

**Table 26 — RC8 - Additional IBT Setting Control Word**

| Input | | | | Definition | Encoding |
|---|---|---|---|---|---|
| DBA1 | DBA0 | DA4 | DA3 | | |
| x | 0 | 0 | 0 | IBT Compatibility Settings | IBT as defined in RC2 |
| 0 | x | x | x | Mirror Mode | IBT Off when MIRROR is 'HIGH' [1] |
| 1 | x | x | x | | IBT On when MIRROR is 'HIGH' [2] |
| x | 0 | 0 | 1 | Input Bus Termination[1] | Reserved |
| x | 0 | 1 | 0 | | 200 ohm |
| x | 0 | 1 | 1 | | Reserved |
| x | 1 | 0 | 0 | | 300 ohm |
| x | 1 | 0 | 1 | | Reserved |
| x | 1 | 1 | 0 | | Reserved |
| x | 1 | 1 | 1 | | Off [3] |

NOTE 1 If MIRROR is 'HIGH', then Input Bus Termination (IBT) is turned off on all inputs, except DCSn# and DODTn inputs.
NOTE 2 When DBA0 = 1, DA4 = 1, DA3 = 1, IBT on all inputs is turned off irrespective of DBA1 setting.
NOTE 3 With this setting, irrespective of the logic level of the MIRROR input pin, IBT on all inputs (including DCSn# and DODTn) is turned off.

**Table 27 — RC9: Power Saving Settings Control Word**

| Input | | | | Definition | Encoding |
|---|---|---|---|---|---|
| DBA1 | DBA0 | DA4 | DA3 | | |
| x | x | x | 0 | Weak Drive Mode [1] | "Floating Outputs" as defined in RC0 [DA4] |
| x | x | x | 1 | (when DCSn# = HIGH, DA3=1, and RC0 [DA4=1]) | Weak Drive enabled<br><br>Weak Drive Impedance:<br>70 Ohm (min), 100 Ohm (nom), 120 Ohm (max) |
| x | x | 0 | x | Reserved | Reserved |
| x | x | 1 | x | | Reserved |
| 1 | 0 | x | x | CKE Power Down Mode | CKE power down with IBT ON, QxODT is a function of DxODT |
| 1 | 1 | x | x | | CKE power down with IBT off, QxODT held **LOW** |
| 0 | x | x | x | CKE Power Down Mode Enable | Disabled |
| 1 | x | x | x | | Enabled |

NOTE 1 When all DCS# pins are HIGH (i.e. SDRAM is in deselected state), there is no memory access to the DRAM, and the Register output can either be in a Normal Drive Mode, floated, or driven under Weak Drive Mode. A Weak Drive Mode is a mode in which CA signal output drivers (QxA0-QxAn, QxBA0-QxBAn, QxRAS#, QxCAS#, QxWE#) will be driven 2.5 to 3 times weaker than the Light Drive as specified in RC3, and the SDRAM VIL/VIH DC limit will be maintained. The Weak Drive Mode entry and exit timing is bounded by tDIS and tEN respectively.

The SSTE32882 register supports different power down modes. By default, the Power Down feature is disabled (RC9[DBA1]=0). The register ignores CKE Power Down mode setting when this function is disabled. If the CKE Power Down mode is enabled (RC9[DBA1]=1), then power down is invoked once both DCKE0 and DCKE1 are **LOW**. Bit DBA0 selects how IBT and ODT behave.

## 2.8 Register R-on Targets for Each Drive Strength (cont'd)

**Table 28 — RC10: Encoding for RDIMM Operating Speed**

| Input | | | | Definition | Encoding |
|---|---|---|---|---|---|
| DBA1 | DBA0 | DA4 | DA3 | | |
| x | 0 | 0 | 0 | f ≤ 800 MT/s | DDR3/DDR3L/DDR3U-800 (default) |
| x | 0 | 0 | 1 | 800 MT/s < f ≤ 1066 MT/s | DDR3/DDR3L/DDR3U-1066 |
| x | 0 | 1 | 0 | 1066 MT/s < f ≤ 1333 MT/s | DDR3/DDR3L/DDR3U-1333 |
| x | 0 | 1 | 1 | 1333 MT/s < f ≤ 1600 MT/s | DDR3/DDR3L/DDR3U-1600 |
| x | 1 | 0 | 0 | 1600 MT/s < f ≤ 1866 MT/s | DDR3-1866 |
| x | 1 | 0 | 1 | Reserved | Reserved |
| x | 1 | 1 | 0 | Reserved | Reserved |
| x | 1 | 1 | 1 | Reserved | Reserved |
| NOTE The encoding value is used to inform the register the operating speed that it is being run at in a system. It is not an indicator of how fast or slow a register can run. | | | | | |

RC11 will be used to inform SSTE32882 under what operating voltage $V_{DD}$ will be used. Register can use the information to optimize their functionality and performance at DDR3L conditions.

**Table 29 — RC11: Operating Voltage VDD and VREFCA Control Word [1]**

| Input | | | | Definition | Encoding |
|---|---|---|---|---|---|
| DBA1 | DBA0 | DA4 | DA3 | | |
| x | x | 0 | 0 | Register VDD Operating Voltage | DDR3 1.5 V mode |
| x | x | 0 | 1 | | DDR3L 1.35 V mode |
| x | x | 1 | 0 | | DDR3U 1.25 V mode |
| x | x | 1 | 1 | | Reserved |
| x | 0 | x | x | Register VrefCA[2] | External VrefCA<Addt'l Footnote>b |
| x | 1 | x | x | | Internal VrefCA<Addt'l Footnote>b |
| 0 | x | x | x | | Reserved |
| 1 | x | x | x | | Reserved |
| NOTE 1 DDR3U 1.5 V, 1.35 V or 1.25 V register is backward compatible and operable to DDR3 & DDR3L specification. To guarantee all timings and specifications for DDR3 & DDR3L, the register must be configured accordantly.<br>NOTE 2 Mandatory for all register supporting 1866 and beyond. | | | | | |

## 2.9 Logic Diagram

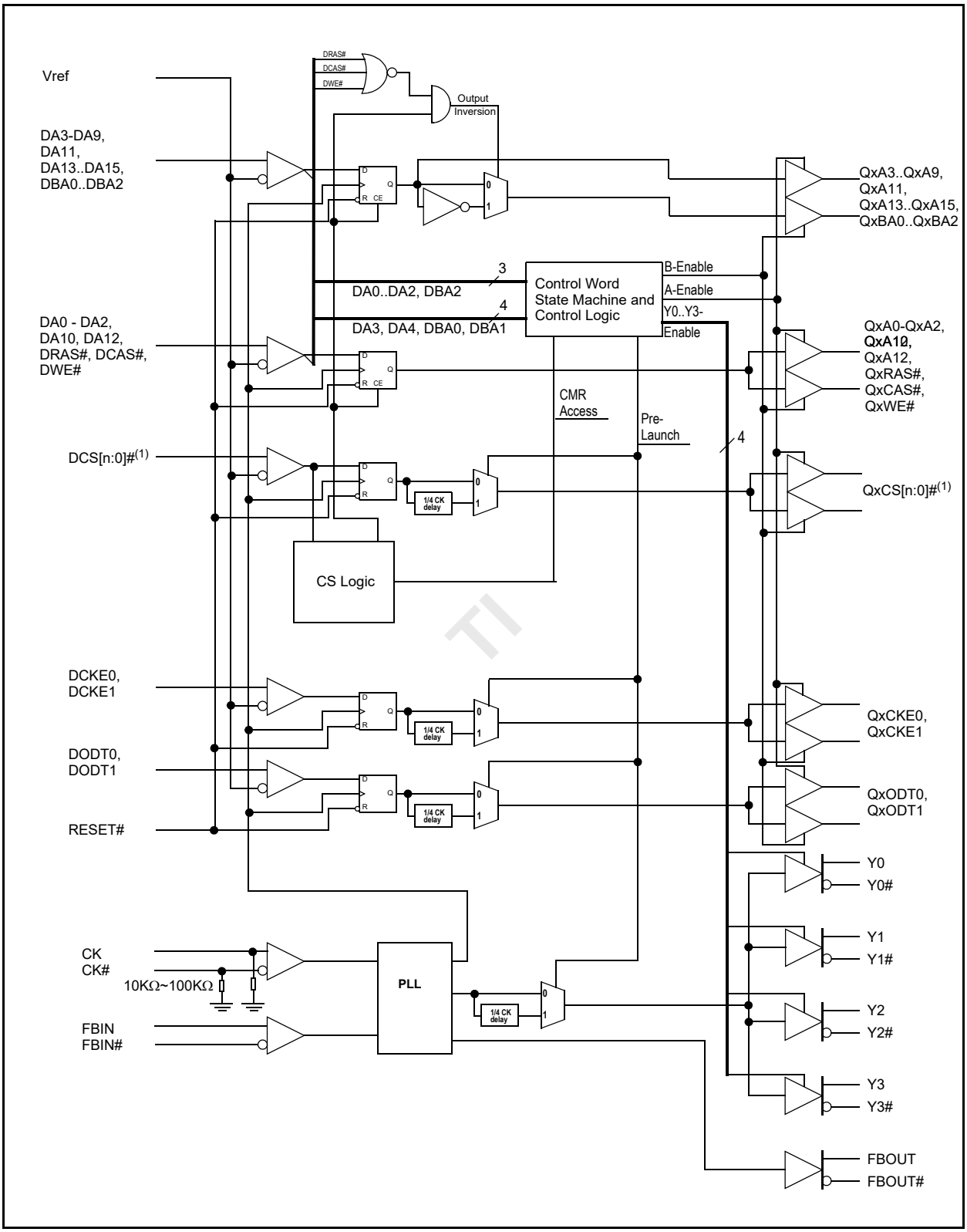



**Figure 20 — Logic Diagram (Positive Logic)**

## 2.9 Logic Diagram (cont'd)

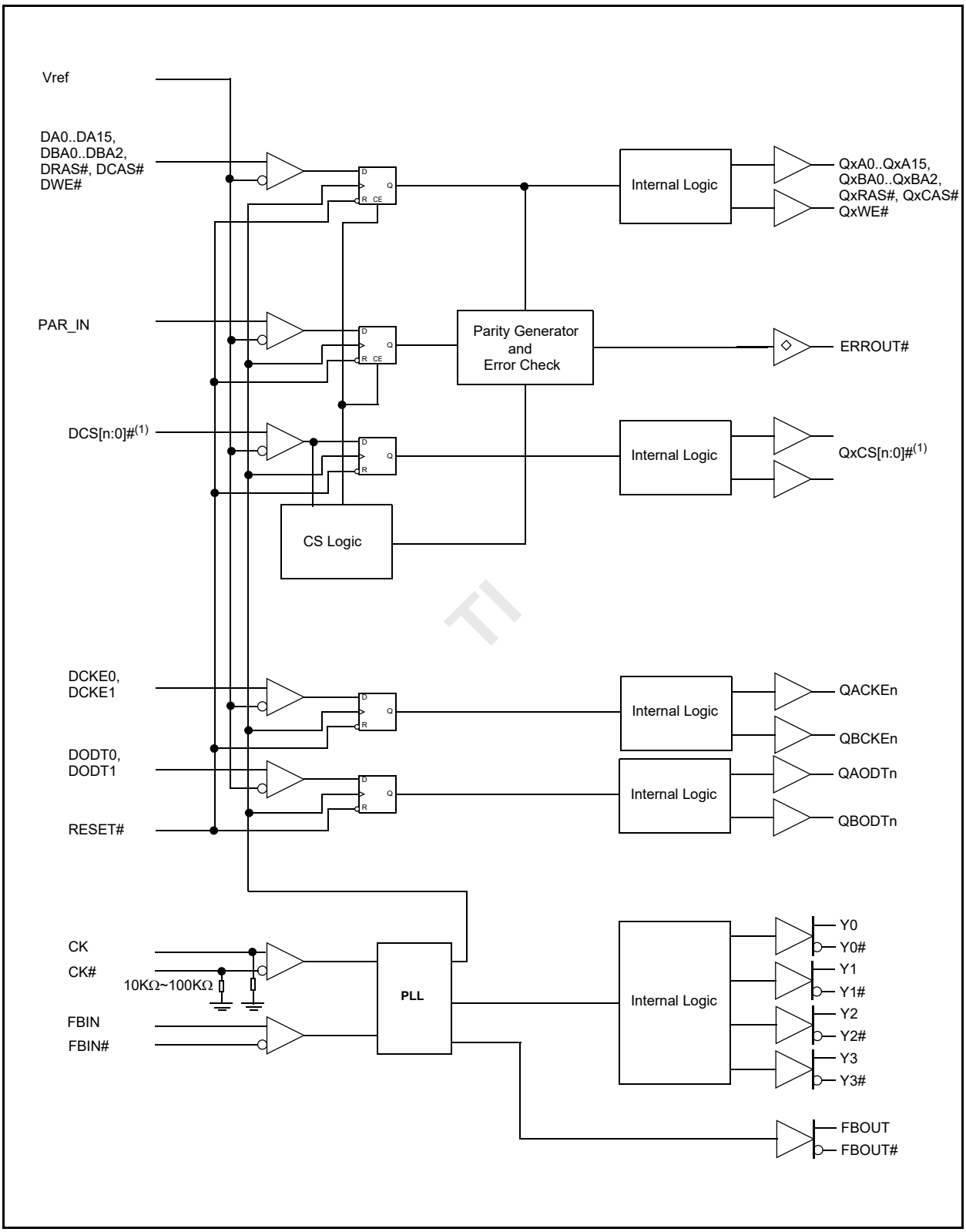



**Figure 21 — Parity Logic Diagram (Positive Logic)**

## 2.10 Absolute Maximum Ratings

**Table 30 — Absolute Maximum Ratings Over Operating Free-air Temperature Range**[1]

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| VDD | Supply voltage | | –0.4 | +1.975 | V |
| VI | Receiver input voltage | See NOTES 2 and 3 | –0.4 | VDD + 0.5 | V |
| VREF | Reference voltage | | –0.4 | VDD + 0.5 | V |
| VO | Driver output voltage | See NOTES 2 and 3 | –0.4 | VDD + 0.5 | V |
| IIK | Input clamp current | VI < 0 or VI > VDD | - | -50 | mA |
| IOK | Output clamp current | VO < 0 or VO > VDD | - | ±50 | mA |
| IO | Continuous output current | 0 < VO < VDD | - | ±50 | mA |
| ICCC | Continuous current through each VDD or GND pin | | - | ±100 | mA |
| $T_{stg}$ | Storage temperature | | –65 | +150 | °C |

NOTE 1 Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 2 The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
NOTE 3 This value is limited to 1.975 V maximum.

## 2.11 DC and AC Specifications

The SSTE32882 parametric values are specified for the device default control word settings, unless otherwise stated. Note that the RC10 setting does not affect any of the parametric values.

**Table 31 — Operating Electrical Characteristics**

| Symbol | Parameter | Signals | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|
| VDD | DC Supply voltage (1.5 V Operation) | | 1.425 | 1.5 | 1.575 | V |
| | DC Supply voltage (1.35 V Operation) | | 1.282 | 1.35 | 1.451 | V |
| VREF | DC Reference voltage | | 0.49 x VDD | 0.50 x VDD | 0.51 x VDD | V |
| VTT | DC Termination voltage | | $V_{REF}$ – 40 mV | $V_{REF}$ | $V_{REF}$ + 40 mV | V |
| VIH(AC) | AC HIGH-level input voltage (1.5 V Operation, DDR3-800/1066/1333) | Data inputs[1] | $V_{REF}$ + 175 mV | – | VDD + 0.4 | V |
| | AC HIGH-level input voltage (1.5 V Operation, DDR3-1600) | Data inputs[1] | $V_{REF}$ + 150 mV | – | VDD + 0.4 | V |
| | AC HIGH-level input voltage (1.5 V Operation, DDR3-1866) | Data inputs[1] | $V_{REF}$ + 135 mV | | VDD + 0.4 | V |
| | AC HIGH-level input voltage (1.35 V Operation, DDR3L-800/1066/1333) | Data inputs[1] | $V_{REF}$ + 150 mV | – | VDD + 0.2 | V |
| | AC HIGH-level input voltage (1.35 V Operation, DDR3L-1600) | Data inputs[1] | $V_{REF}$ + 135 mV | – | VDD + 0.2 | V |
| VIL(AC) | AC LOW-level input voltage (1.5 V Operation, DDR3-800/1066/1333) | Data inputs[1] | –0.4 | – | $V_{REF}$ – 175 mV | V |
| | AC LOW-level input voltage (1.5 V Operation, DDR3-1600) | Data inputs[1] | –0.4 | – | $V_{REF}$ – 150 mV | V |
| | AC LOW-level input voltage (1.5 V Operation, DDR3-1866) | Data inputs[1] | -0.4 | – | $V_{REF}$ - 135 mV | V |
| | AC LOW-level input voltage(1.35 V Operation, DDR3L-800/1066/1333) | Data inputs[1] | –0.2 | – | $V_{REF}$ – 150 mV | V |
| | AC LOW-level input voltage (1.35 V Operation, DDR3L-1600) | Data inputs[1] | –0.2 | – | $V_{REF}$ – 135 mV | V |
| VIH(DC) | DC HIGH-level input voltage(1.5 V Operation) | Data inputs[1] | $V_{REF}$ + 100 mV | – | VDD + 0.4 | V |
| | DC HIGH-level input voltage(1.35 V Operation) | Data inputs[1] | $V_{REF}$ + 90 mV | – | VDD + 0.2 | V |
| VIL(DC) | DC LOW-level input voltage(1.5 V Operation) | Data inputs[1] | –0.4 | – | $V_{REF}$ – 100 mV | V |
| | DC LOW-level input voltage(1.35 V Operation) | Data inputs[1] | –0.2 | – | $V_{REF}$ – 90 mV | V |
| VIH(CMOS) | HIGH-level input voltage | CMOS inputs[2] | 0.65 x VDD | – | VDD | V |
| VIL(CMOS) | LOW-level input voltage | CMOS inputs[2] | 0 | – | 0.35 x VDD | V |
| VIL (Static) | Static LOW-level input voltage[3] | CK, CK#, | - | – | 0.35 x VDD | V |
| VIX(AC) | Differential input crosspoint voltage range(1.5 V Operation, DDR3-800/1066/1333/1600) | CK, CK#, FBIN, FBIN# | 0.5xVDD - 175 mV | 0.5 x VDD | 0.5xVDD + 175 mV | V |
| | | | 0.5xVDD - 200 mV [4] | 0.5 x VDD | 0.5xVDD + 200 mV [4] | V |
| | Differential input crosspoint voltage range(1.5 V Operation, DDR3-1866) | CK, CK#, FBIN, FBIN# | 0.5xVDD - 150mV | 0.5 x VDD | 0.5xVDD + 150 mV | V |
| | | | 0.5xVDD - 180mV [5] | 0.5 x VDD | 0.5xVDD + 180 mV [5] | V |
| | Differential input crosspoint voltage range(1.35 V Operation, DDR3L-800/1066/1333/1600) | CK, CK#, FBIN, FBIN# | 0.5xVDD - 150 mV | 0.5 x VDD | 0.5xVDD + 150 mV | V |
| | | | 0.5xVDD - 180 mV [6] | 0.5 x VDD | 0.5xVDD + 180 mV [6] | V |
| VID(AC) | Differential input voltage[7] (1.5 V Operation, DDR3-800/1066/1333) | CK, CK# | 350 | – | VDD | mV |
| | Differential input voltage[7](1.5 V Operation, DDR3-1600) | CK, CK# | 300 | – | VDD | mV |
| | Differential input voltage[7](1.5 V Operation, DDR3-1866) | CK, CK# | 270 | – | VDD | mV |
| | Differential input voltage[7](1.35 V Operation, DDR3-800/1066/1333) | CK, CK# | 300 | – | VDD | mV |
| | Differential input voltage[7] (1.35 V Operation, DDR3-1600) | CK, CK# | 270 | – | VDD | mV |
| IOH | HIGH-level output current[8] | All outputs except ERROUT# | -11 | – | – | mA |
| IOL | LOW-level output current[8] | All outputs except ERROUT# | 11 | – | –- | mA |
| IOL | LOW-level output current | ERROUT# | 25 | – | – | mA |
| VOD | Differential re-driven clock swing (1.5 V Operation) | Yn, Yn# | 500 | – | VDD | mV |
| | Differential re-driven clock swing (1.35 V Operation) | Yn, Yn# | 450 | – | VDD | mV |
| VOX | Differential Output Crosspoint Voltage (1.5 V Operation) | Yn, Yn# | 0.5xVDD – 100 mV | – | 0.5xVDD + 100 mV | V |
| | Differential Output Crosspoint Voltage (1.35 V Operation) | Yn, Yn# | 0.5xVDD – 90 mV | – | 0.5xVDD + 90 mV | V |

## Table 31 — Operating Electrical Characteristics (cont'd)

| Symbol | Parameter | | Signals | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|---|
| | | DDR3/DDR3L - 800 | DDR3/DDR3L - 1066 | DDR3/DDR3L - 1333 | DDR3/DDR3L -1600 | DDR3-1866 | |
| $T_{case\ (max)}$ | Case temperature [9] | 109[10] | 108[10] | 106[10] | 103[10] | 101[10] | °C |

NOTE 1 DCKE0/1, DODT0/1, DA0..DA15, DBA0..DBA2, DRAS#, DCAS#, DWE#, PAR_IN, DCS[1:0]# when QCSEN# = HIGH, DCS[3:0]# when QCSEN# = LOW.
NOTE 2 RESET#, MIRROR
NOTE 3 This spec applies only when both CK and CK# are actively driven LOW. It does not apply when CK/CK# are floating.
NOTE 4 Extended range for Vix is only allowed for clock (CK and CK#) and if single-ended clock input signals CK and CK# are monotonic with a single-ended swing VSEL / VSEH of at least VDD/2 +/-275 mV, and when the differential slew rate of CK - CK# is larger than 4 V/ns.
NOTE 5 Extended range for Vix is only allowed for clock (CK and CK#) and if single-ended clock input signals CK and CK# are monotonic with a single-ended swing VSEL / VSEH of at least VDD/2 +/-243 mV, and when the differential slew rate of CK - CK# is larger than 4 V/ns.
NOTE 6 Extended range for Vix is only allowed for clock (CK and CK#) and if single-ended clock input signals CK and CK# are monotonic with a single-ended swing VSEL / VSEH of at least VDD/2 +/-243 mV, and when the differential slew rate of CK - CK# is larger than 3.6 V/ns
NOTE 7 VID is the magnitude of the difference between the input level on CK and the input level on CK# See Diagram (Figure 32, "Voltage Waveforms; Input Clock")
NOTE 8 Default settings
NOTE 9 Measurement procedure JESD51-2
NOTE 10 This spec is meant to guarantee a Tj of 125C by the SSTE32882 device. Since Tj cannot be measured or observed by users, Tcase is specified instead. Under all thermal condition, the Tj of a SSTE32882 device shall not be higher than 125 °C.

## Table 32 — Operating Electrical Characteristics (DDR3U 1.25 V)

| Symbol | Parameter | Signals | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | DC Supply voltage (1.25 V Operation) | | 1.19 | 1.25 | 1.31 | V |
| $V_{REF}$ | DC Reference voltage | | 0.49 x $V_{DD}$ | 0.50 x $V_{DD}$ | 0.51 x $V_{DD}$ | V |
| $V_{TT}$ | DC Termination voltage | | $V_{REF}$ – 40 mV | $V_{REF}$ | $V_{REF}$ + 40 mV | V |
| $V_{IH(AC)}$ | AC HIGH-level input voltage (1.25 V Operation, DDR3U-800/1066/1333/1600) | Data inputs[1] | $V_{REF}$ + 125 mV | – | $V_{DD}$ + 0.2 | V |
| $V_{IL(AC)}$ | AC LOW-level input voltage (1.25 V Operation, DDR3U-800/1066/1333/1600) | Data inputs[1] | –0.2 | – | $V_{REF}$ – 125 mV | V |
| $V_{IH(DC)}$ | DC HIGH-level input voltage(1.25 V Operation) | Data inputs[1] | $V_{REF}$ + 90 mV | – | $V_{DD}$ + 0.2 | V |
| $V_{IL(DC)}$ | DC LOW-level input voltage(1.25 V Operation) | Data inputs[1] | –0.2 | – | $V_{REF}$ – 90 mV | V |
| $V_{IH(CMOS)}$ | HIGH-level input voltage | CMOS inputs[2] | 0.65 x VDD | – | $V_{DD}$ | V |
| $V_{IL(CMOS)}$ | LOW-level input voltage | CMOS inputs[2] | 0 | – | 0.35 x VDD | V |
| $V_{IL\ (Static)}$ | Static LOW-level input voltage[3] | CK, CK#, | - | – | 0.35 x VDD | V |
| $V_{IX(AC)}$ | Differential input crosspoint voltage range(1.25 V Operation, DDR3U-800/1066/1333/1600) | CK, CK#, FBIN, FBIN# | 0.5x$V_{DD}$ - 150 mV | 0.5 x VDD | 0.5x$V_{DD}$ + 150 mV | V |
| | | | 0.5x$V_{DD}$ - 180 mV [4] | 0.5 x VDD | 0.5x$V_{DD}$ + 180 mV [5] | V |
| $V_{ID(AC)}$ | Differential input voltage[6](1.25 V Operation, DDR3U-800/1066/1333/1600) | CK, CK# | 250 | – | VDD | mV |
| $I_{OH}$ | HIGH-level output current[5] | All outputs except ERROUT# | -11 | – | – | mA |
| $I_{OL}$ | LOW-level output current[7] | All outputs except ERROUT# | 11 | – | –- | mA |
| $I_{OL}$ | LOW-level output current | ERROUT# | 25 | – | – | mA |
| $V_{OD}$ | Differential re-driven clock swing (1.25 V Operation) | Yn, Yn# | 400 | – | VDD | mV |
| $V_{OX}$ | Differential Output Crosspoint Voltage (1.25 V Operation) | Yn, Yn# | 0.5xVDD – 90 mV | – | 0.5xVDD + 90 mV | V |
| | | DDR3U-800 | DDR3U-1066 | DDR3U-1333 | DDR3U-1600 | |
| Tcase (max) | Case temperature[6] | 109[7] | 108[7] | 106[7] | 103[7] | °C |

NOTE 1 DCKE0/1, DODT0/1, DA0..DA15, DBA0..DBA2, DRAS#, DCAS#, DWE#, PAR_IN, DCS[1:0]# when QCSEN# = HIGH, DCS[3:0]# when QCSEN# = LOW.
NOTE 2 RESET#, MIRROR
NOTE 3 This spec applies only when both CK and CK# are actively driven LOW. It does not apply when CK/CK# are floating.
NOTE 4 Extended range for Vix is only allowed for clock (CK and CK#) and if single-ended clock input signals CK and CK# are monotonic with a single-ended swing VSEL / VSEH of at least VDD/2 +/-243 mV, and when the differential slew rate of CK - CK# is larger than 3.6 V/ns
NOTE 5 Default settings
NOTE 6 Measurement procedure JESD51-2
NOTE 7 This spec is meant to guarantee a Tj of 125 °C by the SSTE32882 device. Since Tj cannot be measured or observed by users, Tcase is specified instead. Under all thermal condition, the Tj of a SSTE32882 device shall not be higher than 125 °C.

## 2.11 DC and AC Specifications (cont'd)

**Table 33 — AC Overshoot/Undershoot Specification for Address, Command, and Control pins**

| | DDR3/3L-800 | DDR3/3L-1066 | DDR3/3L-1333 | DDR3/3L-1600 | DDR3-1866 |
|---|---|---|---|---|---|
| Maximum peak amplitude allowed for overshoot area (See Figure 22) | 0.4 V | 0.4 V | 0.4 V | 0.4 V | 0.4 V |
| Maximum peak amplitude allowed for undershoot area (See Figure 22) | 0.4 V | 0.4 V | 0.4 V | 0.4 V | 0.4 V |
| Maximum overshoot area above VDD (See Figure 22) | 0.7 V-ns | 0.53 V-ns | 0.42 V-ns | 0.35 V-ns | 0.30 V-ns |
| Maximum undershoot area below VSS (See Figure 22) | 0.7 V-ns | 0.53 V-ns | 0.42 V-ns | 0.35 V-ns | 0.30 V-ns |
| (DA0..DA15, DBA0..DBA2, DRAS#, DCAS#, DWE#, DCS[3:0]#, DCKE0/1, DODT0/1) | | | | | |

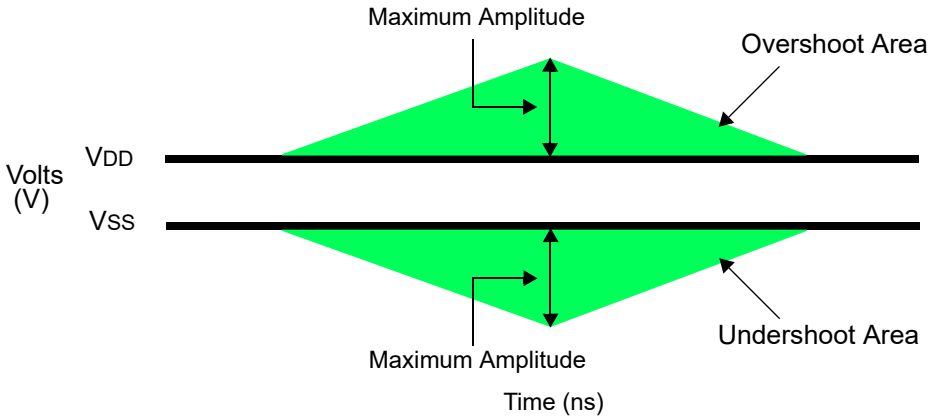



**Figure 22 — Address, Command, and Control Overshoot and Undershoot Definition**

**Table 34 — AC Overshoot/Undershoot Specification for Clock**

| | DDR3/3L-800 | DDR3/3L-1066 | DDR3/3L-1333 | DDR3/3L-1600 | DDR3-1866 |
|---|---|---|---|---|---|
| Maximum peak amplitude allowed for overshoot area (See Figure 23) | 0.4 V | 0.4 V | 0.4 V | 0.4 V | 0.4 V |
| Maximum peak amplitude allowed for undershoot area (See Figure 23) | 0.4 V | 0.4 V | 0.4 V | 0.4 V | 0.4 V |
| Maximum overshoot area above VDDQ (See Figure 23) | 0.5 V-ns | 0.38 V-ns | 0.30 V-ns | 0.25 V-ns | 0.21 V-ns |
| Maximum undershoot area below VSSQ (See Figure 23) | 0.5 V-ns | 0.38 V-ns | 0.30 V-ns | 0.25 V-ns | 0.21 V-ns |
| (CK, CK#) | | | | | |

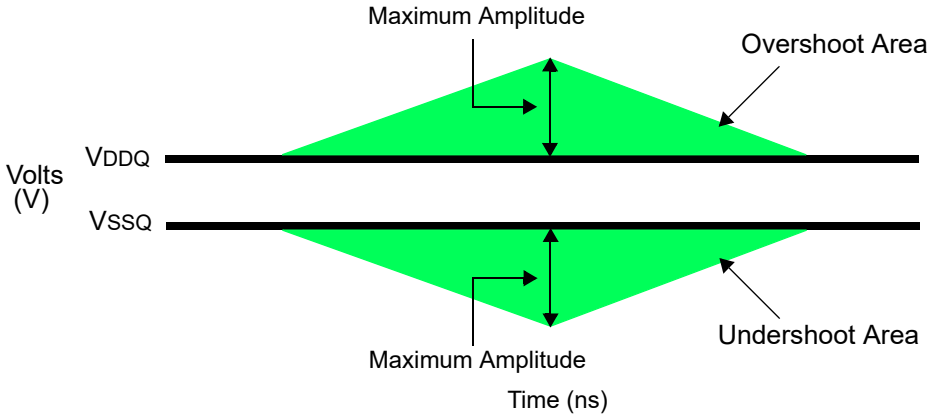



**Figure 23 — Clock Overshoot and Undershoot Definition**

## 2.12 DC Specifications, IDD Specifications

### Table 35 — DC Electrical Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH voltage | $I_{OH}$ = –11 mA | $V_{DD}$-0.4 | - | - | V |
| $V_{OL}$ | Output LOW voltage | $I_{OL}$ = 11 mA | - | - | 0.4 | V |
| $V_{OL}$ | Output LOW voltage ERROUT# | $I_{OL}$ = 25 mA | - | - | 0.4 | V |
| $I_I$ | Input current | RESET#, MIRROR, $V_I = V_{DD}$ or GND | - | - | ±5 | mA |
| $I_I$ | Input current | QCSEN#, $V_I = V_{DD}$ or GND | -150 | | 5 | mA |
| $I_{ID}$ | Input current | Data inputs[1], $V_I = V_{DD}$ or GND | - | - | ±5 | mA |
| $I_{ID}$ | Input current | CK, CK# [2]; $V_I = V_{DD}$ or GND | -5 | | 150 | mA |
| $I_{DD}$ | Static standby current | RESET# = GND and CK, CK# = $V_{IL}$ | - | - | 5 | mA |
| | Static operating current | RESET# = $V_{DD}$, MIRROR=$V_{DD}$, RC8=X111, IBT OFF, Clock inputs not switching (held static **LOW**), $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$ | - | - | 15 | mA |
| $I_{DDD}$ | Dynamic operating current — input clock only | RESET# = $V_{DD}$; MIRROR=$V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK and CK# switching at 50% duty cycle. $I_O$ = 0; $V_{DD}$ = V**DD(max)** | - | vs[3] | - | mA/MHz |
| | Dynamic operating current — per each data input | RESET# = $V_{DD}$; MIRROR=VDD, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK and CK# switching at 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle. $I_O$ = 0; $V_{DD}$ = V**DD(max)** | - | vs<Addt'l Footnote> c | - | mA/MHz |

NOTE 1 DCKE0/1, DODT0/1, DA0..DA15, DBA0..DBA2, DRAS#, DCAS#, DWE#, PAR_IN, DCS[1:0]# when QCSEN# = HIGH, DCS[3:0]# when QCSEN# = LOW are measured while RESET# pulled LOW.
NOTE 2 The CK and CK# inputs have internal pull-down resistors in the range of 10 KW to 100 KW.
NOTE 3 Vendor Specific, must be supplied by register vendor for full device description.

### Table 36 — Capacitance Values

| Symbol | Parameter | Conditions | DDR3/DDR3L/DDR3U 800/1066/1333/1600 | | | DDR3-1866 | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Unit |
| $C_I$ | Input capacitance, Data inputs | see footnotes[1,2] | 1.5 | - | 2.5 | 1.5 | - | 2.2 | pF |
| | Input capacitance, CK, CK#, FBIN, FBIN# | see footnote<Addt'l Footnote>a | 1.5 | - | 2.5 | 1.5 | - | 2.2 | pF |
| $C_{ID}$ | Delta capacitance over all inputs | | | - | 0.5 | - | - | 0.5 | pF |
| $C_{IR}$ | Input capacitance, RESET#, MIRROR, QCSEN# | VI = VDD or GND; VDD = 1.5 V | | | 3 | - | - | 3 | pF |

NOTE 1 This parameter is not subject to production test. It is verified by design and characterization. Input capacitance is measured according to JEP147 ("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER (VNA)") with VDD, VSS, AVDD, AVSS, PVDD, PVSS, $V_{REF}$ applied and all other pins (except the pin under test) floating. Input capacitance are measured with the device default settings when MIRROR=**LOW**.
NOTE 2 Data inputs are DCKE0/1, DODT0/1, DA0..DA15, DBA0..DBA2, DRAS#, DWE#, PAR_IN, and DCS[1:0]# when QCSEN# = HIGH, DCS[3:0]# when QCSEN# = LOW

## 2.13 Timing Requirements

**Table 37 — Timing Requirements**

| Symbol | Parameter | Conditions | DDR3/DDR3L-800/1066/1333 | | DDR3/DDR3L-1600 | | DDR3-1866 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| $f_{clock}$ | Input clock frequency | application frequency[1] | 300 | 670 | 300 | 810 | 300 | 945 | MHz |
| $f_{TEST}$ | Input clock frequency | Test frequency[2] | 70 | 300 | 70 | 300 | 70 | 300 | MHz |
| $t_{CH}/t_{CL}$ | Pulse duration, CK, CK# HIGH or LOW | | 0.4 | - | 0.4 | - | 0.4 | - | $t_{CK}$[3] |
| $t_{ACT}$ | Inputs active time[4] before RESET# is taken HIGH | DCKE0/1=LOW and DCS[n:0]#=HIGH | 8 | - | 8 | - | 8 | - | $t_{CK}$[3] |
| $t_{MRD}$ | Command word to command word programming delay | Number of clock cycles between two command programming accesses | 8 | - | 8 | - | 8 | - | $t_{CK}$[3] |
| $t_{InDIS}$ | Input buffers (except for CK/CK#, DCKEn, DODTn and RESET#) disable time after DCKE[1:0] is **LOW** | DCKE[1:0] = LOW; RESET# = HIGH; CK/CK# = Toggling; RC9[DBA1]=1 and RC9[DBA0]= 0 or 1 | 1 | 4 | 1 | 4 | 1 | 4 | $t_{CK}$[3] |
| $t_{QDIS}$ | Output buffers (except for Yn/Yn#, QxCKEn, QxODTn and FBOUT/FBOUT#) hi-z after QxCKEn is driven **LOW** | DCKE[1:0] = **LOW**; RESET# = HIGH; CK/CK# = toggling; RC9[DBA1]=1 and RC9[DBA0]=0 or 1 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | $t_{CK}$[3] |
| $t_{CKoff}$ | Number of tCK required for both DCKE0 and DCKE1 to remain LOW before both CK/CK# are driven LOW | DCKE[1:0] = LOW; RESET# = HIGH; CK/CK# = Toggling | 5 | - | 5 | - | 5 | - | $t_{CK}$ |
| $t_{CKEV}$ | Input buffers (DCKE0 and DCKE1) disable time after Ck/CK# = LOW | DCKE[1:0] = LOW; RESET# = HIGH; CK/CK# = LOW | 2 | - | 2 | - | 2 | - | $t_{CK}$ |
| tFixedoutput | Static register output after DCKE0 or DCKE1 is HIGH at the input (exit from Power saving state) | RC9[DBA1]=1 and RC9[DBA0]=0 or 1 | 1 | 3 | 1 | 4 | 1 | 4 | $t_{CK}$[3] |
| $t_{SU}$ | Setup time[5] | Input valid before CK/CK# | 100 | - | 50 | - | 40 | - | ps |
| $t_{H}$ | Hold time[6] | Input to remain valid after CK/CK# | 175 | - | 125 | - | 75 | - | ps |

NOTE 1 All specified timing parameters apply

NOTE 2 Timing parameters specified for frequency band 2 apply

NOTE 3 Clock cycle time

NOTE 4 This parameter is not necessarily production tested (see Figure 24, "Voltage Waveforms for Setup and Hold Times – Hold Time Calculation").

NOTE 5 Setup (tSU) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and first crossing of VIH(ac)min. Setup (tSU) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIL(ac)max (see Figure 24, "Voltage Waveforms for Setup and Hold Times – Hold Time Calculation"). If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(dc) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(dc) to ac region', the slew rate of a tangent line to the actual signal from the ac level to VREF(dc) level is used for derating value (see Figure 24, "Voltage Waveforms for Setup and Hold Times – Hold Time Calculation").

NOTE 6 Hold (tH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of VREF(dc). Hold (tH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of VREF(dc) (see Figure 24, "Voltage Waveforms for Setup and Hold Times – Hold Time Calculation"). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to VREF(dc) region' use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to VREF(dc) region', the slew rate of a tangent line to the actual signal from the DC level to VREF(dc) level is used for derating value (see Figure 24, "Voltage Waveforms for Setup and Hold Times – Hold Time Calculation" ).

## 2.13 Timing Requirements (cont'd)

**Table 38 — Timing Requirements (DDR3U 1.25 V)**

| Symbol | Parameter | Conditions | DDR3U-800/1066/1333 | | DDR3U-1600 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $f_{clock}$ | Input clock frequency | application frequency[1] | 300 | 670 | 300 | 810 | MHz |
| $f_{TEST}$ | Input clock frequency | Test frequency[2] | 70 | 300 | 70 | 300 | MHz |
| $t_{CH}/t_{CL}$ | Pulse duration, CK, CK# HIGH or LOW | | 0.4 | - | 0.4 | - | $t_{CK}$[3] |
| $t_{ACT}$ | Inputs active time[4] before RESET# is taken HIGH | DCKE0/1=LOW and DCS[n:0]#=HIGH | 8 | - | 8 | - | $t_{CK<Addt'l Footnote>c}$ |
| $t_{MRD}$ | Command word to command word programming delay | Number of clock cycles between two command programming accesses | 8 | - | 8 | - | $t_{CK}$[3] |
| $t_{InDIS}$ | Input buffers (except for CK/CK#, DCKEn, DODTn and RESET#) disable time after DCKE[1:0] is **LOW** | DCKE[1:0] = LOW; RESET# = HIGH; CK/CK# = Toggling; RC9[DBA1]=1 and RC9[DBA0]= 0 or 1 | 1 | 4 | 1 | 4 | $t_{CK}$[3] |
| $t_{QDIS}$ | Output buffers (except for Yn/Yn#, QxCKEn, QxODTn and FBOUT/FBOUT#) hi-z after QxCKEn is driven **LOW** | DCKE[1:0] = **LOW**; RESET# = HIGH; CK/CK# = toggling; RC9[DBA1]=1 and RC9[DBA0]=0 or 1 | 1.5 | 1.5 | 1.5 | 1.5 | $t_{CK}$[3] |
| $t_{CKoff}$ | Number of tCK required for both DCKE0 and DCKE1 to remain LOW before both CK/CK# are driven LOW | DCKE[1:0] = LOW; RESET# = HIGH; CK/CK# = Toggling | **5** | **-** | **5** | **-** | $t_{CK}$ |
| $t_{CKEV}$ | Input buffers (DCKE0 and DCKE1) disable time after Ck/CK# = LOW | DCKE[1:0] = LOW; RESET# = HIGH; CK/CK# = LOW | **2** | **-** | **2** | **-** | $t_{CK}$ |
| $t_{Fixedoutput}$ | Static register output after DCKE0 or DCKE1 is HIGH at the input (exit from Power saving state) | RC9[DBA1]=1 and RC9[DBA0]=0 or 1 | 1 | 3 | 1 | 3 | $t_{CK}$[3] |
| $t_{SU}$ | Setup time[5] | Input valid before CK/CK# | 100 | - | 50 | - | ps |
| $t_{H}$ | Hold time[6] | Input to remain valid after CK/CK# | 175 | - | 125 | - | ps |

NOTE 1 All specified timing parameters apply

NOTE 2 Timing parameters specified for frequency band 2 apply

NOTE 3 Clock cycle time

NOTE 4 This parameter is not necessarily production tested (see Figure 24, "Voltage Waveforms for Setup and Hold Times – Hold Time Calculation").

NOTE 5 Setup (tSU) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and first crossing of VIH(ac)min. Setup (tSU) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIL(ac)max (see Figure 24, "Voltage Waveforms for Setup and Hold Times – Hold Time Calculation"). If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(dc) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(dc) to ac region', the slew rate of a tangent line to the actual signal from the ac level to VREF(dc) level is used for derating value (see Figure 24, "Voltage Waveforms for Setup and Hold Times – Hold Time Calculation").

NOTE 6 Hold (tH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of VREF(dc). Hold (tH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of VREF(dc) (see Figure 24, "Voltage Waveforms for Setup and Hold Times – Hold Time Calculation"). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to VREF(dc) region' use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to VREF(dc) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(dc) level is used for derating value (see Figure 24, "Voltage Waveforms for Setup and Hold Times – Hold Time Calculation" ).

**2.13 Timing Requirements (cont'd)**

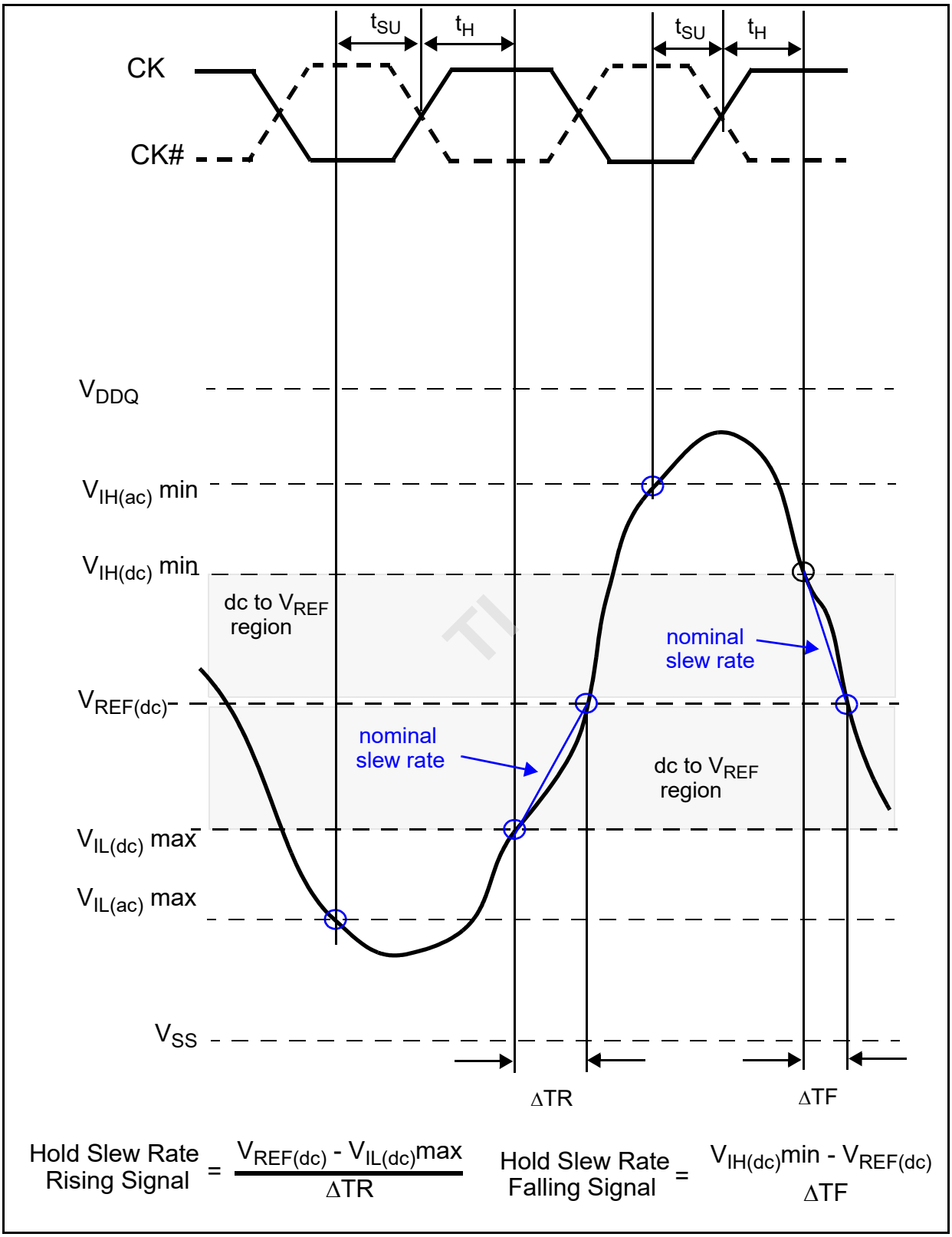



**Figure 24 — Voltage Waveforms for Setup and Hold Times – Hold Time Calculation**

**2.13 Timing Requirements (cont'd)**

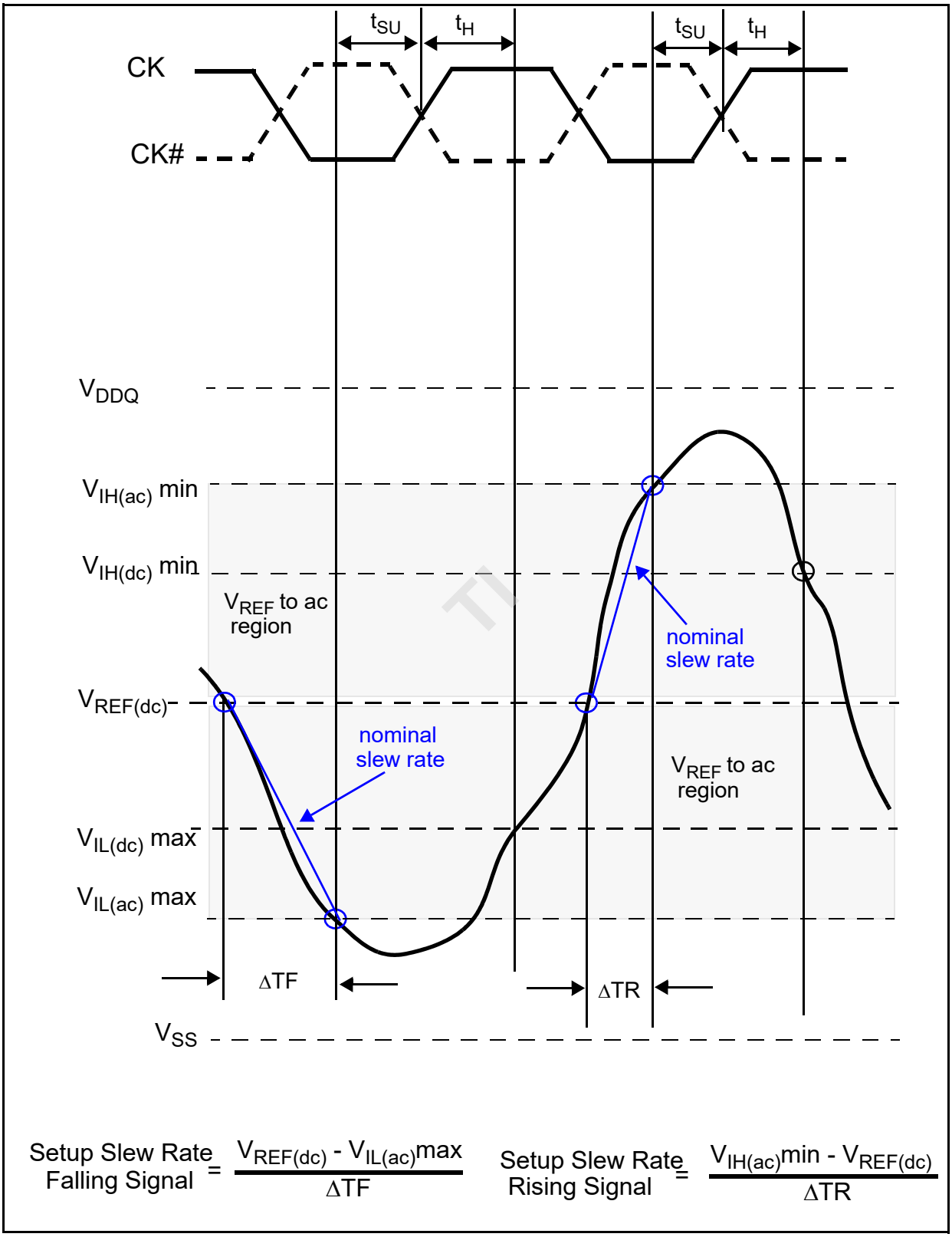



**Figure 25 — Voltage Waveforms for Setup and Hold Times – Setup Time Calculation**

## 2.14 AC Specifications

**Table 39 — Output Timing Requirements (see Clause 3.1)[1]**

| Symbol | Parameter | Conditions | DDR3/DDR3L-800/1066/1333 | | DDR3/DDR3L-1600 | | DDR3-1866 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{PDM}$ | Propagation delay, single-bit switching (1.5 V Operation) | CK/CK# to output[2] | 0.65 | 1.0 | 0.65 | 1.0 | 0.65 | 1.0 | ns |
| | Propagation delay, single-bit switching (1.35 V Operation)[3] | | 0.65 | 1.2 | 0.65 | 1.2 | - | - | ns |
| $t_{DIS}$ | Output disable time (1/2-Clock pre-launch) | Yn/Yn# to output float[4] | 0.5 + tQSK1(min) | - | 0.5 + tQSK1(min) | - | 0.5 + tQSK1(min) | - | ps |
| | Output disable time (3/4-Clock pre-launch) | | 0.25 + tQSK2(min) | - | 0.25 + tQSK2(min) | - | 0.25 + tQSK2(min) | - | ps |
| $t_{EN}$ | Output enable time (1/2-Clock pre-launch) | Output driving to Yn/Yn# | 0.5 - tQSK1(max) | - | 0.5 - tQSK1(max) | - | 0.5 - tQSK1(max) | - | ps |
| | Output enable time (3/4-Clock pre-launch) | | 0.75 - tQSK2(max) | - | 0.75 - tQSK2(max) | - | 0.75 - tQSK2(max) | - | ps |

NOTE 1 See diagram (Figure 33, "Qn and Yn Load Circuit for Propagation Delay and Slew Measurement")
NOTE 2 See diagram (Figure 26, "Propagation Delay Timing")
NOTE 3 tPDM range (tPDM_max - tPDM_min) must remain as 350 ps. For example, if tPDM_min for a device is 0.65 ns, its tPDM_max cannot be more than 1.0 ns. If tPDM_max for a device is 1.2 ns, its tPDM_min cannot be less than 0.85 ns.
NOTE 4 See diagram (Figure 35, "Voltage Waveforms Address Floating")

**Table 40 — Output Timing Requirements (DDR3U 1.25 V) (see Clause 3.1)[1]**

| Symbol | Parameter | Conditions | DDR3U-800/1066 | | DDR3U-1333/1600 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{PDM}$ | Propagation delay, single-bit switching (1.25 V Operation) | CK/CK# to output[2] | 0.65 | 1.35 | 0.65 | 1.35 | ns |
| $t_{DIS}$ | Output disable time (1/2-Clock pre-launch) | Yn/Yn# to output float[3] | 0.5 + tQSK1(min) | - | 0.5 + tQSK1(min) | - | ps |
| $t_{EN}$ | Output enable time (1/2-Clock pre-launch) | Output driving to Yn/Yn# | 0.5 - tQSK1(max) | - | 0.5 - tQSK1(max) | - | ps |

NOTE 1 See diagram (Figure 33, "Qn and Yn Load Circuit for Propagation Delay and Slew Measurement")
NOTE 2 See diagram (Figure 26, "Propagation Delay Timing")
NOTE 3 See diagram (Figure 35, "Voltage Waveforms Address Floating")

## 2.14 AC Specifications (cont'd)

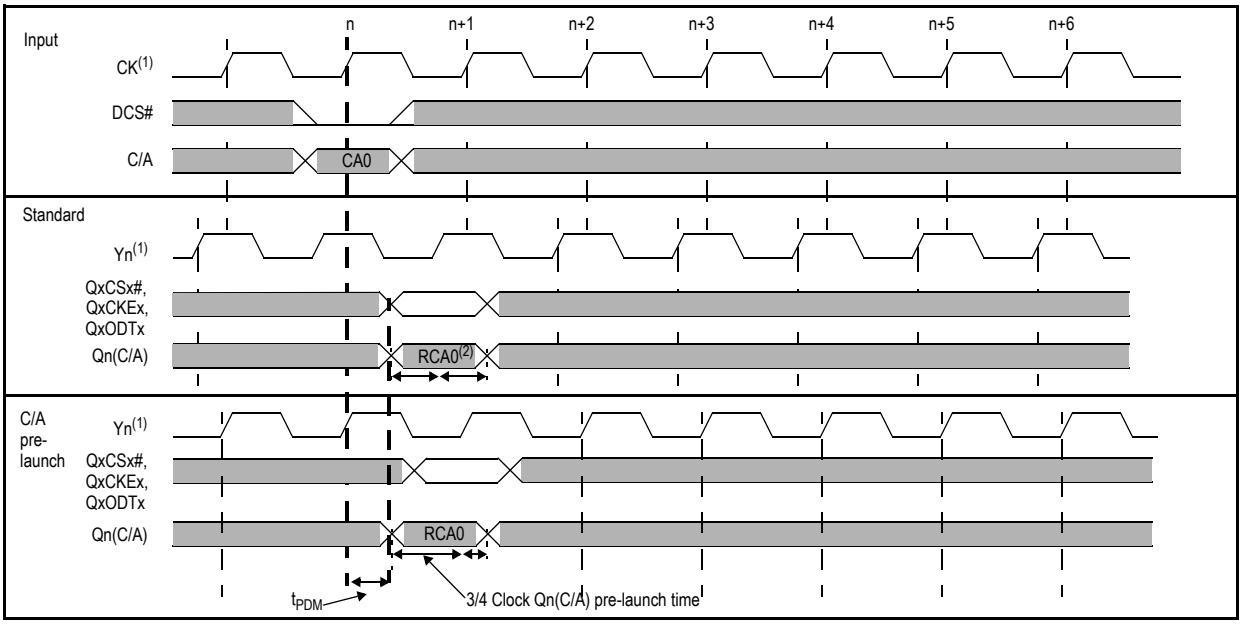



**Figure 26 — Propagation Delay Timing**

NOTE (1) CK# and Yn# left out for better visibility
NOTE (2) RCA0 is re-driven command address signal based on input CA0

## 2.15 Output Buffer Characteristics

**Table 41 — Output Edge Rates Over Specified Operating Free-air Temperature Range**

| Symbol | Parameter | Conditions | DDR3/DDR3L 800/1066/1333 | | DDR3/DDR3L 1600 | | DDR3-1866 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| dV/dt_r | rising edge slew rate[1] **(1.5 V Operation)** | | 2.0 | 7.0 | 2.0 | 5.5 | 2.0 | 5.0 | V/ns |
| | rising edge slew rate[1] **(1.35 V Operation)** | | 1.8 | 5.0 | 1.8 | 5.0 | - | - | V/ns |
| dV/dt_f | falling edge slew rate[1] **(1.5 V Operation)** | | 2.0 | 7.0 | 2.0 | 5.5 | 2.0 | 5.0 | V/ns |
| | falling edge slew rate[1] **(1.35 V Operation)** | | 1.8 | 5.0 | 1.8 | 5.0 | - | - | V/ns |
| dV/dt_D[2] | absolute difference between dV/dt_r and dV/dt_f1 | | - | 1 | - | 1 | - | 1 | V/ns |

NOTE 1 Measured into test load at default register setting except for RC3, RC4 and RC5 which are set according to the driver strength to be measured.
NOTE 2 Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate)

**Table 42 — Output Edge Rates Over Specified Operating Free-air Temperature Range (DDR3U 1.25 V)**

| Symbol | Parameter | Conditions | DDR3U-800/1066 | | DDR3U-1333/1600 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| dV/dt_r | rising edge slew rate[1] **(1.25 V Operation)** | | TBD | TBD | TBD | TBD | V/ns |
| dV/dt_f[1] | falling edge slew rate[1] **(1.25 V Operation)** | | TBD | TBD | TBD | TBD | V/ns |
| dV/dt_D[2] | absolute difference between dV/dt_r and dV/dt_f[1] | | - | 1 | - | 1 | V/ns |

NOTE 1 Measured into test load at default register setting except for RC3, RC4 and RC5 which are set according to the drive strength to be measured
NOTE 2 Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate)

## 2.16 Input Buffer Characteristics

**Table 43 — Input IBT Characteristics over Specified Operating Free-air Temperature Range**

| Symbol | Parameter | Conditions | DDR3/DDR3L/DDR3U-800/1066/1333/1600 | | DDR3 1866 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $R_{IBT(tol)}$ | Total Effective IBT Value Tolerance [1], 2 | | -10 | 10 | -10 | 10 | % |
| **ΔVM** | Deviation of VM w.r.t. VDD/2 3 | DA[15:0], DBA[2:0], DCKE[1:0], DODT[1:0], DRAS#, DCAS#, DWE#, PAR_IN, DCS[n:0]# | - | 2.5 | - | 2.5 | % |

NOTE 1 Example for 100 ohm, Min = 90 ohm, Max = 110 ohm

2 Apply VIH(AC) to pin under test and measure current IIH(AC), then apply VIL(AC) to pin under test and measure current IIL(AC). RIBT = (VIH(AC) - VIL(AC))/(IIH(AC) - IIL(AC))

3 Measure voltage (VOUT = VM) at test pin with no load (IOUT = 0). DVM = |2 *VM/VDD - 1| * 100%

4 n=1 for QuadCS disabled, n=3 for QuadCS enabled

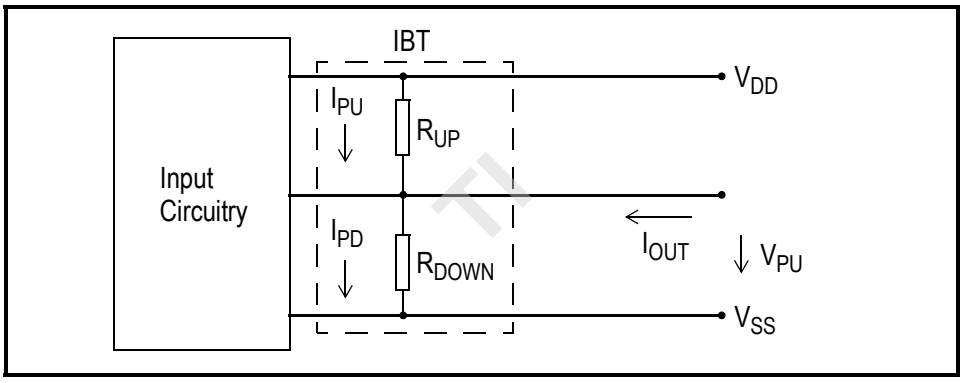



**Figure 27 — Input Bus Termination: Definition of Voltages and Currents**

## 2.17 Clock Driver Characteristics

**Table 44 — Clock Driver Characteristics at Application Frequency (Frequency Band 1)**

| Symbol | Parameter | Conditions | DDR3/DDR3L-800 | | DDR3/DDR3L-1066 | | DDR3/DDR3L-1333 | | DDR3/DDR3L-1600 | | DDR3-1866 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{jit}(cc+)$ | Cycle-to-cycle period jitter | | 0 | 40 | 0 | 40 | 0 | 40 | 0 | 30 | 0 | 25 | ps |
| $t_{jit}(cc-)$ | Cycle-to-cycle period jitter | | 0 | 40 | 0 | 40 | 0 | 40 | 0 | 30 | 0 | 25 | ps |
| $t_{STAB}$ | Stabilization time | | - | 6 | - | 6 | - | 6 | - | 6 | - | 5 | µs |
| $t_{fdyn}$ | Dynamic phase offset | | -50 | 50 | -50 | 50 | -50 | 50 | -40 | 40 | -30 | 30 | ps |
| $t_{CKsk}$ | Fractional Clock Output skew[1] | | - | 15 | - | 15 | - | 15 | - | 10 | - | 10 | ps |
| $t_{jit}(per)$ | Yn Clock Period jitter | | -40 | 40 | -40 | 40 | -40 | 40 | -30 | 30 | -25 | 25 | ps |
| $t_{jit}(hper)$ | Half period jitter | | -50 | 50 | -50 | 50 | -50 | 50 | -40 | 40 | -35 | 35 | ps |
| tPWH/PWL | Yn pulse width HIGH/LOW duration[2] | tPW = 1/2tCK - \|tjit(hper)min\| to 1/2tCK + \|tjit(hper)max\| | 1.200 | 1.300 | 0.888 | 0.988 | 0.700 | 0.800 | 0.585 | 0.665 | 0.501 | 0.571 | ns |
| $t_{Qsk1}$[3] | Qn Output to **Yn** clock tolerance (Standard 1/2-Clock Pre-Launch) | Output Inversion enabled | -150 | 250 | -150 | 250 | -150 | 250 | -140 | 140 | -135 | 125 | ps |
| | | Output Inversion disabled | -150 | 350 | -150 | 350 | -150 | 350 | -140 | 240 | -135 | 225 | |
| $t_{Qsk2}$[4] | **Qn Output to Yn** clock tolerance (3/4 Clock Pre-Launch) | Output Inversion enabled | -150 | 250 | -150 | 250 | -150 | 250 | -140 | 140 | -135 | 125 | ps |
| | | Output Inversion disabled | -150 | 350 | -150 | 350 | -150 | 350 | -140 | 240 | -135 | 225 | |
| $t_{staoff}$ | Average delay through the register between the input clock and output clock[5]. **(1.5 V Operation)** | Standard 1/2-Clock Pre-Launch $t_{staoff} = t_{PDM} + 1/2$ tCK | 1.90 | 2.25 | 1.59 | 1.94 | 1.40 | 1.75 | 1.28 | 1.63 | 1.19 | 1.54 | ns |
| | | 3/4 Clock Pre-Launch $t_{staoff} = t_{PDM} + 3/4$ tCK | 2.53 | 2.88 | 2.06 | 2.41 | 1.77 | 2.12 | 1.59 | 1.94 | 1.45 | 1.80 | ns |
| | Average delay through the register between the input clock and output clock[5]. **(1.35 V Operation)** | Standard 1/2-Clock Pre-Launch $t_{staoff} = t_{PDM} + 1/2$ tCK | 1.90 | 2.45 | 1.59 | 2.14 | 1.40 | 1.95 | 1.28 | 1.83 | - | - | ns |
| | | 3/4 Clock Pre-Launch $t_{staoff} = t_{PDM} + 3/4$ tCK | 2.53 | 3.08 | 2.06 | 2.61 | 1.77 | 2.32 | 1.59 | 2.14 | - | - | ns |
| $t_{dynoff}$[6] | Maximum variation in delay between the input and output clock | | - | 160 | - | 130 | - | 110 | - | 90 | - | 70 | ps |
| The PLL in the SSTE32882 must be capable of meeting all the above test parameters while supporting SSC synthesizers with the following parameters: | | | | | | | | | | | | | |
| | SSC modulation frequency | | 30 | 33 | 30 | 33 | 30 | 33 | 30 | 33 | 30 | 33 | kHz |
| | SSC clock input frequency deviation | | 0.00 | -0.5 | 0.00 | -0.5 | 0.00 | -0.5 | 0.00 | -0.5 | 0.00 | -0.5 | % |
| SSTE32882 PLL designs should target the values below to improve tracking between CK/CK# and Yn/Yn#: | | | | | | | | | | | | | |
| $t_{band}$ | PLL Loop bandwidth (-3 dB from unity gain) | | 25[7] | - | 30<Addt'l Footnote>g | - | 35<Addt'l Footnote>g | - | 40<Addt'l Footnote>g | - | 45<Addt'l Footnote>g | - | Mhz |

## 2.17 Clock Driver Characteristics

**Table 44 — Clock Driver Characteristics at Application Frequency (Frequency Band 1) (cont'd)**

| Symbol | Parameter | Conditions | DDR3/DDR3L-800 | DDR3/DDR3L-1066 | DDR3/DDR3L-1333 | DDR3/DDR3L-1600 | DDR3-1866 | Unit |
|---|---|---|---|---|---|---|---|---|
| NOTE 1 | This skew represents the absolute output clock skew and contains the pad skew and package skew (See Figure 29, "Clock Output (Yn) Skew"). This parameter is specified for the clock pairs on each side of the register independently. The skew is applicable to right side clock pairs between Y0/Y0# and Y2/Y2#, as well as left side of the clock pairs between Y1/Y1# and Y3/Y3#. This is not a tested parameter and has to be considered as a design goal only. | | | | | | | |
| NOTE 2 | This parameter is a measure of the output clock pulse width HIGH/LOW. The output clock duty cycle can be calculated based on tPW. | | | | | | | |
| NOTE 3 | This skew represents the cumulative of instantaneous Qn skew compared to the output clock (Yn), and contains the register pad skew, clock skew, package routing skew and the output clock jitter (See Figure 30, "Qn Output Skew for Standard 1/2-Clock Pre-Launch"). This parameter applies to each side of the register independently. The parameter includes the skew related to simultaneous switching noise (SSO). The Qn output can either be early or late. For outputs QxA0 .. QxA15, QxBA0 .. QxBA2, QxRAS#, QxCAS#, QxWE#, QCKE0, QCKE1, QODT0, QODT1 this parameter applies to each side of the register independently. If QCSEN# is HIGH then also for outputs QxCS0# and QxCS1# this parameter applies to each side of the register independently. If QCSEN# is LOW then this parameter applies to any combination of clocks Y0/Y0# .. Y3/Y3# and QCS[3:0]#. The parameter is measured per JEPXX-XX (procedure defined by Validation TG.) | | | | | | | |
| NOTE 4 | This skew represents the cumulative of instantaneous Qn skew compared to the output clock (Yn), and contains the register pad skew, clock skew, package routing skew, and the output clock jitter. (See Figure 31, "Qn Output Skew for 3/4-Clock Pre-Launch"). This parameter applies to each side of the register independently. The parameter includes the skew related to simultaneous switching noise (SSO). The Qn output can either be early or late. For outputs QxA0 .. QxA15, QxBA0 .. QxBA2, QxRAS#, QxCAS#, QxWE#, QCKE0, QCKE1, QODT0, QODT1 this parameter applies to each side of the register independently. If QCSEN# is HIGH then also for outputs QxCS0# and QxCS1# this parameter applies to each side of the register independently. If QCSEN# is LOW then this parameter applies to any combination of clocks Y0/Y0# .. Y3/Y3# and QCS[3:0]#. The parameter is measured per JEPXX-XX (procedure defined by Validation TG. This parameter maybe omitted in vendor's datasheet if 3/4 Pre-Launch is not supported in RC2 | | | | | | | |
| NOTE 5 | This parameter measures the delay from the rising differential input clock which samples incoming C/A to the rising differential output clock that will be used to sample the same C/A data. tstaoff may vary by the amount of tdynoff based on voltage and temperature drift as well as tracking error and jitter. Including this variation tstaoff may not exceed the limits set by $t_{staoff}$(min) and $t_{staoff}$(max) | | | | | | | |
| NOTE 6 | See Figure 28, "Definition for tstaoff and tdynoff" | | | | | | | |
| NOTE 7 | Implies a -3 dB bandwidth and jitter peaking of 3 dB. | | | | | | | |

## 2.17 Clock Driver Characteristics (cont'd)

**Table 45 — Clock Driver Characteristics at Application Frequency (Frequency Band 1) (DDR3U 1.25 V)**

| Symbol | Parameter | Conditions | DDR3U-800 | | DDR3U-1066 | | DDR3U-1333 | | DDR3U-1600 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{jit}(cc+)$ | Cycle-to-cycle period jitter | | 0 | 40 | 0 | 40 | 0 | 40 | 0 | 30 | ps |
| $t_{jit}(cc-)$ | Cycle-to-cycle period jitter | | 0 | 40 | 0 | 40 | 0 | 40 | 0 | 30 | ps |
| $t_{STAB}$ | Stabilization time | | - | 6 | - | 6 | - | 6 | - | 6 | µs |
| $t_{fdyn}$ | Dynamic phase offset | | -50 | 50 | -50 | 50 | -50 | 50 | -40 | 40 | ps |
| $t_{CKsk}$ | Fractional Clock Output skew[1] | | - | 15 | - | 15 | - | 15 | - | 10 | ps |
| $t_{jit}(per)$ | Yn Clock Period jitter | | -40 | 40 | -40 | 40 | -40 | 40 | -30 | 30 | ps |
| $t_{jit}(hper)$ | Half period jitter | | -50 | 50 | -50 | 50 | -50 | 50 | -40 | 40 | ps |
| tPWH/PWL | Yn pulse width HIGH/LOW duration[2] | tPW = 1/2tCK - \|tjit(hper)min\| to 1/2tCK + \|tjit(hper)max\| | 1.200 | 1.300 | 0.888 | 0.988 | 0.700 | 0.800 | 0.585 | 0.665 | ns |
| $t_{Qsk1}$[3] | Qn Output to **Yn** clock tolerance (Standard 1/2-Clock Pre-Launch) | Output Inversion enabled | -100 | 200 | -100 | 200 | -100 | 200 | -100 | 100 | ps |
| | | Output Inversion disabled | -100 | 300 | -100 | 300 | -100 | 300 | -100 | 200 | |
| $t_{staoff}$ | Average delay through the register between the input clock and output clock[4]. **(1.25 V Operation)** | Standard 1/2-Clock Pre-Launch $t_{staoff} = t_{PDM} + 1/2$ tCK | 1.90 | 2.60 | 1.59 | 2.29 | 1.40 | 2.10 | 1.28 | 1.98 | ns |
| $t_{dynoff}$[5] | Maximum variation in delay between the input and output clock | | - | 160 | - | 130 | - | 110 | - | 90 | ps |
| The PLL in the SSTE32882 must be capable of meeting all the above test parameters while supporting SSC synthesizers with the following parameters: | | | | | | | | | | | |
| | SSC modulation frequency | | 30 | 33 | 30 | 33 | 30 | 33 | 30 | 33 | kHz |
| | SSC clock input frequency deviation | | 0.00 | -0.5 | 0.00 | -0.5 | 0.00 | -0.5 | 0.00 | -0.5 | % |
| SSTE32882 PLL designs should target the values below to improve tracking between CK/CK# and Yn/Yn#: | | | | | | | | | | | |
| $t_{band}$ | PLL Loop bandwidth (-3 dB from unity gain) | | 25[6] | - | 30[1] | - | 35[1] | - | 40[1] | - | Mhz |

NOTE 1 This skew represents the absolute output clock skew and contains the pad skew and package skew (See Figure 29, "Clock Output (Yn) Skew"). This parameter is specified for the clock pairs on each side of the register independently. The skew is applicable to right side clock pairs between Y0/Y0# and Y2/Y2#, as well as left side of the clock pairs between Y1/Y1# and Y3/Y3#. This is not a tested parameter and has to be considered as a design goal only.

NOTE 2 This parameter is a measure of the output clock pulse width HIGH/LOW. The output clock duty cycle can be calculated based on tPW.

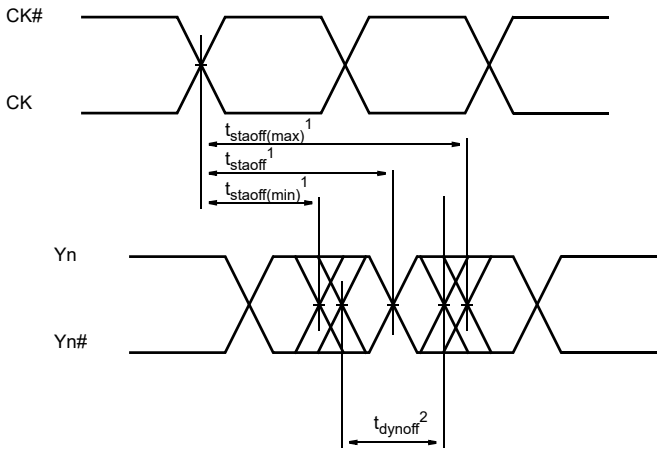
NOTE 3 This skew represents the absolute Qn skew compared to the output clock **(Yn)**, and contains the register pad skew, clock skew and package routing skew (See Figure 30, "Qn Output Skew for Standard 1/2-Clock Pre-Launch"). The output clock jitter is not included in this skew. This parameter applies to each side of the register independently. The parameter includes the skew related to simultaneous switching noise (SSO). The Qn output can either be early or late.

NOTE 4 This parameter measures the delay from the rising differential input clock which samples incoming C/A to the rising differential output clock that will be used to sample the same C/A data. $t_{staoff}$ may vary by the amount of $t_{dynoff}$ based on voltage and temperature drift as well as tracking error and jitter. Including this variation $t_{staoff}$ may not exceed the limits set by $t_{staoff(min)}$ and $t_{staoff(max)}$

NOTE 5 See Figure 28, "Definition for tstaoff and tdynoff"

NOTE 6 Implies a -3 dB bandwidth and jitter peaking of 3 dB.

## 2.17 Clock Driver Characteristics (cont'd)




1. $t_{staoff}$ = propagation delay for clock signal (rising CK input clock edge to rising Yn output clock edge).

2. $t_{dynoff}$ = maximum $t_{staoff}$ variation over voltage and temperature.
This includes all sources of jitter and drift (e.g.Thermal noise, supply noise, voltage/temperature drift, SSC tracking, SSO, etc) except reference clock noise.

**Figure 28 — Definition for $t_{staoff}$ and $t_{dynoff}$**

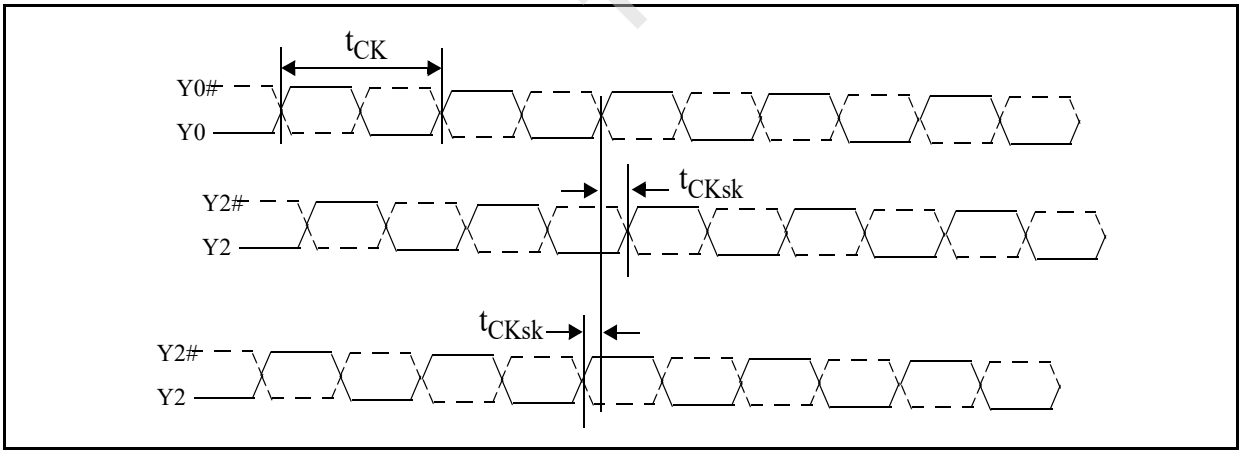



**Figure 29 — Clock Output (Yn) Skew**

## 2.17 Clock Driver Characteristics (cont'd)

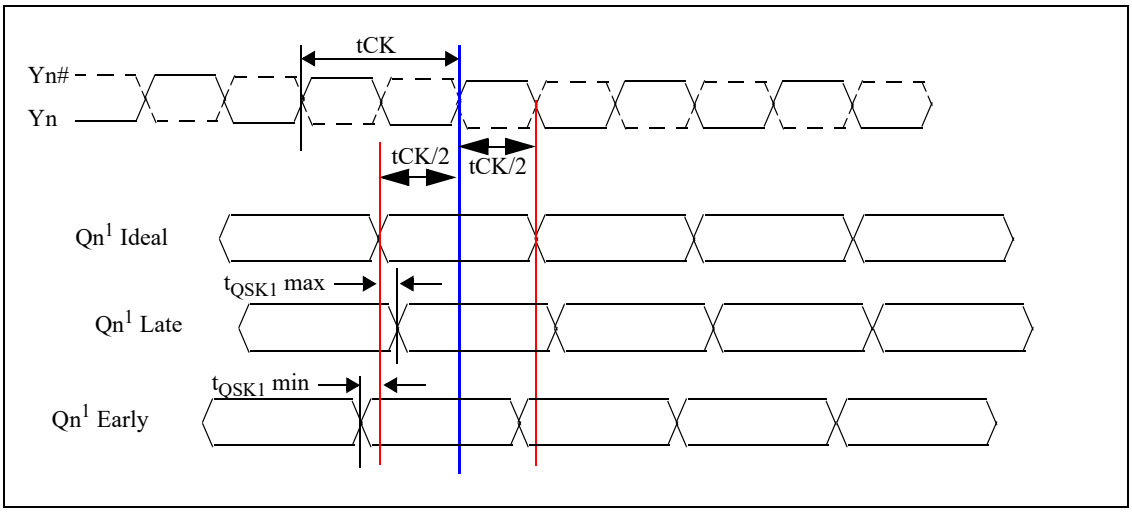



**Figure 30 — Qn Output Skew for Standard 1/2-Clock Pre-Launch**

NOTE 1 Outputs as specified in Figure 2.17, "Clock Driver Characteristics" Footnote c

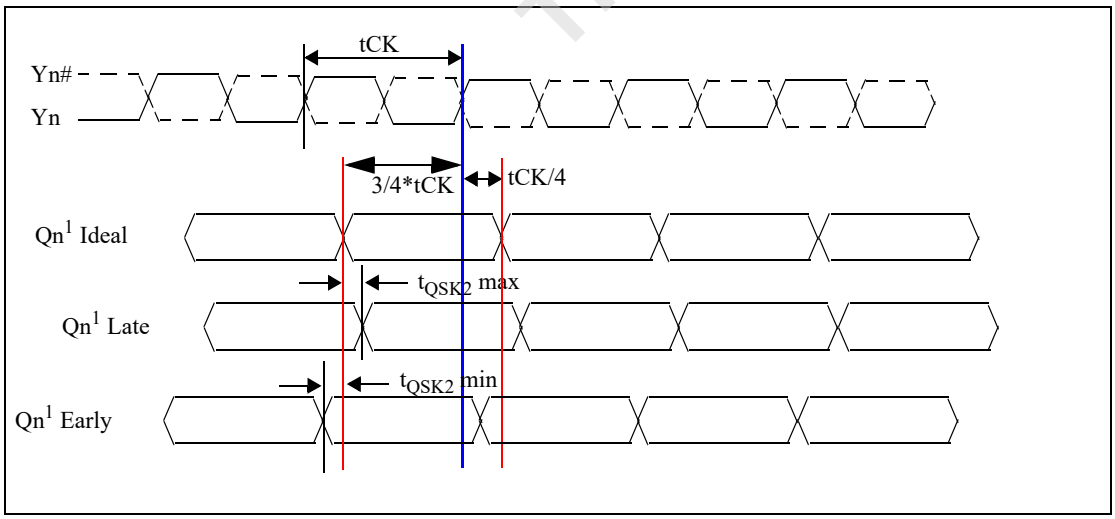



**Figure 31 — Qn Output Skew for 3/4-Clock Pre-Launch**

NOTE 1 Outputs as specified in Table 44, "Clock Driver Characteristics at Application Frequency (Frequency Band 1)", NOTE 4.

## 2.17 Clock Driver Characteristics (cont'd)

**Table 46 — Clock Driver Characteristics at Test Frequency (Frequency Band 2)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{jit}(cc)$ | Cycle-to-cycle period jitter | | 0 | 160 | ps |
| $t_{STAB}$ | Stabilization time | | - | 15 | µs |
| $t_{CKsk}$ | Total Clock Output Skew [1] | | | 100 | ps |
| | Fractional Clock Output skew [2] | | | vs[3] | ps |
| tjit(per) | Yn Clock Period jitter | | -160 | 160 | ps |
| tjit(hper) | Half period jitter | | -200 | 200 | ps |
| $t_{Qsk1}$[4] | Qn Output to clock tolerance (Standard 1/2-Clock Pre-Launch) | Output Inversion enabled | -100 | vs<Addt'l Footnote >c | ps |
| | | Output Inversion disabled | -100 | vs<Addt'l Footnote >c | |
| $t_{Qsk2}$[5] | Output clock tolerance (3/4 Clock Pre-Launch) | Output Inversion enabled | -100 | vs<Addt'l Footnote >c | ps |
| | | Output Inversion disabled | -100 | vs<Addt'l Footnote >c | |
| $t_{dynoff}$ | Maximum re-driven dynamic clock offset [6] | | -500 | 500 | ps |

NOTE 1 This skew represents the absolute output clock skew and contains the pad skew and package skew.

NOTE 2 This skew represents the absolute output clock skew and contains the pad skew and package skew (See Figure 29, "Clock Output (Yn) Skew")

NOTE 3 Vendor Specific

NOTE 4 This skew represents the absolute Qn skew compared to the output clock **(Yn)**, and contains the register pad skew, clock skew and package routing skew (See Figure 30, "Qn Output Skew for Standard 1/2-Clock Pre-Launch"). The output clock jitter is not included in this skew. This parameter applies to each side of the register independently. The parameter includes the skew related to simultaneous switching noise (SSO). The Qn output can either be early or late.

NOTE 5 This skew represents the absolute Qn skew compared to the output clock **(Yn)**, and contains the register pad skew, clock skew and package routing skew (See Figure 31, "Qn Output Skew for 3/4-Clock Pre-Launch"). The output clock jitter is not included in this skew. This parameter applies to each side of the register independently. The parameter includes the skew related to simultaneous switching noise (SSO). The Qn output can either be early or late.

NOTE 6 The re-driven clock signal is ideally centered in the address/control signal eye. This parameter describes the dynamic deviation from this ideal position including jitter and dynamic phase offset.

# 3 Test Circuits and Switching Waveforms

## 3.1 Parameter Measurement Information

All input pulses are supplied by generators having the following characteristics: 300 MHz ≤ PRR ≤ 945 MHz; $Z_o$ = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified.

The outputs are measured one at a time with one transition per measurement.

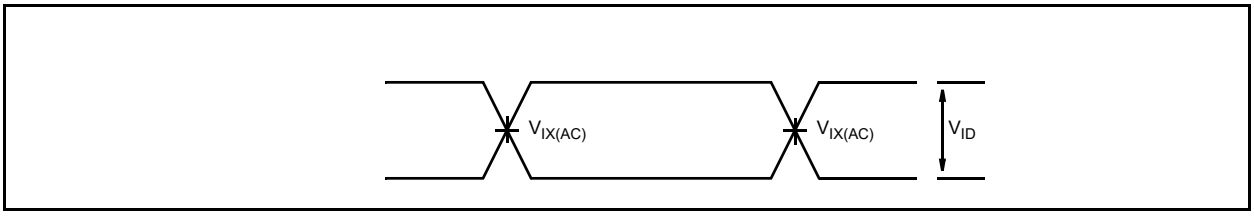



**Figure 32 — Voltage Waveforms; Input Clock**

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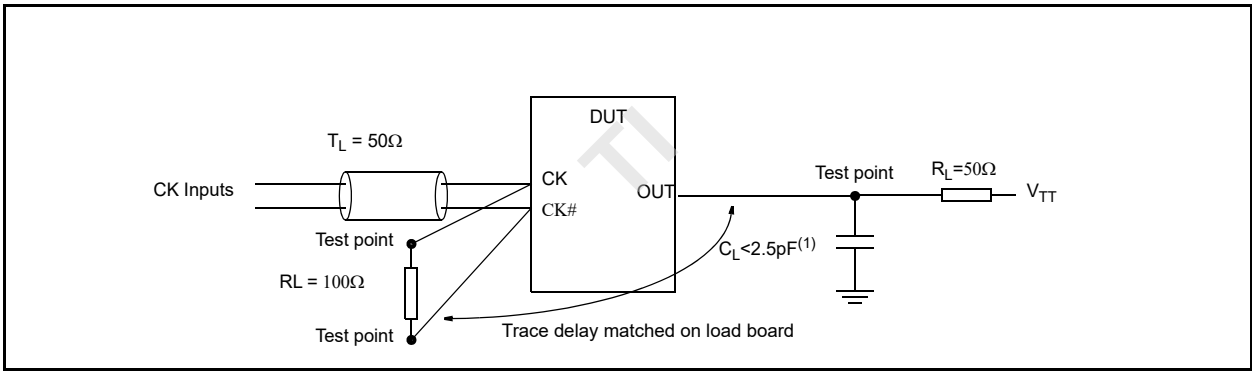


**Figure 33 — Qn and Yn Load Circuit for Propagation Delay and Slew Measurement**

NOTE (1) $C_L$ is parasitic (probe and jig capacitance)

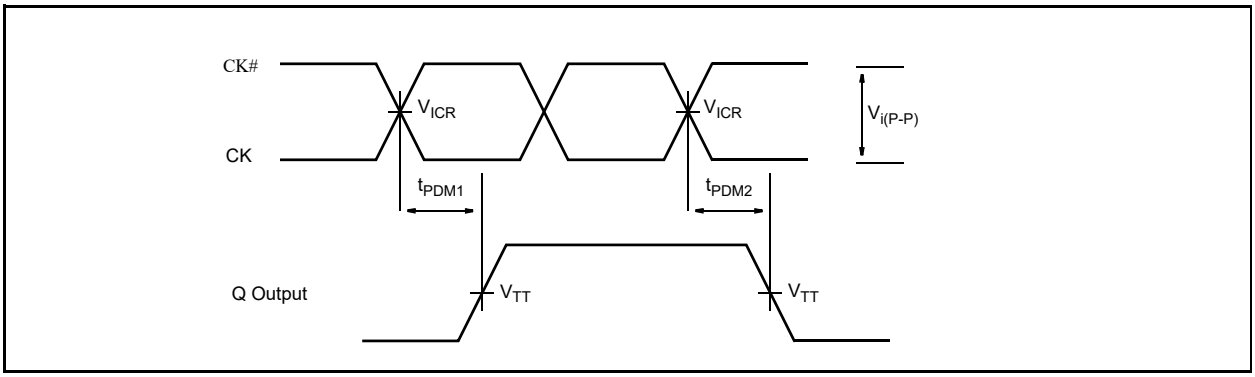


**Figure 34 — Voltage Waveforms; Propagation Delay Times**

NOTE 1 VTT = VDD/2

NOTE 2 VICR Cross Point Voltage

NOTE 3 Vi(P-P) = 500 mV (1.5 V Operation), 450 mV (1.35 V Operation) or 400 mV (1.25 V Operation).

NOTE 4 tPDM1, tPDM2 the larger number of both has to be taken when performing tPDM max measurement, the smaller number of both has to be taken when performing tPDM min measurement

## 3.1 Parameter Measurement Information (cont'd)

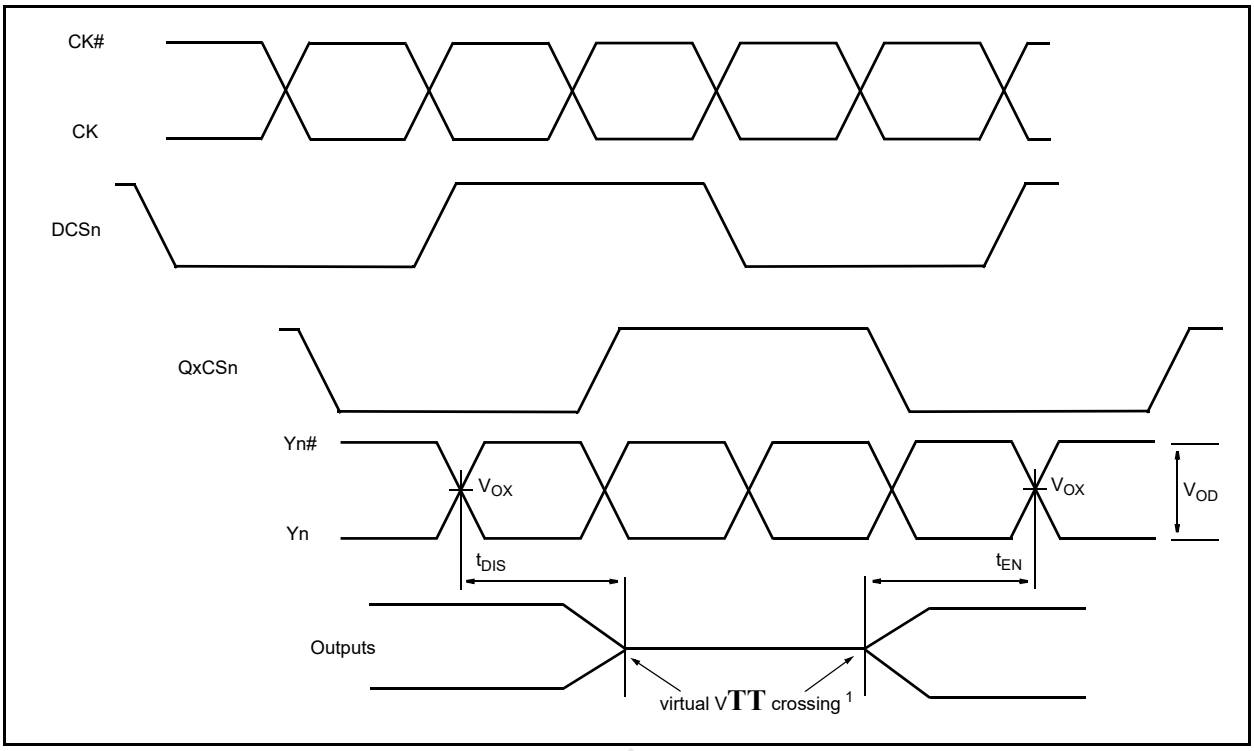


**Figure 35 — Voltage Waveforms Address Floating**

NOTE 1 See Figure 36, "Calculating the Virtual VTT Crossing Point"

.Enabling and disabling the CA outputs must not violate DRAM setup and hold time requirements. Therefore a tDIS transition may not occur earlier than the earliest (HL/LH) transition and a tEN transition may not occur later than the latest (HL/LH) transition. Regular transitions are measured between CK/CK# and CA/VTT crossings however a VTT crossing is not available in the state where the outputs are Hi-Z. To allow a correct and not overly conservative measurement a virtual VTT crossing point is defined below. The calculation of the virtual VTT crossing point is shown in Figure 31. The voltage levels for yxa and yxb are measured from VTT (VDD/2) and should be selected such that the region between t1 and t2 covers a linear range and represents a typical slope of the waveform within the transition area. They have to be used signed in the formula.

## 3.1 Parameter Measurement Information (cont'd)

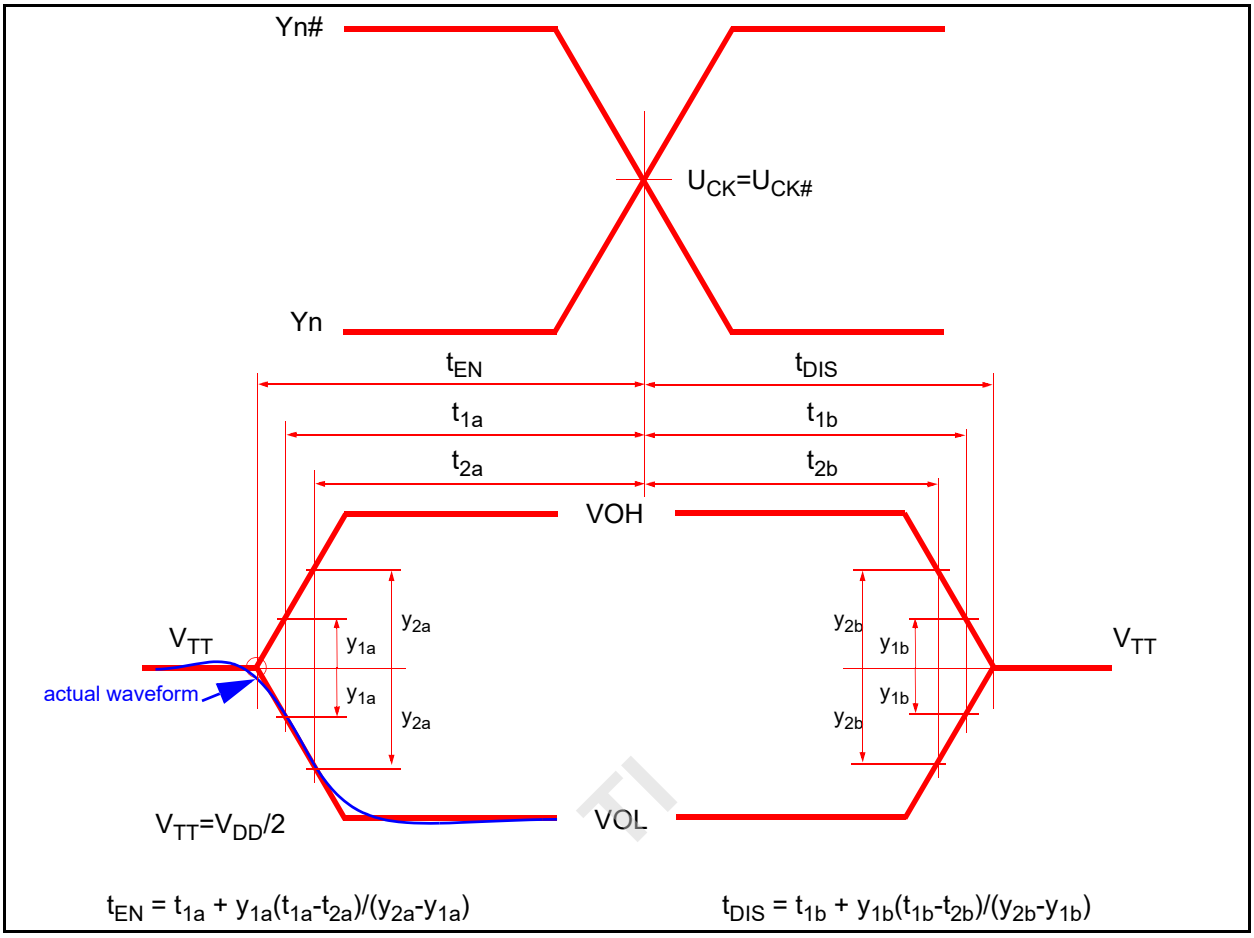


**Figure 36 — Calculating the Virtual VTT Crossing Point**

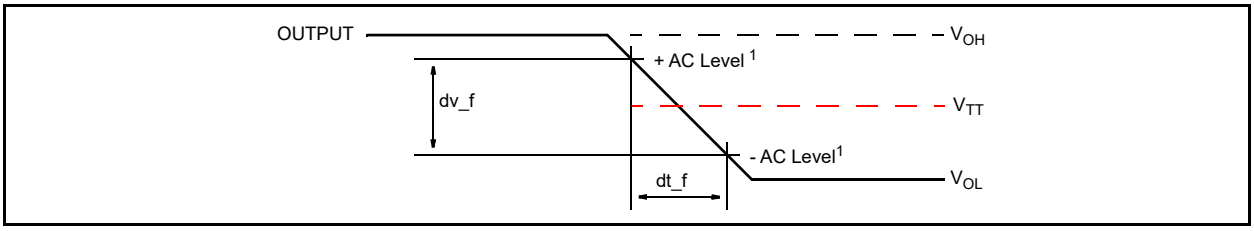


**Figure 37 — Voltage Waveforms, HIGH-to-LOW Slew Rate Measurement**

NOTE 1 See Table 41

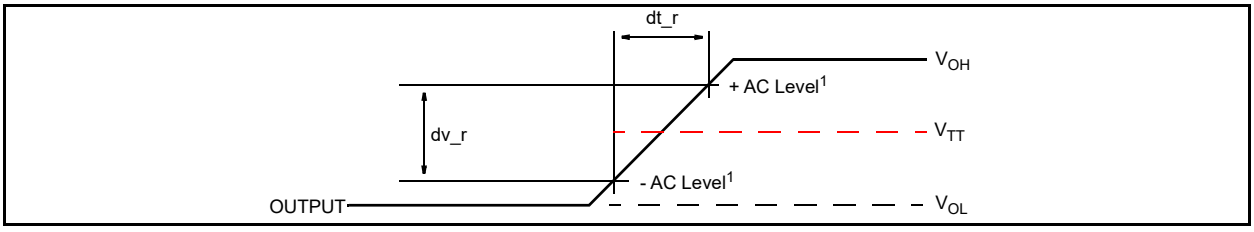


**Figure 38 — Voltage Waveforms, LOW-to-HIGH Slew Rate Measurement**

NOTE 1 See Table 41

## 3.1 Parameter Measurement Information (cont'd)

**Table 47 — AC Level for Slew Rate Measurement**

| | DDR3/DDR3L-800/1066/1333/1600 | **DDR3-1866** |
|---|---|---|
| AC Level (1.5 V) | 150 mV | 135 mV |
| AC Level (1.35 V) | 135 mV | |

**Table 48 — AC Level for Slew Rate Measurement (DDR3U 1.25 V)**

| | **DDR3U-800/1066/1333/1600** |
|---|---|
| AC Level (1.25 V) | 125 mV |

## 3.2 Error Output Load Circuit and Voltage Measurement Information

All input pulses are supplied by generators having the following characteristics: 300 MHz ≤ PRR ≤ 945 MHz; $Z_o$ = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified.

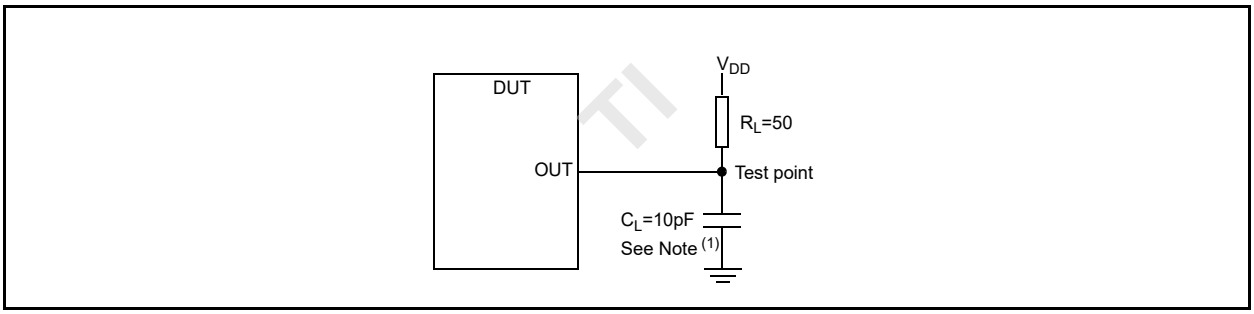


**Figure 39 — Load Circuit, ERROUT# Outputs**

NOTE (1) $C_L$ includes probe and jig capacitance.

Output driver characteristics are separately controlled for outputs that are often loaded with twice as many DRAMs as the other outputs. Outputs are grouped as follows:

1. CA Signals =QxA0-QxAn, QxBA0-QxBAn, QxRAS#, QxCAS#, QxWE#
2. Control Signals = QxCSn#, QxCKEn, QxODTn
3. CK = Yn .. Yn#

## 4 Recommended Filtering for the Analog Power Supply (AVDD)

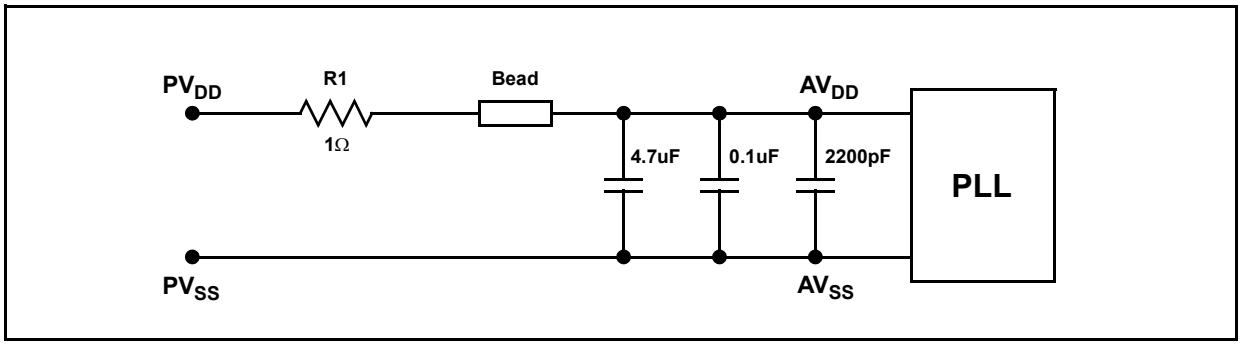


**Figure 40 — AVDD Filtering**

1. Place the 2200 pF capacitor close to the PLL
2. Use a wide trace for the PLL analog power and ground. Connect PLL and caps to AGND trace and connect trace to one GND via (farthest from PLL).
3. Bead: 0.8 ohm DC max, 600 ohms @ 100 MHz

## 5 Feedback Loop Topology for Registers with External Feedback

The SSTE32882 registering clock driver feedback path provides, when used by the device, compensation for drift caused by voltage and temperature effects. The flight time of the unloaded trace from FBOUT to FBIN must be 95 ± 15 ps to assure proper operation.

Figure 41, “External Feedback Loop” shows a topology proposal with the corresponding mechanical and electrical dimensions as per Table 49. Both figure and table are for reference only. Actual values may vary according to application requirements. The overall loop length in this example is in the range of 15 mm which fits a typical DIMM stack-up The feedback loop does not affect post-register timing. It influences the phase relationship between pre- and post-register signaling. The register manufacturer guarantees the specified propagation delay if the user follows the feedback loop topology proposal in this paragraph.

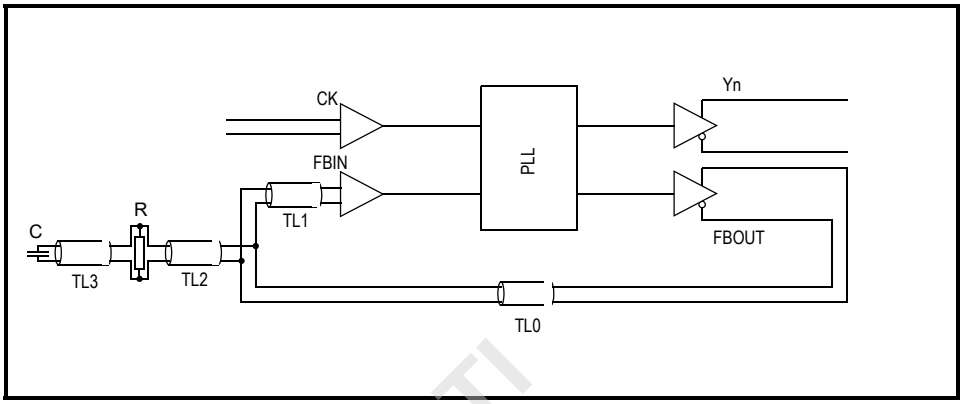


**Figure 41 — External Feedback Loop**

**Table 49 — Feedback Loop Mechanical Dimensions**

| TL0 | | TL1 | TL2 | TL3 | R | C |
|---|---|---|---|---|---|---|
| Min | Max | | | | | |
| 12.4 | 12.6 | 2.5 | 0.6 | 1.0 | equals $R_{TERM}$ of Yn/Yn# | 0 pF typ[1] |
| NOTE 1 Pads should be present as parasitics are part of the feedback loop. If pads are not present feedback loop length must be corrected. | | | | | | |

## 6 Reference to Other Applicable JEDEC Standards and Publications

1. JEP95, *JEDEC Registered and Standard Outlines for Solid State and Related Products.*
2. JEP104, *Reference Guide to Letter Symbols for Semiconductor Devices.*
3. JESD21-C, *Configuration for Solid State Memories.*
4. JESD8-11A, *Definition of wide range non-terminated logic*

## 7 Annex A - (Informative) Differences Between JESD82-29A and JESD29

Changes made to the document base on the December-2006 JEDEC Meeting discussions:

Page 1: Deleted all references to JC-16 SSTL_15 specification.

Page 2: Updated Initialization diagram

Page 3: Updated Initialization sequence table

Page 3: Changed footnote 2 (table 1) to specify that the QxODTn output changes only tACT after reset. Sentence now reads “After the first rising CK edge, after tACT, the state of QxODTx.....”.

Page 6: Excluded QBA0, QBA1 and QBA2 from the list of signals with output inversions.

Page 13: Deleted all references to SSTL_15

Page 17: Changed RC0[DA3] from “Reserved” to “Output Inversion” function.

Page 18: Changed RC2[DA4] from “Reserved” to 1T/3T Output Timing” function.

Page 20: Combined the drive characteristics (Table 12, 13 & 14) for 16 DRAM and 20 DRAM load to a single setting.

Page 22: Figure 14: Excluded the DA0-DA2 (and QxA0-QxA2) from the list of signals with output inversions.

Page 24: Changed “NORE 2” to NOTE 2”.

Page 30: Fixed font mismatch in notes.

Deleted RESET-to-Q timing waveform, RESET-to-ERROUT# timing waveform and CK-to-ERROUT# timing waveform.

Changes made to the document base on the March-2007 JEDEC Meeting discussions:

Page 2: Updated Initialization diagram

Page 3: Updated Initialization sequence table

Page 9: Only the DA[15:5] inputs must be driven LOW during Control Word access. The DRAS#, DCAS#, DWE#, DCKE[1:0] and DODT[1:0] inputs can be either HIGH or LOW.

Page 10: Updated Package Configuration information.

Page 20: Replaced TBD in RC3 table (Table 12) with logical values.

Page 20: Replaced TBD in RC4 table (Table 13) with logical values.

Page 21: Replaced TBD in RC5 table (Table 14) with logical values.

Page 27: Update Timing Requirements Table (Table 19) with DDR3-1600 speed bin columns.

Page 29: Update Output Timing Requirements Table (Table 20) with DDR3-1600 speed bin columns.

Page 29: Update Output Edge Rate Table (Table 21) with DDR3-1600 speed bin columns.

Page 30: Update Clock Driver Characteristics at Application Frequency Table (Table 22) with DDR3-1600 speed bin columns.

Page 32: Update Clock Driver Characteristics at Test Frequency Table (Table 23) with DDR3-1600 speed bin columns.

Changes made to the document base on the June-2007 JEDEC Meeting discussions:

Updated the entire document to include the QuadCS feature and corresponding references.

Page 2: Updated Initialization diagram with QuadCS feature.

Page 3: Updated Initialization table with QuadCS feature.

Pages 6-9: Added description for CKE Power Down Feature.

Page 12: Edited second paragraph in Control Word description to state that “at least one DCKEn input must be HIGH for valid data access”.

Page 18: Updated the MIRROR pin description by adding exclusion of turning off IBT on the DCSn# and DODTn inputs when MIRROR=HIGH.

Page 20: Updated the Function Table (Table 7) per Item 104.34.

## 7 Annex A - (Informative) Differences Between JESD82-29A and JESD29 (cont'd)

Page 26: Updated Table 11 footnote 2 description by adding exclusion of turning off IBT on the DCSn# and DODTn inputs when MIRROR=HIGH. Also update the second paragraph with the same exclusion.

Page 29: Added RC9 Control Word definition for CKE Power Down feature.

Page 35: Updated the Timing Requirement Table by adding the following parameters: tInDIS, tQDIS and tFixedoutput.

Changes made to the document base on the August-2007 JEDEC Meeting discussions:

Added ballout for MIRROR=HIGH, QCSEN#=LOW

Updated 1T and 3T (during MRS Command) timing diagrams to list which QBxx outputs are excluded from output inversion and toggle with the QAxx outputs and to include the QBxx outputs and show when inversion is enabled/disabled.

Changed min/max values for Data Inputs capacitance from 2pF/3pF to 1.5pF/2.5pF.

Changes to the parametric table according to Item # 104.38.

Changes to the Test Circuit and Switching Waveforms section according to Item # 104.36

Changes made to the document base on the November-2007 JEDEC Meeting discussions

:Page 10, section 2.1.4, modified the text according to Item# 104.00, "Writing the Register Control Bit"

Page 16, section 2.1.6, modified the text according to Item# 104.00, "Writing the Register Control Bit"

Page 28, section 2.5, modified the text according to Item# 104.00, "Writing the Register Control Bit"

Changes made to the document base on September-2008 JEDEC Meeting discussions.

Page 24-28 Added 176-ball Thin-Profile Fine-Pitch BGA (TFBGA) with 0.65mm ball pitch, 8x22 grid, 6.0mmx15mm

Page 24 Added footnote 1 to Figure 18 "Pinout Configuration"– "This package may only be used in new DIMM designs. It is not intended for use in existing DIMMs."

Page 34, section 2.7, modified the text according to Item#104.45, "RC10: Encoding for DIMM Operating Speed"

Page 49 Table 33 "Timing Requirements" fclock (max) DDR3-1600 from 938MHz to 810MHz.

Page 50 Figure 22 title from "Voltage Waveforms for Setup and Hold Times" to "Voltage Waveforms for Setup and Hold Times -Setup time calculations"

Page 51 Figure 23 added "Voltage Waveforms for Setup and Hold Times -Setup time calculations"

Page 52 Table 34 "Output Timing Requirements". tDIS, tEN units from tCK to ps.

Page 54 Table 37 "Clock Driver Characteristic at Application Frequency (Frequency Band 1). Tfdyn (Dynamic Phase Offset) DDR3-1600 min/max from -50/+50 to -40/+40 ps.

Page 64 Added Figure 37 "AVDD Filtering", Section 4 "Recommended Filtering for the Analog Power Supply (AVDD)"

Table 2 "SSTE32882 Device Initialization Sequence". VD to VDD.

Table 11 "Terminal Functions". 1.5-V CMOS to 1.5 V CMOS.

Table 28 "RC11: Operating Voltage VDD Control Word". Vdd to VDD; 'Normal' deleted.

Table 30 "Operating Electrical Characteristics". VIH(AC), VIL(AC), VID(AC) updated for DDR3-1600.

Table 35 "Output Edge Rate Over Specified Free-Air Temperature Range". DDR3-1600 1.5 V rising and falling edge slew rate from 2.8 V/ns min to 2.6 V/ns min

Table 36 "Input IBT Characteristics Over Specified Operating Free-Air Temperature Range". RIBT max from -10% to 10%.

Section 3.1 "Parameter Measurement Information" PRR < 938 MHz to 810 MHz.

Section 3.2 "PRR < 938 MHz to 810 MHz"

## 7 Annex A - (Informative) Differences Between JESD82-29A and JESD29 (cont'd)

Section 3.3 "Output Slew Rate & R-on Target". Table updated for 1.5 V DDR3-800/1066/1333 and DDR3-1600.

Changes made to the document based on December-2008 JEDEC Meeting discussions:

Page 1 Section 2.1 "Description" 1.35 V added to the description.

Page2 Section 2.1.1. Added sentence "The LV (Low voltage) SSTE32882 can be powered-on at 1.5 V or 1.35 V. After the voltage transition, stable power is provided for a minimum of 200 µs with RESET # asserted.

Page 18 Section 2.2 "Control words" modified DBA1 to RC2[DBA1].

Page 29 Section Table 11 "Terminal functions" 1.35 V added.

Page 31 Table 14 "Parity, low power and Standby function table with QuadCS mode disabled" footnote 2 modified to "A/C = DA0..DA15, DBA0..DBA2, DRAS#, DCAS#, DWE#. Inputs DCKE0, DCKE1, DODT0, DODT1, DCS[1:0]# when QCSEN# = HIGH, DCS[3:0]# when QCSEN# = LOW are not included in this range. This column represents the sum of the number of A/C signals that are electrically HIGH."

Page 32 Table 15 "Parity, low power and Standby function table with QuadCS mode enabled" footnote 2 modified to "A/C = DA0..DA15, DBA0..DBA2, DRAS#, DCAS#, DWE#. Inputs DCKE0, DCKE1, DODT0, DODT1, DCS[1:0]# when QCSEN# = HIGH, DCS[3:0]# when QCSEN# = LOW are not included in this range. This column represents the sum of the number of A/C signals that are electrically HIGH."

Page 42 Table 28 "RC11:Operating Voltage VDD Control Word" added footnote 1: "DDR3L 1.35 V register is backward compatible and operable to DDR3 1.5 V specification. To guarantee all timings and specifications for DDR3 1.5 V, the register must be configured with RC11[DA4:DA3]=00b".

Page 46 Table 30 "Operating Electrical Characteristics" added 1.35 V specifications. Footnote 1 modified to "DCKE0/1, DODT0/1, DA0..DA15, DBA0..DBA2, DRAS#, DCAS#, DWE#, PAR_IN, DCS[1:0]# when QCSEN# = HIGH, DCS[3:0]# when QCSEN# = LOW".

Page 47 Table 31 "DC Electrical characteristics" Footnote 1 modified to "DCKE0/1, DODT0/1, DA0..DA15, DBA0..DBA2, DRAS#, DCAS#, DWE#, PAR_IN, DCS[1:0]# when QCSEN# = HIGH, DCS[3:0]# when QCSEN# = LOW are measured while RESET# pulled LOW".

Page 47 Table 32 "Capacitance values" Input capacitance CK,CK#, FBIN# from 2pF min, 3pF max to 1.5pF min, 2.5pF max. Added footnote 2: "Data inputs are DCKE0/1, DODT0/1, DA0..DA15, DBA0..DBA2, DRAS#, DWE#, PAR_IN, DCS[1:0]# when QCSEN# = HIGH, DCS[3:0]# when QCSEN# = LOW".

Page 51 Table 34 "Output timing requirements" tPDM values added for 1.35 V.

Page 52 Table 35 "Output edge rates over specified operating free-air temperature range" rising and falling slew rates for 1.35 V added. Rising and falling slew rates at 1.5 V/ DDR3-1600 from 2.6 V/ns min, 5.5V/ns to 2.0 V/ns min, 5.0V/ns max.

Page 53 Table 37 "Clock driver Characteristics at application frequency (frequency band 1)". Added tstaoff specification for 1.35 V.

Page 58 Figure 31 "Voltage waveforms, propagation delay times" Added 1.35 V on Vi(p-p) footnote.

Page 60 Figure 34 and Figure 35 deleted footnote "AC Level = 150mv (1.5 V Operation)".

Page 60 Added "AC Level for Slew Rate Measurement" table.

Changes made to document based on Dec 2008 JEDEC meeting discussions.

Page 5 Note 4 Changed "VDD is 1.5 (nominal)" to "VDD is nominal"

Page 6 Under Figure 6 "mod" changed to "mode"

Page 9 and 10 Notes under Figures 9 and 10 changed from DCS[1,0]# to DCS[1:0]#

Pages 12 and 13 Referenced note 3 on Figures 11 and 12 changed to note 4

Page 19 Added "It is using the mechanical outline MO-246 variation F.

Page 24 Changed: "It is using the mechanical outline MO-246B" to "It is using the mechanical outline MO-246 variation B"

## 7 Annex A - (Informative) Differences Between JESD82-29A and JESD29 (cont'd)

Page 41 Table 31 Changed "VDD-0.4" to "VDD-0.4".Table 32 Removed Co spec. Added dash in the typical column and formatting. Used the correct DDR3- and DDR3L prefixes. Moved Table 42 to be before Table 22.

Page 42 Text above Table 28: changed "LV conditions" to "DDR3L conditions".

Page 52 Table 36 Note 2 Updated formula format to (1-x/x)*100% <=ABS(5%)

Page 53 Table 37 Removed Note1 "Total Clock Output Skew" spec. Adjusted text under Parameter and Conditions column to match other table format. Swapped "right side" with "left side" and vice versa on Note 2.

Page 56 Table 38, adjusted the format for all notes and changed the "TBD"s to "Vendor Specific" note.

Page 59 Figure 32, changed the reference in the "Calculating the Virtual Vtt Crossing point" from Figure 31 to Figure 33.

Page 64 Removed the dash in Table 42 from "TL0-" to "TL0".

Changed the date on the first page to January 2009

Moved Table 39 to be after Table 37

Tables 19, 25, 26, 27 Updated fonts and sizes to match other tables

Remove Underline on Tables
3,4,11,12,13,14,15,16,21,25,26,28,30,31,32,33,34,35,36,37,38,39,42

Changes made to document based on Feb 2009 JEDEC meeting discussions.

Page 42 Table 31 "Operating Electrical Characteristics". VIX(AC) updated for Wide Range.

Changes made to document based on following balloted item numbers:

104.75

104.56a

104.76

104.68

104.71

104.72

104.78

104.69

## 8 Annex B - (Informative) Differences Between JESD82-29A.01 and JESD29A

Editorial changes as follows:

1. Table 11: terminology update, changed "master clock" to "main clock"
2. Relocate figure titles to bottom of figure per JEDEC standard layout
3. Table NOTES placed inside borders at the bottom of tables per JEDEC standard
4. Corrected cross reference in the note below Figure 31 from "Figure 44" to "Table 44"
5. Changed doesn't to does not in Section 5
6. Changed all instances of unit of measure "us" to "µs"

**Standard Improvement Form** **JEDEC Standard JESD82-29A.01**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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