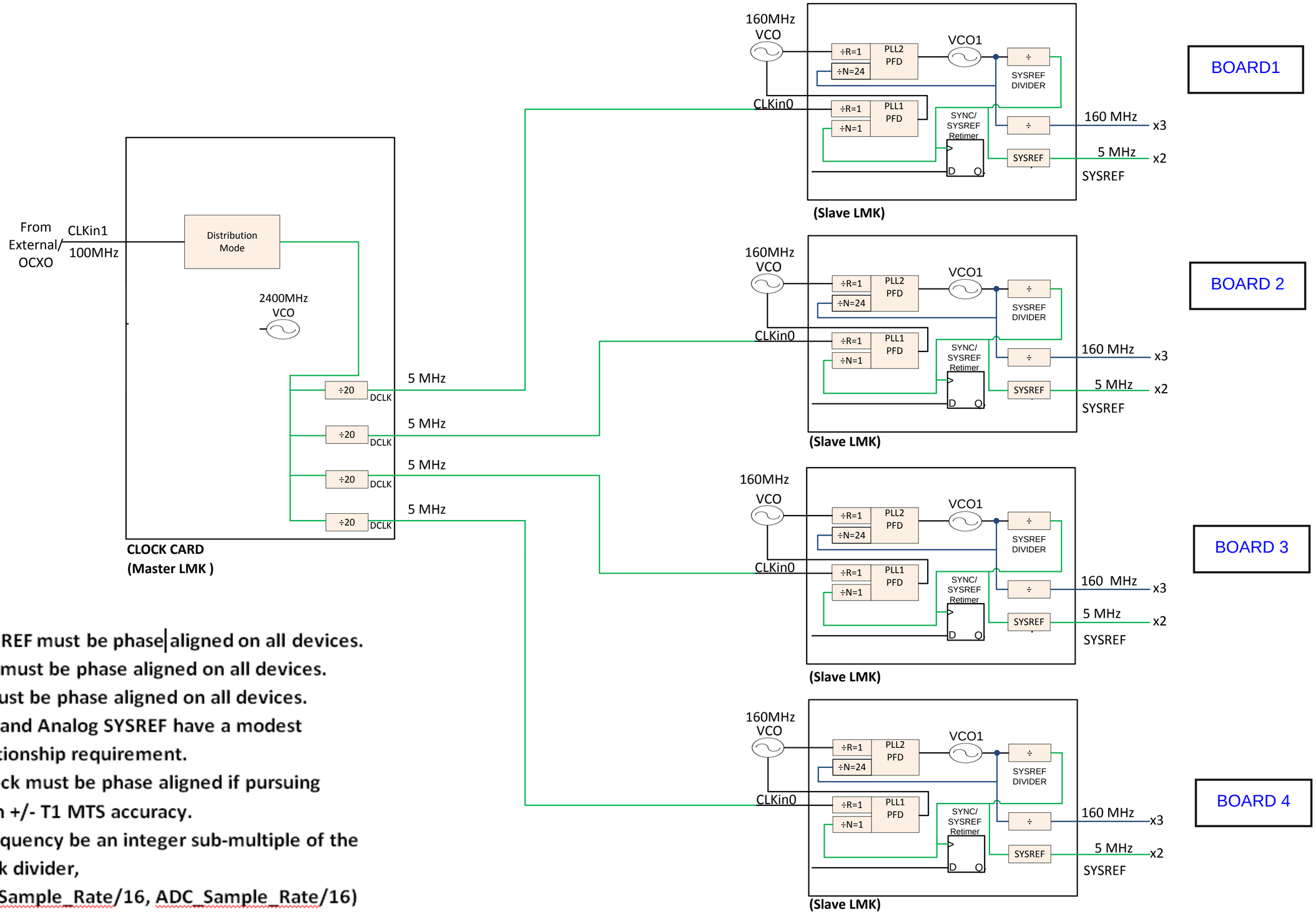
LMK
CLK GEN



1. Analog SYSREF must be phase aligned on all devices.
2. PL SYSREF must be phase aligned on all devices.
3. PL clock must be phase aligned on all devices.
4. PL SYSREF and Analog SYSREF have a modest phase relationship requirement.
5. Sample clock must be phase aligned if pursuing better than +/- T1 MTS accuracy.
6. SYSREF frequency be an integer sub-multiple of the global clock divider, GCD(DAC_Sample_Rate/16, ADC_Sample_Rate/16)
7. SYSREF must be an integer submultiples of all PL Clocks. So now the SYSREF is getting safe captured in the PL clock domains.