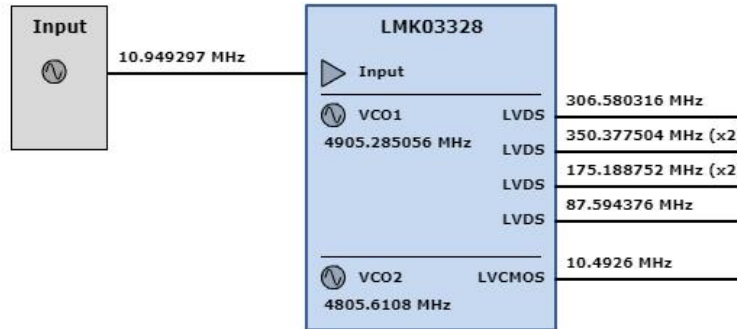


# WEBENCH<sup>®</sup> Clock Architect

## Project Report

Project: 4342674/74 Project 74 - [LMK03328]  
Created: 7/17/19 9:22:17 AM



Block Diagram

### My Comments

No comments

## System Specification and Parameters

### Fixed Outputs

Name	Freq (MHz)	Format	Count
10R5MHZ_L5	10.4926	LVC MOS	1
FREF_FPGA1	175.188752	LVDS	1
FREF_FPGA2	350.377504	LVDS	1
FREF_FPGA3	350.377504	LVDS	1
FREF_FPGA4	175.188752	LVDS	1
GEM_TSU_CLK	306.580316	Any	1
L5_CLK	87.594376	LVDS	1

### Options

Name	Design Value
Automatically Select	No
Input Frequencies	
Part Filter	LMK03328

### Properties

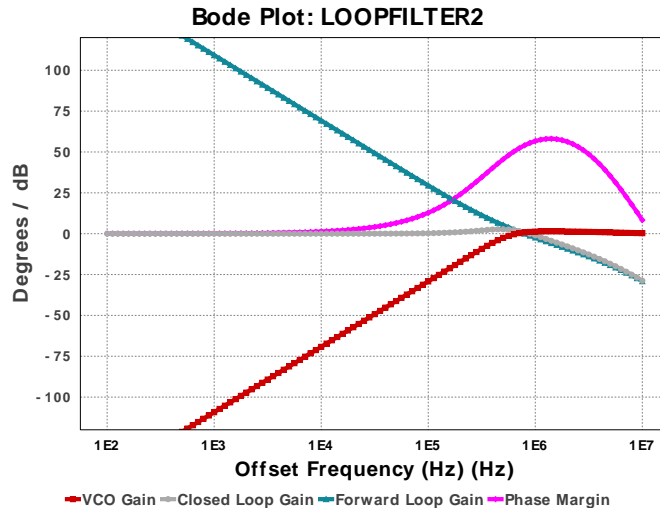
Name	Design Value
External Sources	none
Total BOM Cost	\$10.0
Total Current	627.5 mA
Total Footprint	49.0 mm <sup>2</sup>



User ID = 4342674  
 Design Id = 325  
 Device = LMK03328  
 Created = 7/17/19 9:22:17 AM

## WEBENCH® Clock Design Report

Loop Filter: LMK03328 LOOPFILTER2



### Preferences

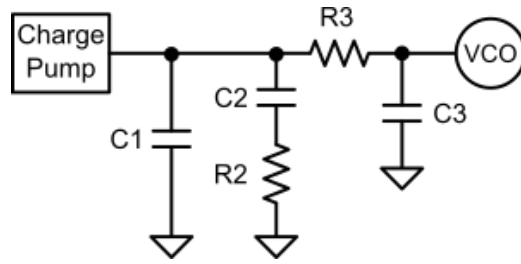
Name	Design Value
Filter Type	Passive
Filter Order	3rd Order
Op Amp Gain	1.00
Charge Pump Gain	6.40 mA
VCO Gain	40.00 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	10.949 MHz
Phase Det. Frequency	10.949 MHz
Filter type	designed
Brickwall Bandwidth	1389.1843768664905 kHz
Delta Sigma Order	3
Randomization Factor	0.0 %
PLL Whole Part	1
PLL Numerator	0.0
PLL Denominator	1.0
Reference spurs	enabled
Fractional spurs	disabled
Subfractional spurs	disabled
Other spurs	enabled

### Parameters

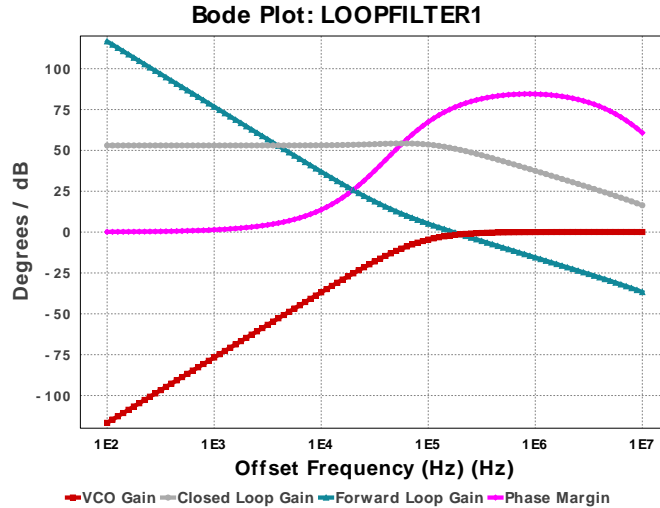
Name	Design Value	Forced	Actual Value
Loop Bandwidth	1094.93 kHz	N	1389.184 kHz
Phase Margin	49.20 deg	N	12.042 deg
T3/T1Ratio	50.00 %	N	22.03 %
T4/T3Ratio	0.00 %	N	0.00 %
Gamma	0.964	N	0.141

### Loop Filter Components

Name	Target Value	Fixed	Forced
C1	0.355 nF	Y	N
C2	3.30 nF	N	Y
C3	0.035 nF	Y	N
C4	Open	N	N
R2	0.018 kohms	Y	N
R3	0.717 kohms	Y	N



## Loop Filter: LMK03328 LOOPFILTER1



### Preferences

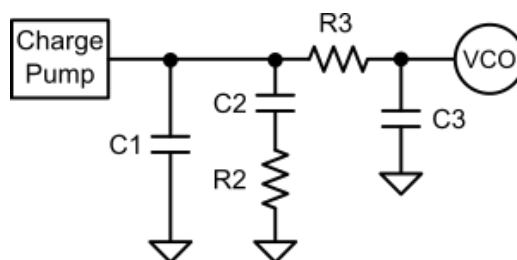
Name	Design Value
Filter Type	Passive
Filter Order	3rd Order
Op Amp Gain	1.00
Charge Pump Gain	6.40 mA
VCO Gain	41.755 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	4905.285 MHz
Phase Det. Frequency	10.949 MHz
Filter type	designed
Brickwall Bandwidth	64.35278493753424 kHz
Delta Sigma Order	3
Randomization Factor	0.0 %
PLL Whole Part	447
PLL Numerator	109480.0
PLL Denominator	109493.0
Reference spurs	enabled
Fractional spurs	disabled
Subfractional spurs	disabled
Other spurs	enabled

### Parameters

Name	Design Value	Forced	Actual Value
Loop Bandwidth	13.198 kHz	N	64.353 kHz
Phase Margin	70.00 deg	N	3.944 deg
T3/T1Ratio	50.00 %	N	18.716 %
T4/T3Ratio	0.00 %	N	0.00 %
Gamma	0.24	N	0.019

### Loop Filter Components

Name	Target Value	Fixed	Forced
C1	0.355 nF	Y	N
C2	3.30 nF	N	Y
C3	0.035 nF	Y	N
C4	Open	N	N
R2	0.133 kohms	Y	N
R3	6.299 kohms	Y	N



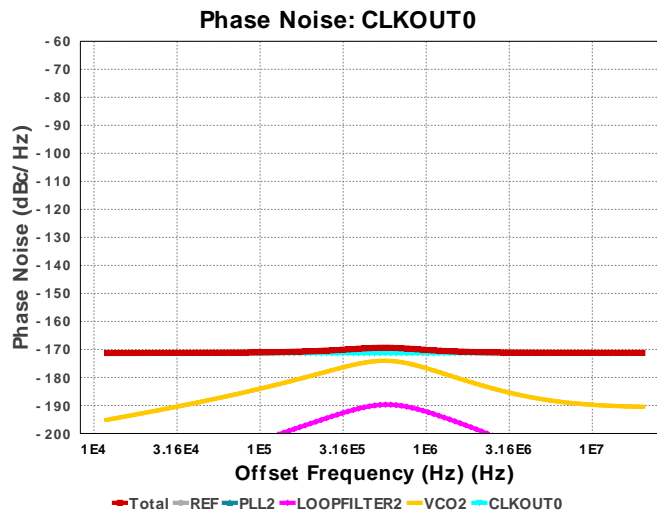
Output Block: LMK03328 LMK03328 : CLKOUT0 as LVCMOS output, 0+10949297/458000000 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-170.959 dBc/Hz
RMS Jitter	119194.859 fs
RMS Phase Error (deg)	0.001 deg
RMS Phase Error	0.018 mrad
EVM	0.002%
SNR	94.941 dB
Spur	-97.941 dBc
Jitter (Pk-Pk)	849918.301 fs
Jitter (Cycle to Cycle Pk)	1699836.602 fs
Jitter (Cycle to Cycle RMS)	168566.986 fs
A/D ENOB	15.485 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	12	100	20000
<b>Total</b>	-170.73	-171.19	-171.23
<b>REF</b>	-179.93	-188.14	-242.55
<b>PLL2</b>	-212.73	-212.79	-254.68
<b>LOOPFILTER2</b>	-236.75	-218.29	-229.98
<b>VCO2</b>	-210.77	-199.66	-190.47
<b>CLKOUT0</b>	-171.29	-171.29	-171.29



Spurs are not displayed in this PDF version of the phase noise graph. See the simulation page in Clock Architect to view the spurs in the phase noise graph.

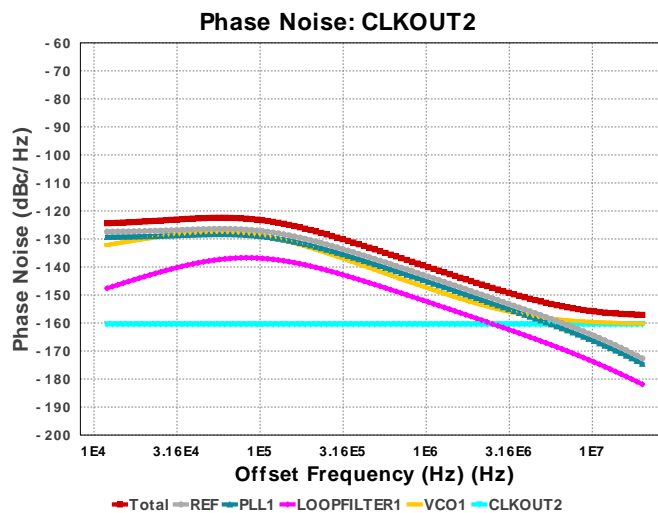
## Output Block: LMK03328 LMK03328 : CLKOUT2 as LVDS output, 350.3775 MHz

## Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-114.509 dBc/Hz
RMS Jitter	5404.358 fs
RMS Phase Error (deg)	0.682 deg
RMS Phase Error	11.898 mrad
EVM	1.19%
SNR	38.491 dB
Spur	-41.491 dBc
Jitter (Pk-Pk)	38535.743 fs
Jitter (Cycle to Cycle Pk)	77071.487 fs
Jitter (Cycle to Cycle RMS)	7642.916 fs
A/D ENOB	6.108 bits
TIE (Time Interval Error)	-0.284
UI (Unit Interval)	0.002
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

## Phase Noise Values (dBc/Hz)

Offset	12	100	20000
<b>Total</b>	-96.29	-107.34	-157.32
<b>REF</b>	-96.3	-107.67	-225.87
<b>PLL1</b>	-129.1	-132.31	-238
<b>LOOPFILTER1</b>	-143.7	-128.71	-208.34
<b>VCO1</b>	-127.16	-119.43	-160.22
<b>CLKOUT2</b>	-160.44	-160.44	-160.44



Spurs are not displayed in this PDF version of the phase noise graph. See the simulation page in Clock Architect to view the spurs in the phase noise graph.

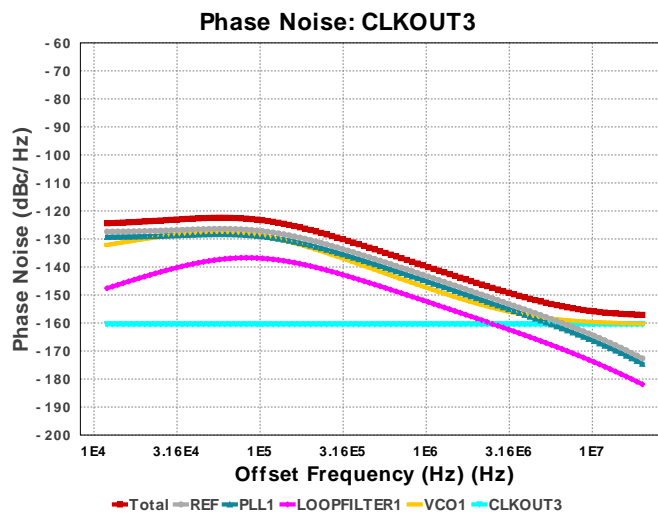
## Output Block: LMK03328 LMK03328 : CLKOUT3 as LVDS output, 350.3775 MHz

## Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-114.509 dBc/Hz
RMS Jitter	5404.358 fs
RMS Phase Error (deg)	0.682 deg
RMS Phase Error	11.898 mrad
EVM	1.19%
SNR	38.491 dB
Spur	-41.491 dBc
Jitter (Pk-Pk)	38535.743 fs
Jitter (Cycle to Cycle Pk)	77071.487 fs
Jitter (Cycle to Cycle RMS)	7642.916 fs
A/D ENOB	6.108 bits
TIE (Time Interval Error)	-0.284
UI (Unit Interval)	0.002
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

## Phase Noise Values (dBc/Hz)

Offset	12	100	20000
<b>Total</b>	-96.29	-107.34	-157.32
<b>REF</b>	-96.3	-107.67	-225.87
<b>PLL1</b>	-129.1	-132.31	-238
<b>LOOPFILTER1</b>	-143.7	-128.71	-208.34
<b>VCO1</b>	-127.16	-119.43	-160.22
<b>CLKOUT3</b>	-160.44	-160.44	-160.44



Spurs are not displayed in this PDF version of the phase noise graph. See the simulation page in Clock Architect to view the spurs in the phase noise graph.

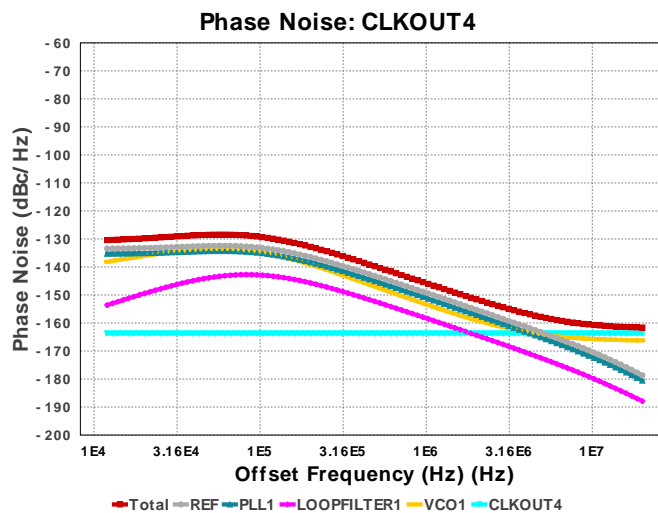
## Output Block: LMK03328 LMK03328 : CLKOUT4 as LVDS output, 175.1888 MHz

## Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-120.529 dBc/Hz
RMS Jitter	5404.419 fs
RMS Phase Error (deg)	0.341 deg
RMS Phase Error	5.949 mrad
EVM	0.595%
SNR	44.511 dB
Spur	-47.511 dBc
Jitter (Pk-Pk)	38536.183 fs
Jitter (Cycle to Cycle Pk)	77072.365 fs
Jitter (Cycle to Cycle RMS)	7643.003 fs
A/D ENOB	7.108 bits
TIE (Time Interval Error)	-0.285
UI (Unit Interval)	0.001
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

## Phase Noise Values (dBc/Hz)

Offset	12	100	20000
<b>Total</b>	-102.31	-113.36	-161.77
<b>REF</b>	-102.32	-113.69	-231.89
<b>PLL1</b>	-135.12	-138.34	-244.03
<b>LOOPFILTER1</b>	-149.72	-134.73	-214.36
<b>VCO1</b>	-133.18	-125.45	-166.24
<b>CLKOUT4</b>	-163.69	-163.69	-163.69



Spurs are not displayed in this PDF version of the phase noise graph. See the simulation page in Clock Architect to view the spurs in the phase noise graph.



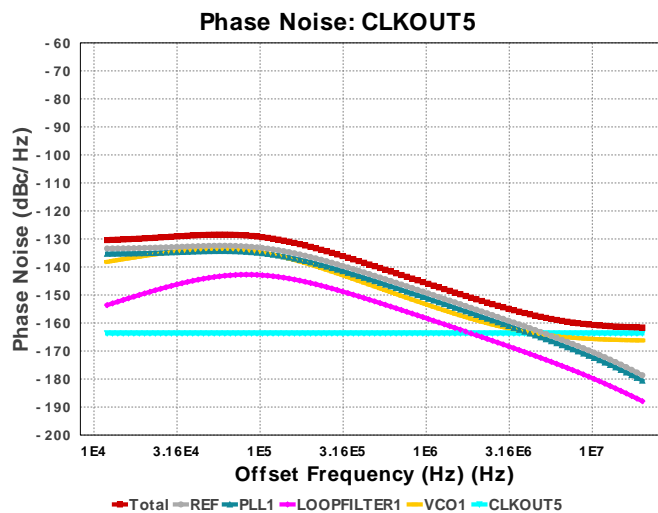
## Output Block: LMK03328 LMK03328 : CLKOUT5 as LVDS output, 175.1888 MHz

## Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-120.529 dBc/Hz
RMS Jitter	5404.419 fs
RMS Phase Error (deg)	0.341 deg
RMS Phase Error	5.949 mrad
EVM	0.595%
SNR	44.511 dB
Spur	-47.511 dBc
Jitter (Pk-Pk)	38536.183 fs
Jitter (Cycle to Cycle Pk)	77072.365 fs
Jitter (Cycle to Cycle RMS)	7643.003 fs
A/D ENOB	7.108 bits
TIE (Time Interval Error)	-0.285
UI (Unit Interval)	0.001
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

## Phase Noise Values (dBc/Hz)

Offset	12	100	20000
<b>Total</b>	-102.31	-113.36	-161.77
<b>REF</b>	-102.32	-113.69	-231.89
<b>PLL1</b>	-135.12	-138.34	-244.03
<b>LOOPFILTER1</b>	-149.72	-134.73	-214.36
<b>VCO1</b>	-133.18	-125.45	-166.24
<b>CLKOUT5</b>	-163.69	-163.69	-163.69



Spurs are not displayed in this PDF version of the phase noise graph. See the simulation page in Clock Architect to view the spurs in the phase noise graph.

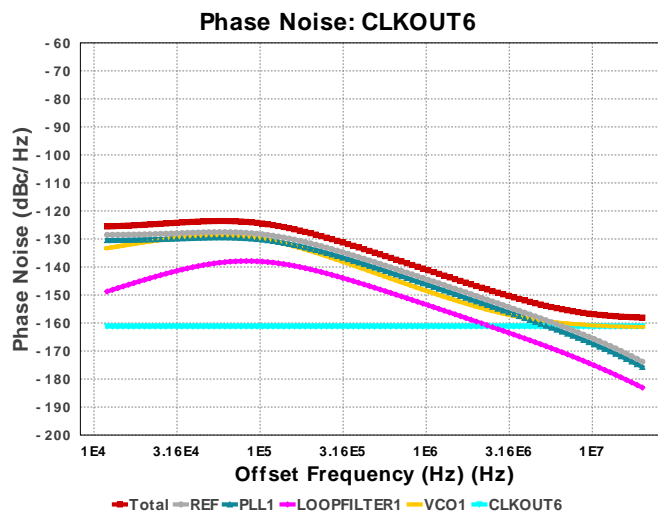
## Output Block: LMK03328 LMK03328 : CLKOUT6 as LVDS output, 306.5803 MHz

## Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-115.669 dBc/Hz
RMS Jitter	5404.364 fs
RMS Phase Error (deg)	0.596 deg
RMS Phase Error	10.41 mrad
EVM	1.041%
SNR	39.651 dB
Spur	-42.651 dBc
Jitter (Pk-Pk)	38535.789 fs
Jitter (Cycle to Cycle Pk)	77071.578 fs
Jitter (Cycle to Cycle RMS)	7642.925 fs
A/D ENOB	6.301 bits
TIE (Time Interval Error)	-0.284
UI (Unit Interval)	0.002
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

## Phase Noise Values (dBc/Hz)

Offset	12	100	20000
<b>Total</b>	-97.45	-108.5	-158.29
<b>REF</b>	-97.46	-108.83	-227.03
<b>PLL1</b>	-130.26	-133.47	-239.16
<b>LOOPFILTER1</b>	-144.86	-129.87	-209.5
<b>VCO1</b>	-128.32	-120.59	-161.38
<b>CLKOUT6</b>	-161.22	-161.22	-161.22



Spurs are not displayed in this PDF version of the phase noise graph. See the simulation page in Clock Architect to view the spurs in the phase noise graph.

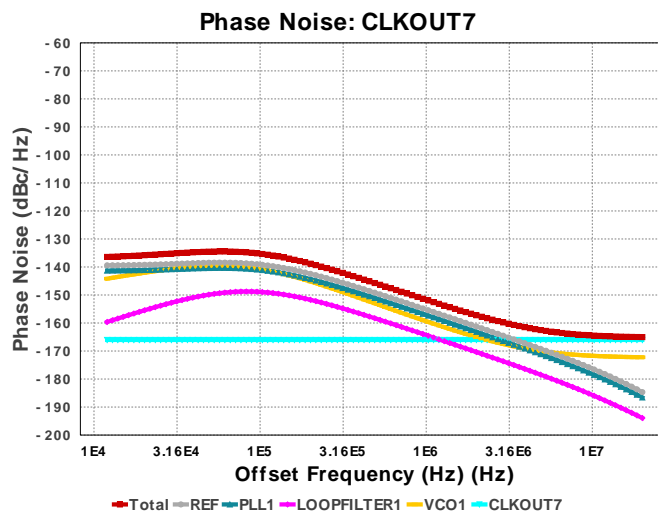
## Output Block: LMK03328 LMK03328 : CLKOUT7 as LVDS output, 87.5944 MHz

## Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-126.55 dBc/Hz
RMS Jitter	5404.593 fs
RMS Phase Error (deg)	0.17 deg
RMS Phase Error	2.975 mrad
EVM	0.297%
SNR	50.532 dB
Spur	-53.532 dBc
Jitter (Pk-Pk)	38537.418 fs
Jitter (Cycle to Cycle Pk)	77074.837 fs
Jitter (Cycle to Cycle RMS)	7643.248 fs
A/D ENOB	8.108 bits
TIE (Time Interval Error)	-0.285
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

## Phase Noise Values (dBc/Hz)

Offset	12	100	20000
<b>Total</b>	-108.33	-119.38	-165.11
<b>REF</b>	-108.34	-119.71	-237.91
<b>PLL1</b>	-141.14	-144.36	-250.05
<b>LOOPFILTER1</b>	-155.74	-140.75	-220.38
<b>VCO1</b>	-139.2	-131.47	-172.26
<b>CLKOUT7</b>	-166.04	-166.04	-166.04



Spurs are not displayed in this PDF version of the phase noise graph. See the simulation page in Clock Architect to view the spurs in the phase noise graph.

## REF at MHz

Offset	Phase Noise
0.01 kHz	-90.0 dBc/Hz
0.1 kHz	-108.0 dBc/Hz
1.0 kHz	-117.0 dBc/Hz
10.0 kHz	-126.0 dBc/Hz
100.0 kHz	-135.0 dBc/Hz
1000.0 kHz	-141.0 dBc/Hz
10000.0 kHz	-146.0 dBc/Hz

## VCO2 at MHz

Offset	Phase Noise
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## VCO1 at MHz

Offset	Phase Noise
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