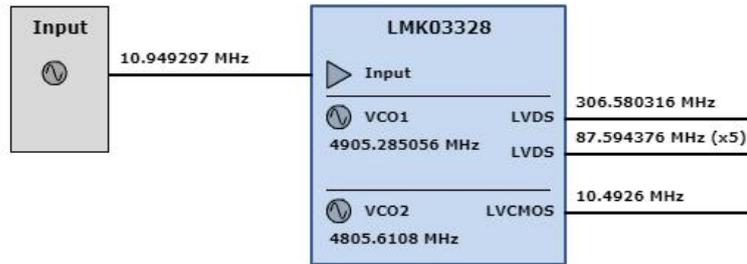


WEBENCH[®] Clock Architect

Project Report

Project: 4342674/87 Project 87 - [LMK03328]
Created: 2019-07-23 07:44:00.648



Block Diagram

My Comments

No comments

System Specification and Parameters

Fixed Outputs

Name	Freq (MHz)	Format	Count
10R5MHZ_L5	10.4926	LVCMOS	1
FREF_FPGAX	87.594376	LVDS	4
GEM_TSU_CLK	306.580316	Any	1
L5_CLK	87.594376	LVDS	1

Options

Name	Design Value
Automatically Select	No
Input Frequencies	
Part Filter	LMK03328

Properties

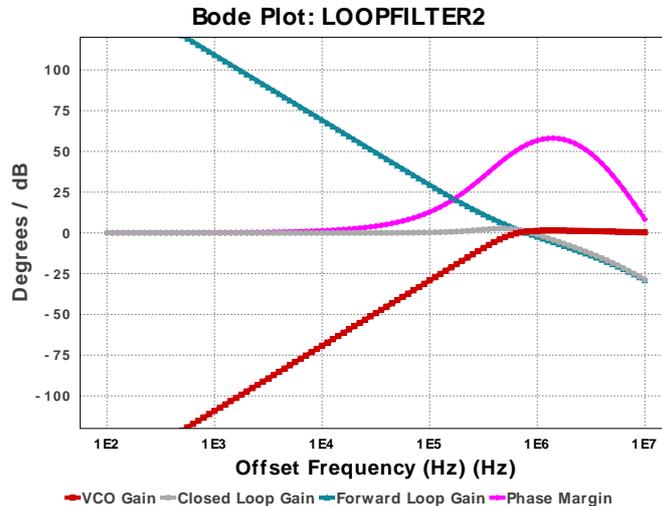
Name	Design Value
External Sources	none
Total BOM Cost	\$10.0
Total Current	627.5 mA
Total Footprint	49.0 mm ²



User ID = 4342674
 Design Id = 338
 Device = LMK03328
 Created = 2019-07-23 07:44:00.719

WEBENCH® Clock Design Report

Loop Filter: LMK03328 LOOPFILTER2



Preferences

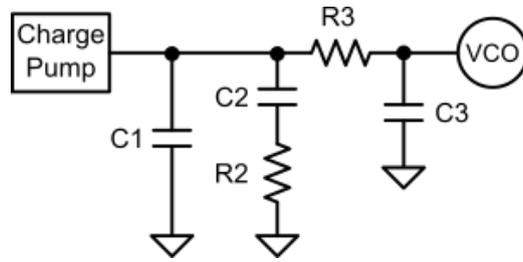
Name	Design Value
Filter Type	Passive
Filter Order	3rd Order
Op Amp Gain	1.00
Charge Pump Gain	6.40 mA
VCO Gain	40.094 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	4805.611 MHz
Phase Det. Frequency	21.899 MHz
Filter type	designed
Brickwall Bandwidth	89.1782006077488 kHz
Delta Sigma Order	3
Randomization Factor	0.0 %
PLL Whole Part	219
PLL Numerator	49087.0
PLL Denominator	109493.0
Reference spurs	enabled
Fractional spurs	disabled
Subfractional spurs	disabled
Other spurs	enabled

Parameters

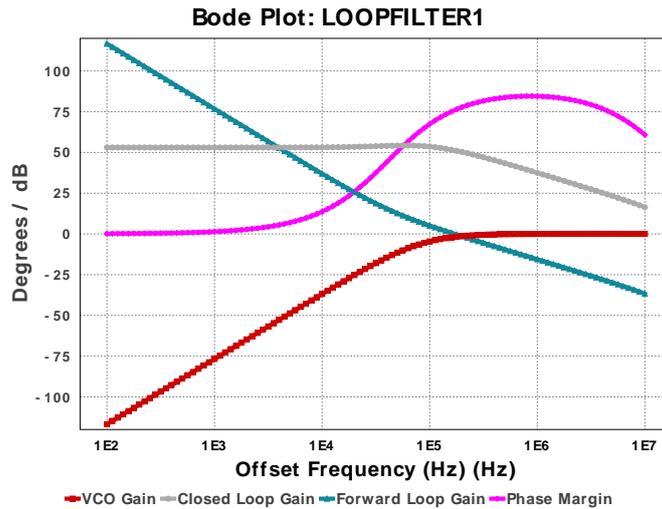
Name	Design Value	Forced	Actual Value
Loop Bandwidth	11.661 kHz	N	89.178 kHz
Phase Margin	49.20 deg	N	354.729 deg
T3/T1Ratio	50.00 %	N	2.629 %
T4/T3Ratio	0.00 %	N	0.00 %
Gamma	0.964	N	0.004

Loop Filter Components

Name	Target Value	Fixed	Forced
C1	0.355 nF	Y	N
C2	3.30 nF	N	Y
C3	0.035 nF	Y	N
C4	Open	N	N
R2	0.018 kohms	Y	N
R3	6.299 kohms	Y	N



Loop Filter: LMK03328 LOOPFILTER1



Preferences

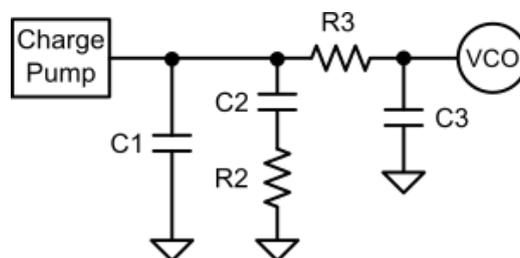
Name	Design Value
Filter Type	Passive
Filter Order	3rd Order
Op Amp Gain	1.00
Charge Pump Gain	6.40 mA
VCO Gain	41.755 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	4905.285 MHz
Phase Det. Frequency	21.899 MHz
Filter type	designed
Brickwall Bandwidth	90.17586297715815 kHz
Delta Sigma Order	3
Randomization Factor	0.0 %
PLL Whole Part	223
PLL Numerator	218973.0
PLL Denominator	218986.0
Reference spurs	enabled
Fractional spurs	disabled
Subfractional spurs	disabled
Other spurs	enabled

Parameters

Name	Design Value	Forced	Actual Value
Loop Bandwidth	13.198 kHz	N	90.176 kHz
Phase Margin	70.00 deg	N	354.671 deg
T3/T1Ratio	50.00 %	N	2.629 %
T4/T3Ratio	0.00 %	N	0.00 %
Gamma	0.24	N	0.004

Loop Filter Components

Name	Target Value	Fixed	Forced
C1	0.355 nF	Y	N
C2	3.30 nF	N	Y
C3	0.035 nF	Y	N
C4	Open	N	N
R2	0.018 kohms	Y	N
R3	6.299 kohms	Y	N



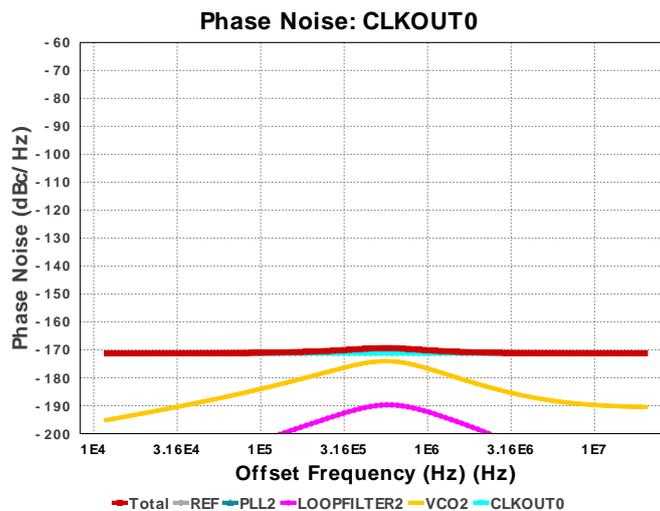
Output Block: LMK03328 LMK03328 : CLKOUT0 as LVCMOS output, 0+10949297/458000000 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-145.563 dBc/Hz
RMS Jitter	2218482.269 fs
RMS Phase Error (deg)	0.019 deg
RMS Phase Error	0.333 mrad
EVM	0.033%
SNR	69.545 dB
Spur	-72.545 dBc
Jitter (Pk-Pk)	15818875.866 fs
Jitter (Cycle to Cycle Pk)	31637751.732 fs
Jitter (Cycle to Cycle RMS)	3137407.712 fs
A/D ENOB	11.267 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	12	100	20000
Total	-126.92	-123.99	-171.23
REF	-126.93	-124.08	-256.23
PLL2	-162.62	-151.73	-270.07
LOOPFILTER2	-180.4	-150.9	-239.01
VCO2	-163.77	-141.52	-190.53
CLKOUT0	-171.29	-171.29	-171.29



Spurs are not displayed in this PDF version of the phase noise graph. See the simulation page in Clock Architect to view the spurs in the phase noise graph.

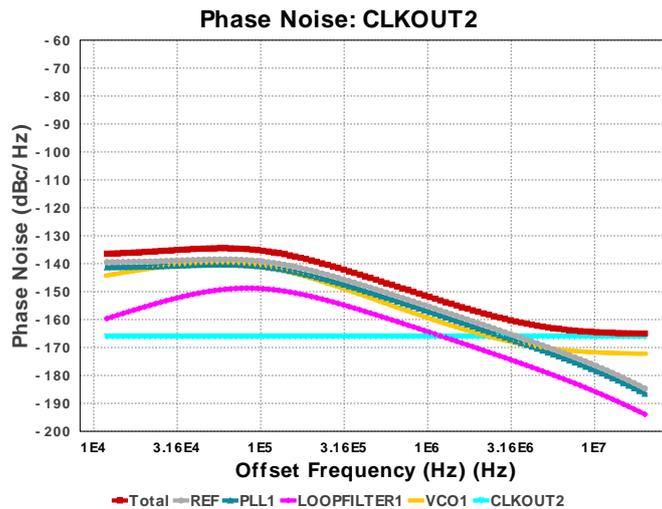
Output Block: LMK03328 LMK03328 : CLKOUT2 as LVDS output, 87.5944 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-127.251 dBc/Hz
RMS Jitter	4985.403 fs
RMS Phase Error (deg)	0.157 deg
RMS Phase Error	2.744 mrad
EVM	0.274%
SNR	51.233 dB
Spur	-54.233 dBc
Jitter (Pk-Pk)	35548.392 fs
Jitter (Cycle to Cycle Pk)	71096.784 fs
Jitter (Cycle to Cycle RMS)	7050.425 fs
A/D ENOB	8.225 bits
TIE (Time Interval Error)	-0.285
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	12	100	20000
Total	-108.49	-104.71	-165.11
REF	-108.5	-104.8	-237.61
PLL1	-144.19	-132.44	-251.45
LOOPFILTER1	-161.98	-131.62	-220.38
VCO1	-145.38	-122.28	-172.26
CLKOUT2	-166.04	-166.04	-166.04



Spurs are not displayed in this PDF version of the phase noise graph. See the simulation page in Clock Architect to view the spurs in the phase noise graph.

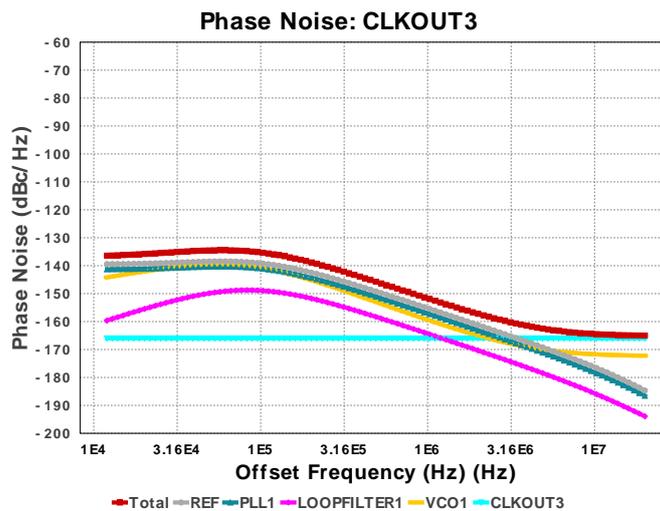
Output Block: LMK03328 LMK03328 : CLKOUT3 as LVDS output, 87.5944 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-127.251 dBc/Hz
RMS Jitter	4985.403 fs
RMS Phase Error (deg)	0.157 deg
RMS Phase Error	2.744 mrad
EVM	0.274%
SNR	51.233 dB
Spur	-54.233 dBc
Jitter (Pk-Pk)	35548.392 fs
Jitter (Cycle to Cycle Pk)	71096.784 fs
Jitter (Cycle to Cycle RMS)	7050.425 fs
A/D ENOB	8.225 bits
TIE (Time Interval Error)	-0.285
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	12	100	20000
Total	-108.49	-104.71	-165.11
REF	-108.5	-104.8	-237.61
PLL1	-144.19	-132.44	-251.45
LOOPFILTER1	-161.98	-131.62	-220.38
VCO1	-145.38	-122.28	-172.26
CLKOUT3	-166.04	-166.04	-166.04



Spurs are not displayed in this PDF version of the phase noise graph. See the simulation page in Clock Architect to view the spurs in the phase noise graph.

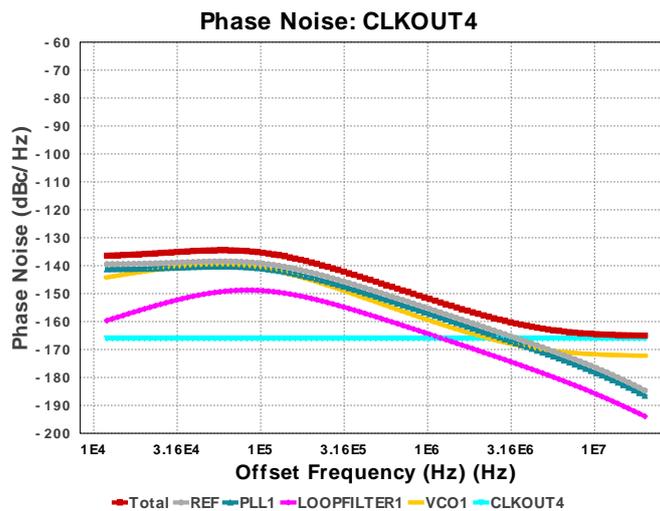
Output Block: LMK03328 LMK03328 : CLKOUT4 as LVDS output, 87.5944 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-127.251 dBc/Hz
RMS Jitter	4985.403 fs
RMS Phase Error (deg)	0.157 deg
RMS Phase Error	2.744 mrad
EVM	0.274%
SNR	51.233 dB
Spur	-54.233 dBc
Jitter (Pk-Pk)	35548.392 fs
Jitter (Cycle to Cycle Pk)	71096.784 fs
Jitter (Cycle to Cycle RMS)	7050.425 fs
A/D ENOB	8.225 bits
TIE (Time Interval Error)	-0.285
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	12	100	20000
Total	-108.49	-104.71	-165.11
REF	-108.5	-104.8	-237.61
PLL1	-144.19	-132.44	-251.45
LOOPFILTER1	-161.98	-131.62	-220.38
VCO1	-145.38	-122.28	-172.26
CLKOUT4	-166.04	-166.04	-166.04



Spurs are not displayed in this PDF version of the phase noise graph. See the simulation page in Clock Architect to view the spurs in the phase noise graph.

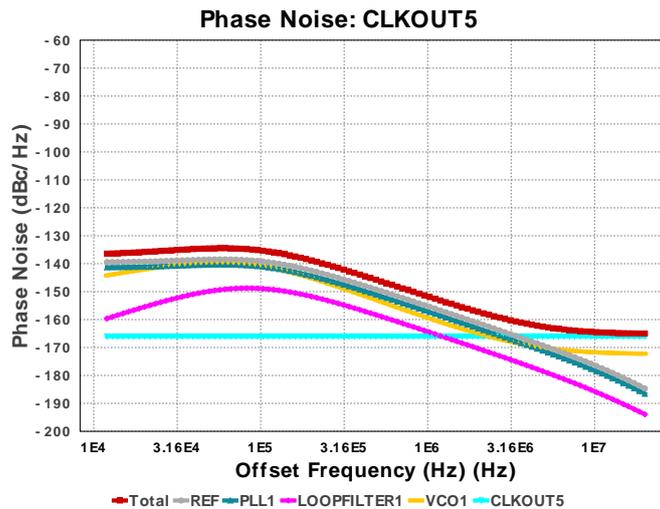
Output Block: LMK03328 LMK03328 : CLKOUT5 as LVDS output, 87.5944 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-127.251 dBc/Hz
RMS Jitter	4985.403 fs
RMS Phase Error (deg)	0.157 deg
RMS Phase Error	2.744 mrad
EVM	0.274%
SNR	51.233 dB
Spur	-54.233 dBc
Jitter (Pk-Pk)	35548.392 fs
Jitter (Cycle to Cycle Pk)	71096.784 fs
Jitter (Cycle to Cycle RMS)	7050.425 fs
A/D ENOB	8.225 bits
TIE (Time Interval Error)	-0.285
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	12	100	20000
Total	-108.49	-104.71	-165.11
REF	-108.5	-104.8	-237.61
PLL1	-144.19	-132.44	-251.45
LOOPFILTER1	-161.98	-131.62	-220.38
VCO1	-145.38	-122.28	-172.26
CLKOUT5	-166.04	-166.04	-166.04



Spurs are not displayed in this PDF version of the phase noise graph. See the simulation page in Clock Architect to view the spurs in the phase noise graph.

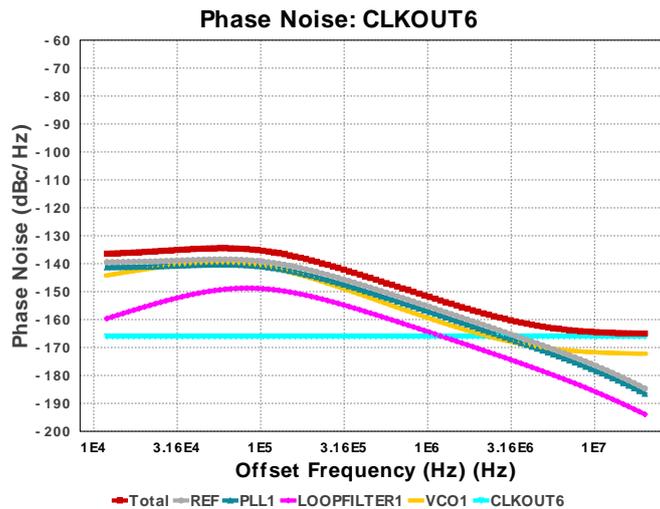
Output Block: LMK03328 LMK03328 : CLKOUT6 as LVDS output, 87.5944 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-127.251 dBc/Hz
RMS Jitter	4985.403 fs
RMS Phase Error (deg)	0.157 deg
RMS Phase Error	2.744 mrad
EVM	0.274%
SNR	51.233 dB
Spur	-54.233 dBc
Jitter (Pk-Pk)	35548.392 fs
Jitter (Cycle to Cycle Pk)	71096.784 fs
Jitter (Cycle to Cycle RMS)	7050.425 fs
A/D ENOB	8.225 bits
TIE (Time Interval Error)	-0.285
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	12	100	20000
Total	-108.49	-104.71	-165.11
REF	-108.5	-104.8	-237.61
PLL1	-144.19	-132.44	-251.45
LOOPFILTER1	-161.98	-131.62	-220.38
VCO1	-145.38	-122.28	-172.26
CLKOUT6	-166.04	-166.04	-166.04



Spurs are not displayed in this PDF version of the phase noise graph. See the simulation page in Clock Architect to view the spurs in the phase noise graph.

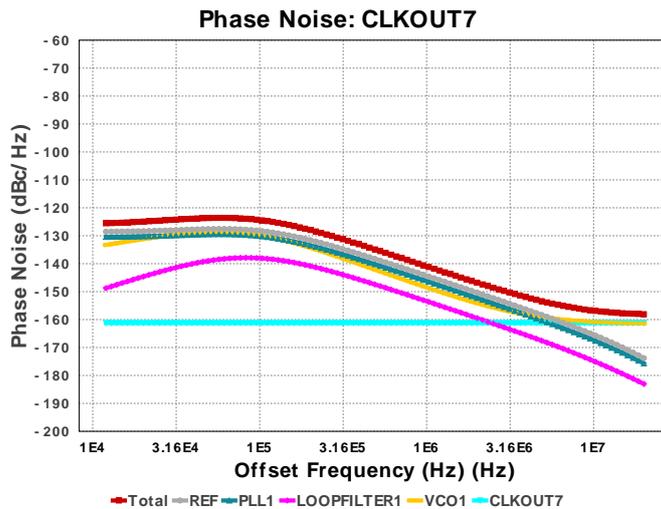
Output Block: LMK03328 LMK03328 : CLKOUT7 as LVDS output, 306.5803 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-116.37 dBc/Hz
RMS Jitter	4985.156 fs
RMS Phase Error (deg)	0.55 deg
RMS Phase Error	9.603 mrad
EVM	0.96%
SNR	40.352 dB
Spur	-43.352 dBc
Jitter (Pk-Pk)	35546.626 fs
Jitter (Cycle to Cycle Pk)	71093.252 fs
Jitter (Cycle to Cycle RMS)	7050.075 fs
A/D ENOB	6.417 bits
TIE (Time Interval Error)	-0.285
UI (Unit Interval)	0.002
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	12	100	20000
Total	-97.61	-93.83	-158.29
REF	-97.62	-93.92	-226.72
PLL1	-133.31	-121.56	-240.57
LOOPFILTER1	-151.09	-120.74	-209.5
VCO1	-134.5	-111.4	-161.38
CLKOUT7	-161.22	-161.22	-161.22



Spurs are not displayed in this PDF version of the phase noise graph. See the simulation page in Clock Architect to view the spurs in the phase noise graph.

REF at MHz

Offset	Phase Noise
0.01 kHz	-90.0 dBc/Hz
0.1 kHz	-108.0 dBc/Hz
1.0 kHz	-117.0 dBc/Hz
10.0 kHz	-126.0 dBc/Hz
100.0 kHz	-135.0 dBc/Hz
1000.0 kHz	-141.0 dBc/Hz

VCO2 at MHz

Offset	Phase Noise
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VCO1 at MHz

Offset	Phase Noise
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