TICS Pro - LMK04616

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Read All Registers | Write All Registers | Toggle Sync

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  - Tool: PLL2 Loop Filter
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  - Burst Mode

General | Context

```
Field Name: PLL1_LDO_WAIT_TMR

Register Name: R84
Start Bit: 0
Stop Bit   : 3
Length     : 4

Description: PLL1 LDO Wait Timer.
The PLL1 LDO Wait Timer counts a
number of clock cycles equal to 32*
(PLL1_LDO_WAIT_TMR+31) before
releasing the PLL1 NDIV and RDIV
resets.
```

PLL1 Control

PLL1_STORAGE_CELL 11 — Read storage cell

The read back storage cell value provides an indication of the level of the analog tuning voltage for the external VCXO.

MHz | Input Buffers | Dividers | Inversion | MHz | Reference Mux

122.88	CLKIN0_EN: Differential	CLKIN0_PLL1_RDIV: 100	CLKIN0_INVERSION	1.2288	CLKINBLK ALL_EN
122.88	CLKIN1_EN: 1=Single-ended	CLKIN1_PLL1_RDIV: 100	CLKIN1_INVERSION	1.2288	CLKINSEL1_MODE: 2=Register
122.88	CLKIN2_EN: 0=Differential	CLKIN2_PLL1_RDIV: 100	CLKIN2_INVERSION	1.2288	SW_REFINSEL: 0: None
122.88	CLKIN3_EN: 0=Differential	CLKIN3_PLL1_RDIV: 100	CLKIN3_INVERSION	1.2288	CLKINSEL1_INV: 0=Non-Inverted
					CLKMUX: 8:CLKIN3 — Read

PLL1_RDIV_CLKEN PLL1_RDIV_SWRST RST

PLL1_NDIV 100 — FBCLK INVERSION — 1.2288 MHz

PLL1_NDIV_CLKEN PLL1_NDIV_SWRST RST

PFD: PLL1_DIR_POS_GAI 1=Positive — PLL1_SWRST RST

Charge Pumps: Integral Final 0 — Fast Lock 3 — Proportional Final 10 — Fast Lock 50 — PLL1_EN_REGULATION

122.88 MHz — VCXO

FIN	FVCXO	PLL1_RDIV	PLL1_NDIV	PROP MODE	PLL1_PROP	PLL1_INTG	C3
122.88 MHz	122.88 MHz	100	100	Low Pulse Mode	2	0	4.7 µF
122.88 MHz	122.88 MHz	100	100	Low Pulse Mode	10	0	4.7 µF
122.88 MHz	30.72 MHz	100	25	Low Pulse Mode	2	0	4.7 µF
122.88 MHz	30.72 MHz	100	25	Low Pulse Mode	10	0	4.7 µF

E-Mail Support @ TI

CLKIN_STAGGER_EN — Disable RDIV/NDIV 50% Duty Cycle CLK Output

CLKIN_SWRST

PLL1_LDO_WAIT_TMR 0

PLL1_LOL_NORESET

PLL1_RC_CLK_EN

PLL1_RC_CLK_DIV 1

PLL1_F_30 0=122MHz

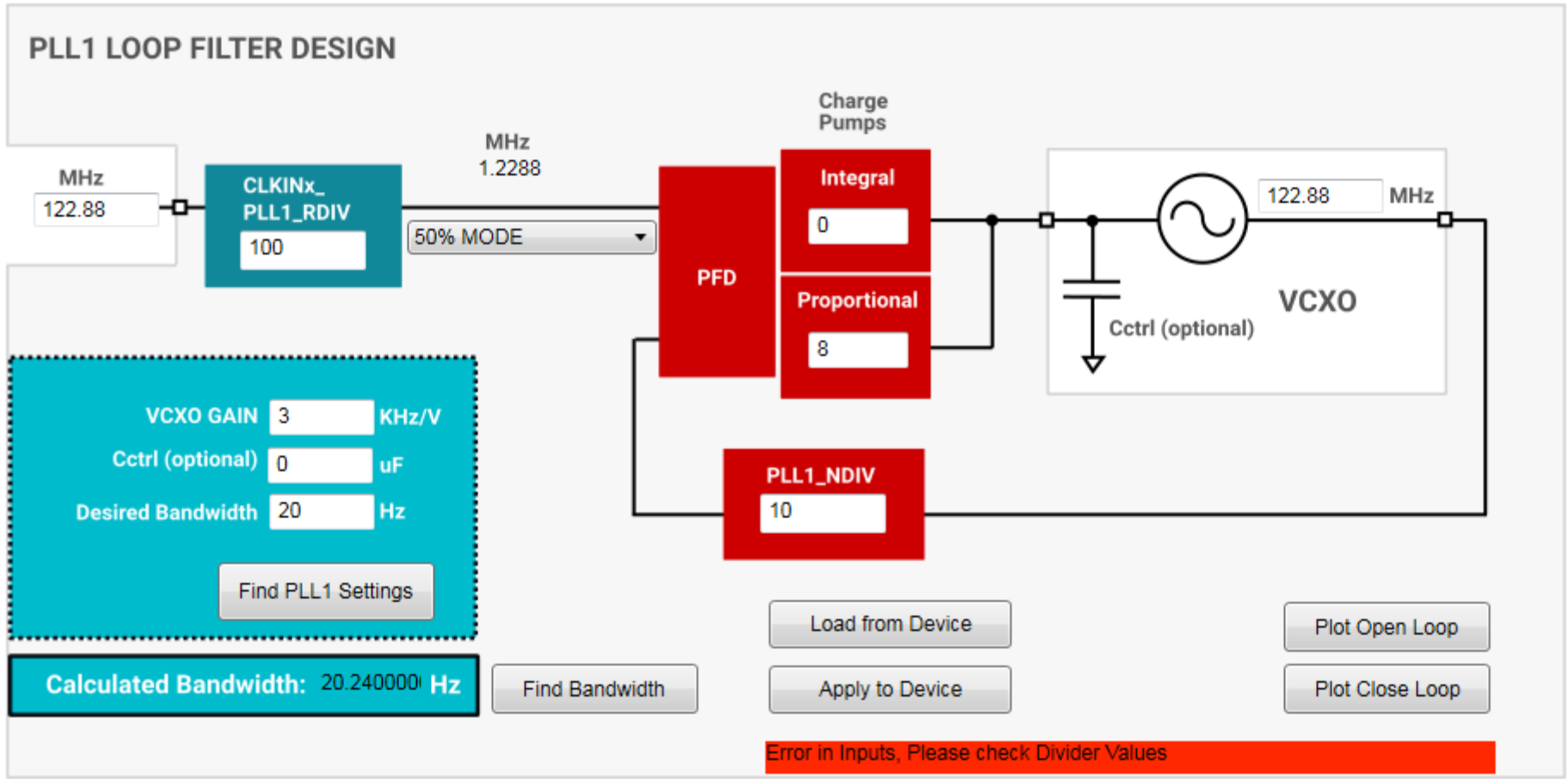
Lock Detection

Window Comparator — PLL1_PD_LD

PLL1_LD WNDW_SIZE 63 ns — PLL1_FAST LOCK

PLL1_LCKDET_BY_32 — /32

PLL1_LOCKDET CYC_CNT 16384


PLL1 LOOP FILTER DESIGN
MHz
122.88
CLKINx_
PLL1_RDIV
100
MHz
1.2288
50% MODE
PFD
Charge
Pumps
Integral
0
Proportional
8
122.88
MHz
VCXO
Cctrl (optional)
PLL1_NDIV
10
VCXO GAIN
3
KHz/V
Cctrl (optional)
0
uF
Desired Bandwidth
20
Hz
Find PLL1 Settings
Calculated Bandwidth: 20.240000 Hz
Find Bandwidth
Load from Device
Apply to Device
Plot Open Loop
Plot Close Loop
Error in Inputs, Please check Divider Values

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