LMK0461x SYSREF Generation

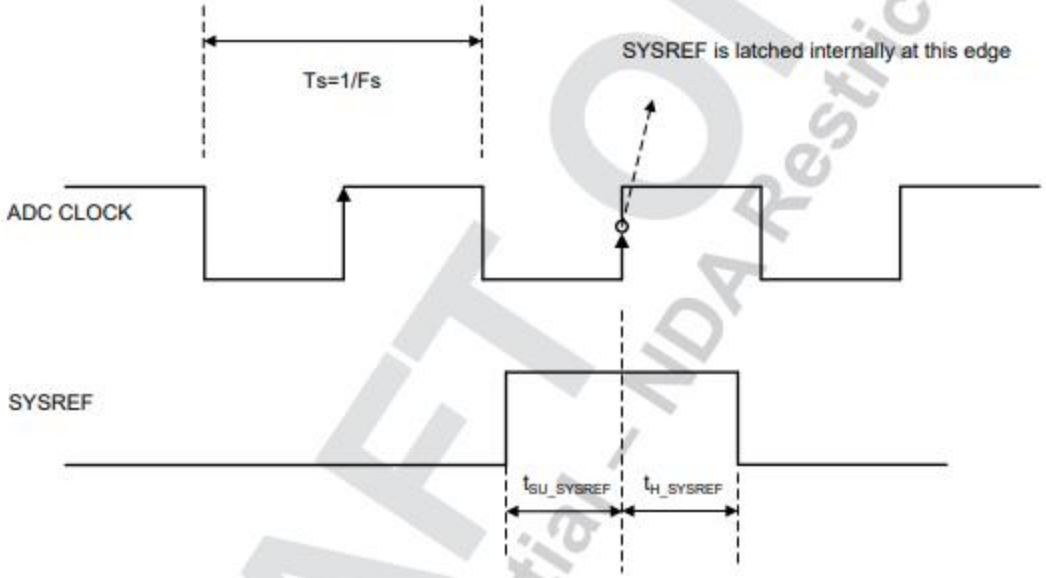


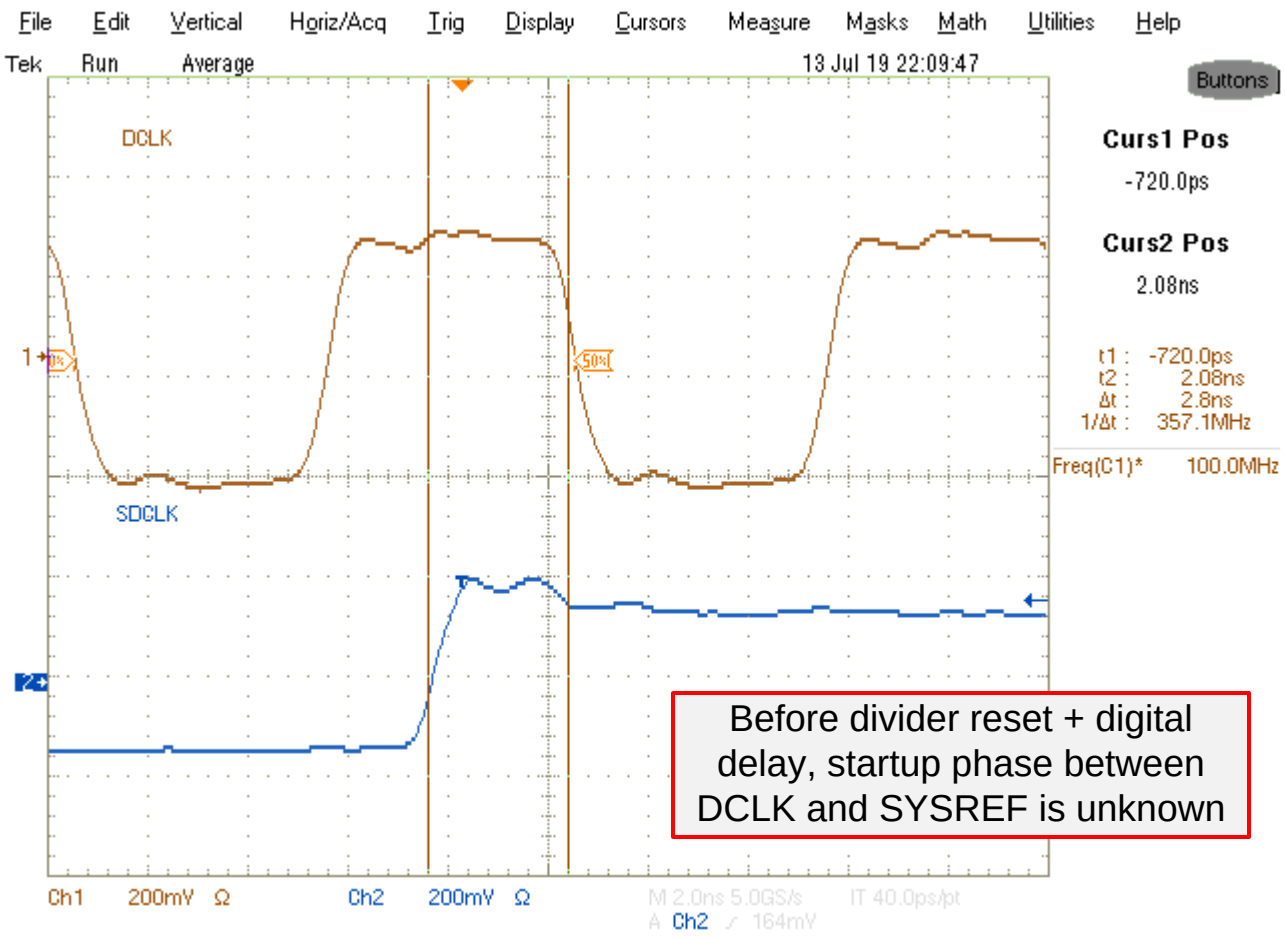
Figure 2. SYSREF Timing

How can we guarantee DCLK-to-SCLK phase to satisfy t_{SU_SYSREF} and t_{H_SYSREF}?

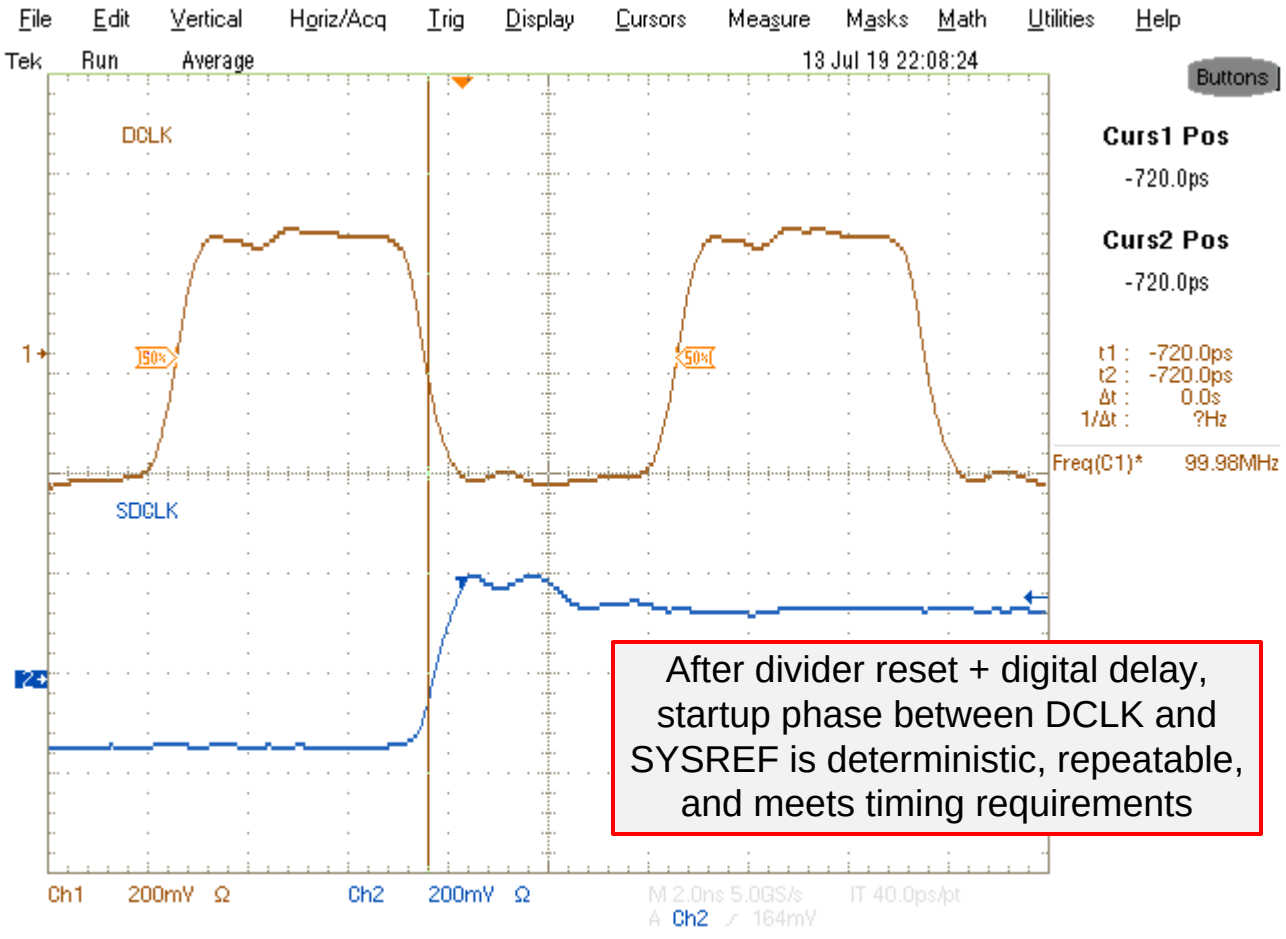
Step 1: Determine digital delay which places rising edge of SYSREF pulse between t_{H_SYSREF} and t_{SU_SYSREF}

Step 2: Set the digital delays and reset dividers through POR or SYNC

After reset, DCLK-to-SYSREF phase is known. SYSREF timing will be correct.



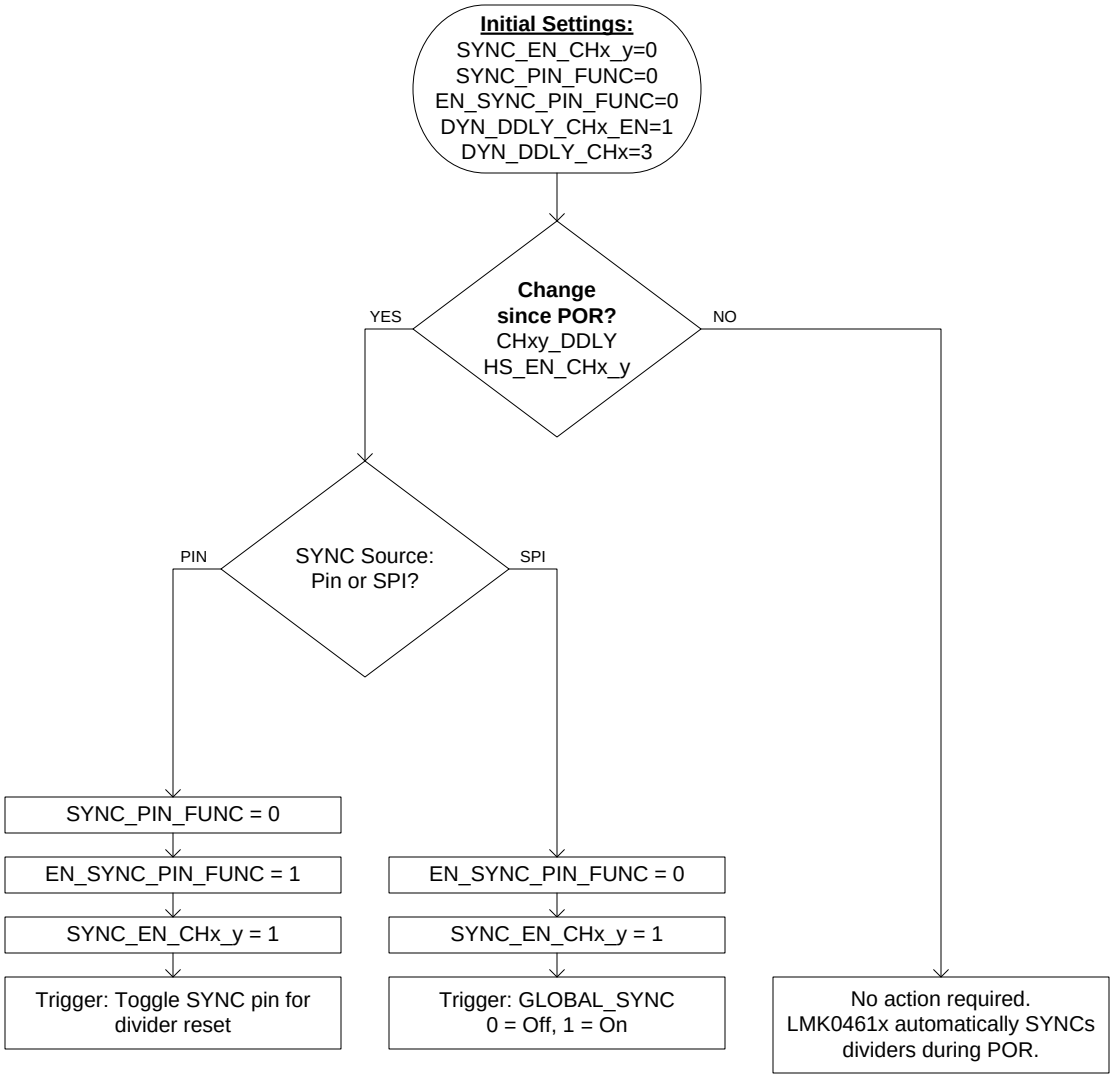
Before divider reset + digital delay, startup phase between DCLK and SYSREF is unknown



After divider reset + digital delay, startup phase between DCLK and SYSREF is deterministic, repeatable, and meets timing requirements

Divider Reset Procedure

Recommended: Since DCLK divide is 10, dynamic digital delay can probably be used to adjust SYSREF edge to correct location. Then just accept POR SYNC.



SYSREF Generation