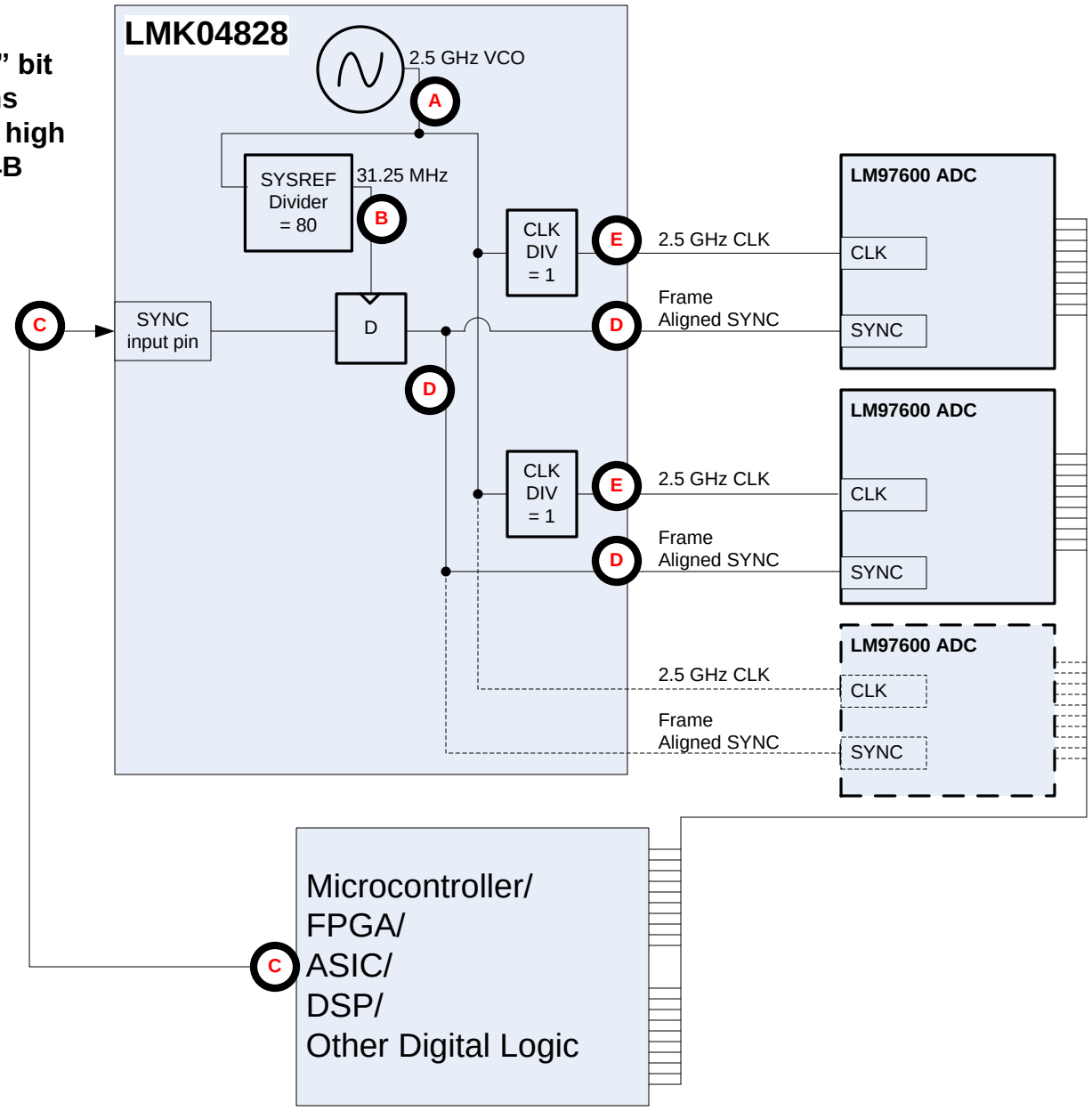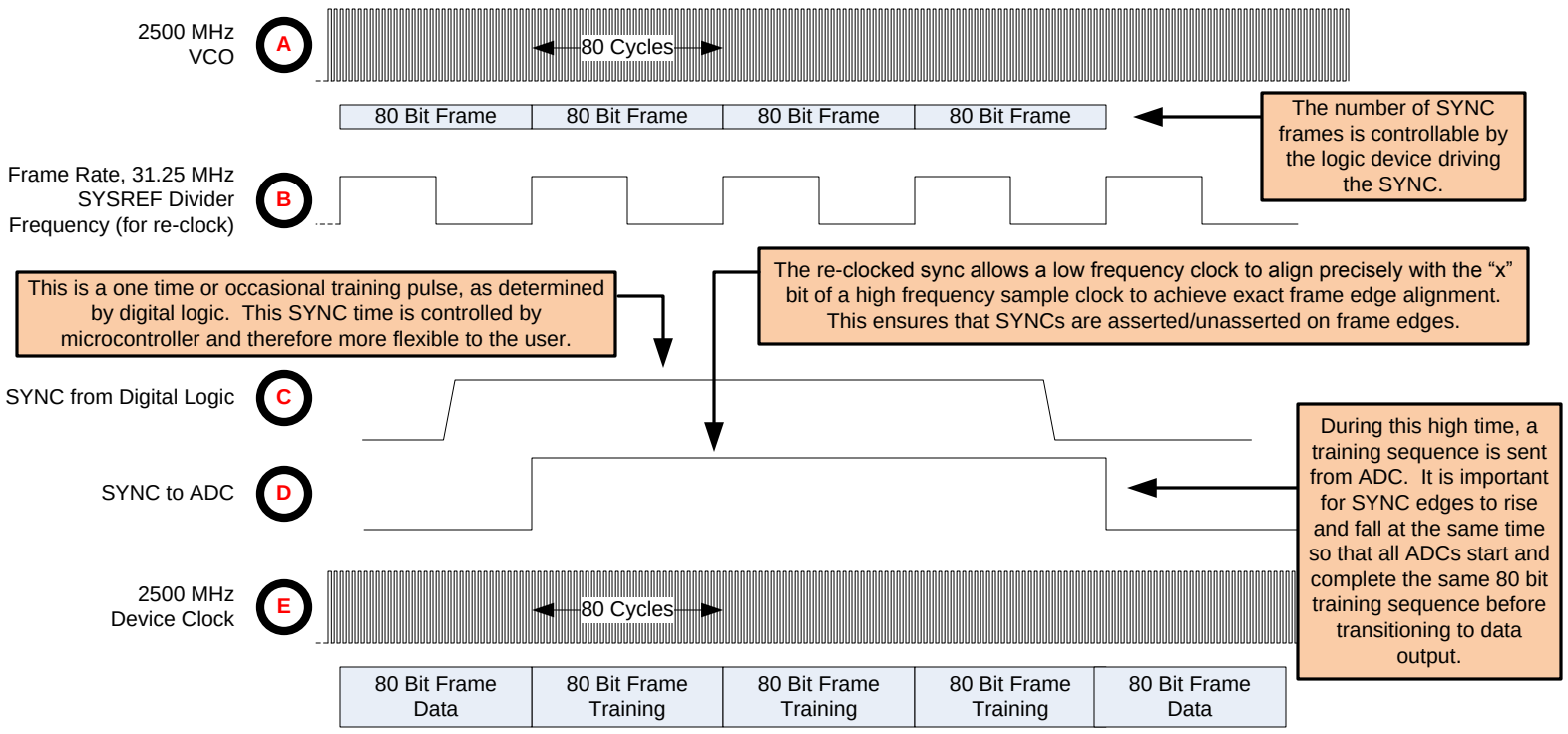Re-clocked sync for enabling complete "x" bit frame training patterns and SYNC of multiple high speed non-JEDEC204B ADCs controlled by external logic device.