LMK04828 to LMK04832 Migration Guide

2021-01-13

Contents

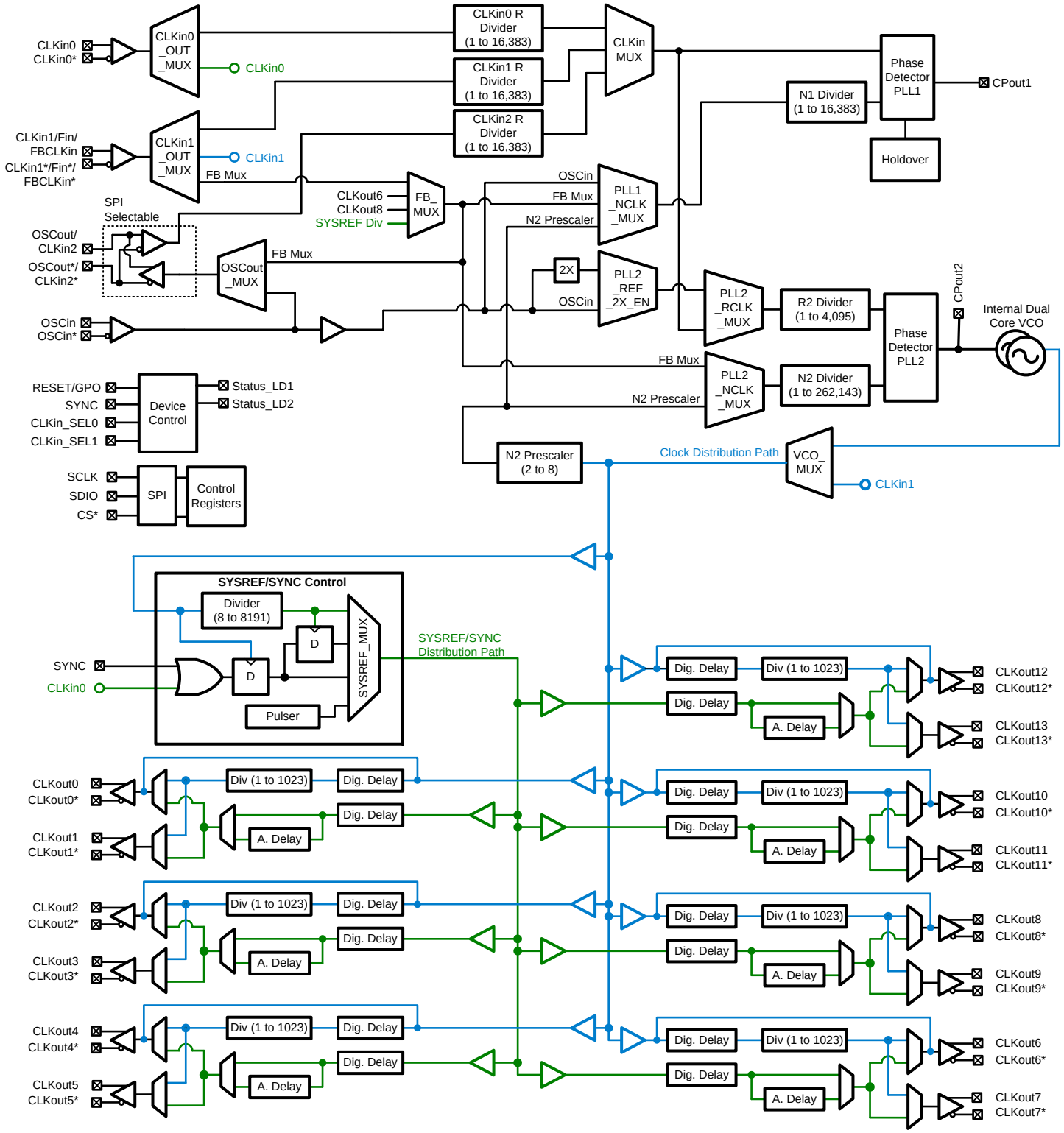
Overview

The LMK04832 is an evolution of the LMK04828 which among other things

- adds CMOS and CML outputs,
- improves CLKin/Holdover selection,
- adds PLL R synchronization

Block Diagram

Note, no direct analog CLKin0 → SYSREF output path via SYSREF_CLKin0_MUX. CLKin0 → SYSREF output is still supported via SYSREF_MUX which will re-clock CLKin0 to Clock Distribution path for tight devclk/sysref alignment at high frequencies.



Programming

Output Section

The biggest changes apply to the clock output section. One change allows the device clock to drive both outputs and the SYSREF to drive both outputs. Accordingly the naming convention of DCLKoutX and SDCLKoutY are dropped. All outputs are now referred to as CLKout#. Bits which correspond to device clock in a channel pair are DCLKX_Y_*. Bits which correspond to the SYSREF clock in a channel pair are SCLKX_Y_*. Bits which only apply to a specific physical clock output are still CLKout#_*.

For the Output Section, the registers repeat every 8 registers for all 7 pairs. This is the same as LMK0482x.

LMK04832A1 Note: DCLKX_Y_PD is swapped with CLKoutX_Y_PD.

Output Pair	CLKout0/1	CLKout2/3	CLKout4/5	CLKout6/7	CLKout8/9	CLKout10/11	CLKout12/13
Registers	0x100 to 0x107	0x108 to 0x10f	0x110 to 0x117	0x118 to 0x11f	0x120 to 0x127	0x128 to 0x12f	0x130 to 0x137

Deleted Field - No longer exists in LMK04832	**New Field** - Did not previously exist in LMK04828	**Redefined** - Functionality has changed or expanded since LMK04828 If name changed, then **name is bolded**	**Displaced** - Same functionality, but displaced from previous location If name changed, then **name is bolded**	**No Change** If name changed, then **name is bolded**

LMK04828 Register Map

D7	D6	D5	D4	D3	D2	D1	D0	
	CLKout0_1_ODL	CLKout0_1_IDL	DCLKout0_DIV[4:0]					0x100
DCLKout0_DDLY_CNTH[3:0](5)				DCLKout0_DDLY_CNTL[3:0](5)				0x101
DCLKout0_DDLYd_CNTH[3:0](5)				DCLKout0_DDLYd_CNTL[3:0](5)				0x102
DCLKout0_ADLY[4:0]					DCLKout0_ADLY_MUX	DCLKout0_MUX[1:0]		0x103
	DCLKout0_HS	SDCLKout1_MUX	SDCLKout1_DDLY[3:0]				SDCLKout1_HS	0x104
			SDCLKout1_ADLY_EN	SDCLKout1_ADLY[3:0]				0x105
DCLKout0_DDLY_PD	DCLKout0_HSg_PD	DCLKout0_ADLYg_PD	DCLKout0_ADLY_PD	CLKout0_1_PD	SDCLKout1_DIS_MODE[1:0]		SDCLKout1_PD	0x106
SDCLKout1_POL	SDCLKout1_FMT[2:0]			DCLKout0_POL	DCLKout0_FMT[2:0]			0x107

LMK04832 Register map

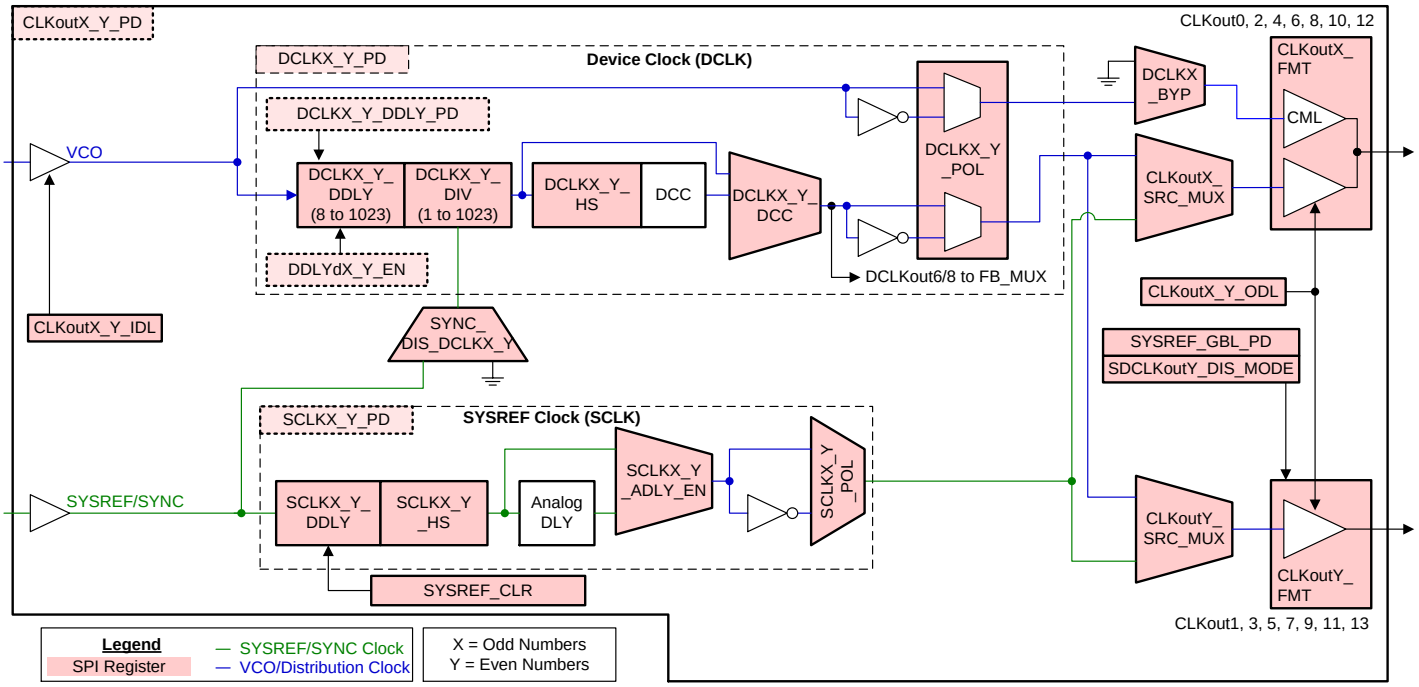
D7	D6	D5	D4	D3	D2	D1	D0	
DCLK0_1_DIV[7:0] (DEF 24)								0x100
DCLK0_1_DDLY[7:0] (DEF 24)								0x101
CLKout0_1_PD	CLKout0_1_ODL	CLKout0_1_IDL	**DCLK0_1_DDLY_PD**	**DCLK0_1_DDLY[9:8] (DEF 0)**		**DCLK0_1_DIV[9:8] (DEF 0)**		0x102
	DCLK0_1_HSg_PD	**CLKout0_SRC_MUX**	**DCLK0_1_PD**	**DCLK0_1_BYP**	**DCLK0_1_DCC**	**DCLK0_1_POL**	**DCLK0_1_HS**	0x103
		CLKout1_SRC_MUX	**SCLK0_1_PD**	**SCLK0_1_DIS_MODE[1:0]**		**SCLK0_1_POL**	**SCLK0_1_HS**	0x104
		SCLK0_1_ADLY_EN	**SCLK0_1_ADLY[4:0] (1 extra bit)**					0x105
				SCLK0_1_DDLY[3:0] (DEF 0)				0x106
CLKout1_FMT[3:0] (1 extra bit)				CLKout0_FMT[3:0] (1 extra bit)				0x107

LMK04828 Field Name	LMK04828 Location	LMK04828 to LMK04832	LMK04832 Location	LMK04832 Field Name	Definition
CLKout0_1_ODL	0x100[6] +n	Displaced	0x102[6] +n	CLKout0_1_ODL	Sets output drive level for clocks; 1 = higher power and lower noise floor.
CLKout0_1_IDL	0x100[5] +n	Displaced	0x102[5] +n	CLKout0_1_IDL	Sets input drive level for clocks; 1 = higher power and lower noise floor.
DCLKout0_DIV	0x100[4:0] +n	Expanded	0x102[1:0] > 0x100[7:0] +n	DCLK0_1_DIV[7:0] DCLK0_1_DIV[9:8]	Divide value (2 to 1023) Use bypass mode for /1.
DCLKout0_ DDLY_CNTH/L	0x101[7:4] / 0x101[3:0] + n	Merged & Expanded	0x102[3:2] > 0x101[7:0] +n	DCLK0_1_DDLY[7:0] DCLK0_1_DDLY[9:8]	Digital delay (2 to 1023)
DCLKout0_ DDLYd_CNTH/L	0x102[7:4] / 0x102[3:0] + n	Deleted	-	-	-
DCLKout0_ADLY	0x103[7:3] + n	Deleted	-	-	-
DCLKout0_ADLY_MUX	0x103[2] + n	Deleted	-	-	-
DCLKout0_MUX	0x103[1:0] + n	Redefined	0x103[3] + n	DCLK0_1_BYP	1: Bypass divider for DevCLK
DCLKout0_MUX	0x103[1:0] + n	Redefined	0x103[2] + n	DCLK0_1_DCC	1: Enable DevCLK Duty cycle correction
DCLKout0_POL	0x107[3] + n	Displaced	0x103[1] + n	DCLK0_1_POL	1: Invert DevCLK polarity
DCLKout0_HS	0x104[6] + n	Displaced	0x103[0] + n	DCLK0_1_HS	1: Enable DevCLK HalfStep (-0.5)
SDCLKout1_MUX	0x104[5] + n	Same	0x104[5] + n	CLKout1_SRC_MUX	Select... 0: Device Clock 1: SYSREF
SDCLKout1_DDLY	0x104[4:1] + n	Same	0x106[3:0] + n	SCLK0_1_DDLY[3:0] (DEF 0)	Set digital delay value for SYSREF clock
SDCLKout1_HS	0x104[0] + n	Same	0x104[0] + n	SCLK0_1_HS	1: Enable SYSREF HalfStep (-0.5)
SDCLKout1_ADLY_EN	0x105[4] + n	Same	0x105[5]	SCLK0_1_ADLY_EN	1: Enable SYSREF Analog Delay
SDCLKout1_ADLY	0x105[3:0] + n	Expanded	0x105[4:0] + n	SCLK0_1_ADLY[4:0] (1 extra bit)	0..15: Analog delay in 25 ps steps
DCLKout0_DDLY_PD	0x106[7] + n	Displaced	0x102[4] + n	DCLK0_1_DDLY_PD	1: Device Clock Digital Delay powerdown
DCLKout0_HSg_PD	0x106[6] + n	Same	0x103[6] + n	DCLK0_1_HSg_PD	0: Enable DDLY half-step glitchless
DCLKout0_ADLYg_PD	0x106[5] + n	Deleted	-	-	-
DCLKout0_ADLY_PD	0x106[4] + n	Deleted	-	-	-
CLKout0_1_PD	0x106[3] + n	Same	0x102[7] + n	CLKout0_1_PD	1: Power down the entire clock buffer
SDCLKout1_DIS_MODE	0x106[2:1] + n	Same	0x104[3:2] + n	SCLK0_1_DIS_MODE	0..3: Set disable mode for when SYSREF_GBL_PD is = 1 or otherwise.
SDCLKout1_PD	0x106[0] + n	Same	0x104[4] + n	SCLK0_1_PD	1: Power down the SYSREF clock (only DevCLK used)
SDCLKout1_POL	0x107[7] + n	Displaced	0x104[1]	SCLK0_1_POL	1: Invert the SYSREF clock
SDCLKout1_FMT	0x107[6:4] + n	Expanded	0x107[7:4] + n	CLKout1_FMT[3:0]	Set CLKout1 clock format
DCLKout0_FMT	0x107[2:0] + n	Expanded	0x107[3:0] + n	CLKout0_FMT[3:0]	Set CLKout0 clock format
-	-	New	0x103[5] + n	CLKout0_SRC_MUX	Select... 0: Device Clock 1: SYSREF
-	-	New	0x103[4] + n	DCLK0_1_PD	1: Power down Device Clock (only SYSREF used)

CLKout#_FMT has been updated with CML format for all outputs, and CMOS format for all odd-numbered outputs (as well as CLKout8/10). CMOS format polarity is reversed/inverted on some outputs.

Field Value	Decode (CLKout 1, 7, 10, 11)	Decode (CLKout 3, 5, 8, 9, 13)	Decode (CLKout0, 2, 4, 6, 12)
0	Powerdown	Powerdown	Powerdown
1	LVDS	LVDS	LVDS
2	HSDS 6 mA	HSDS 6 mA	HSDS 6 mA
3	HSDS 8 mA	HSDS 8 mA	HSDS 8 mA
4	LVPECL (1.6 Vpp)	LVPECL (1.6 Vpp)	LVPECL (1.6 Vpp)
5	LVPECL (2 Vpp)	LVPECL (2 Vpp)	LVPECL (2 Vpp)
6	LCPECL	LCPECL	LCPECL
7	CML 16 mA	CML 16 mA	CML 16 mA
8	CML 24 mA	CML 24 mA	CML 24 mA
9	CML 32 mA	CML 32 mA	CML 32 mA
10	CMOS **(Off/Inv)**	CMOS **(Off/Norm)**	-
11	CMOS **(Norm/Off)**	CMOS **(Inv/Off)**	-
12	CMOS **(Inv/Inv)**	CMOS **(Norm/Norm)**	-
13	CMOS **(Inv/Norm)**	CMOS **(Norm/Inv)**	-
14	CMOS **(Norm/Inv)**	CMOS **(Inv/Norm)**	-
15	CMOS **(Norm/Norm)**	CMOS **(Inv/Inv)**	-

LMK04832 CLKout Diagram



Dynamic Digital Delay

As there are no more dynamic digital delay adjustment registers in the CLKout group registers, DDLYd_STEP_CNT is used to set the global number of VCO cycles slipped.

LMK04828 Field Name	LMK04828 Location	LMK04828 to LMK04832	LMK04832 Location	LMK04832 Field Name	Definition
DDLYd_STEP_CNT	0x142[4:0]	Expanded	0x142[7:0]	DDLYd_STEP_CNT[7:0]	Number of steps to take for dynamic digital delay slip 0 = No adjust; 1 = 1 Step, 2 = 2 Steps, ..., 255 = 255 Steps

PLL1 and PLL2 R Divider Synchronization

Register 0x145 can be skipped or programmed to 0x00 if PLL R divider synchronization is not needed.

LMK04828 Field Name	LMK04828 Location	LMK04828 to LMK04832	LMK04832 Location	LMK04832 Field Name	Definition
Fixed 1	0x145[0]	Deleted	-	-	-
Fixed 1	0x145[1]	Deleted	-	-	-
Fixed 1	0x145[2]	Deleted	-	-	-
Fixed 1	0x145[3]	Deleted	-	-	-
Fixed 1	0x145[4]	Deleted	-	-	-
Fixed 1	0x145[5]	Deleted	-	-	-
Fixed 1	0x145[6]	Deleted	-	-	-
Fixed 0	0x145[7]	Deleted	-	-	-
-	-	New	0x145[6]		Relating to PLL 1 & 2 R counter SYNC
		New	0x145[5]		Relating to PLL 1 & 2 R counter SYNC
		New	0x145[4]		Relating to PLL 1 & 2 R counter SYNC
		New	0x145[3]		Relating to PLL 1 & 2 R counter SYNC

Clock Input Selection

LMK04828 Field Name	LMK04828 Location	LMK04828 to LMK04832	LMK04832 Location	LMK04832 Field Name	Definition
CLKin_SEL_MODE	0x147[6:4]	Redefined	0x146[7]	CLKin_SEL_PIN_EN	Setting = 1 enables pin control
CLKin_SEL_POL	0x147[7]	Displaced/ Renamed	0x146[6]	CLKin_SEL_PIN_POL	0: Normal CLKin_SEL 1: Invert the CLKin_SEL pins for decode purposes when using pins to select active clock. Also impacts LOS state defined from external pins mode.
-	-	New	0x147[7]	CLKin_SEL_AUTO_REVERT_EN	Causes clock to switch to lowest number clock according to auto mode clock state machine. But this is lowest enabled clock input with active clock by LOS definition.
CLKin_SEL_MODE	0x147[6:4]	Redefined	0x147[6]	CLKin_SEL_AUTO_EN	Enables active clock to be set by input clock state machine
CLKin_SEL_MODE	0x147[6:4]	Redefined	0x147[5:4]	CLKin_SEL_MANUAL	Clock Input Select 0 = CLKin0 1 = CLKin1 2 = CLKin2 3 = Holdover

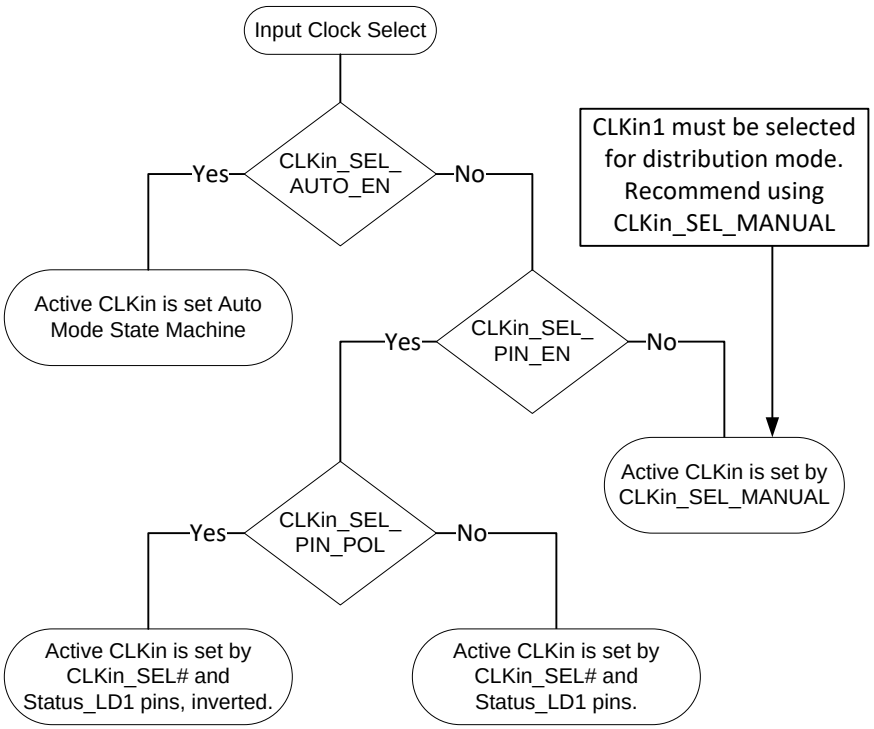


Figure 1 – Yes/No correspond to bit Set/Clear

Holdover

LMK04828 Field Name	LMK04828 Location	LMK04828 to LMK04832	LMK04832 Location	LMK04832 Field Name	Definition
HOLDOVER_HITLESS_SWITCH	0x150[1]	Redefined	0x150[5]	HOLDOVER_EXIT_MODE	0: Exit holdover based on LOS. 1: Stay in holdover based on DLD lock window. (Legacy holdover exit)
HOLDOVER_PLL1_DET	0x150[4]	-	0x150[4]	HOLDOVER_PLL1_DET	1: PLL1 DLD going low will cause a clock switch (only used in auto mode)
-	-	New	0x150[3]	LOS_EXTERNAL_INPUT	Overrides internal LOS mode. LOS_EN = 1 is still required. CLKin_SEL0 → CLKin0 LOS CLKin_SEL1 → CLKin1 LOS Status_LD1 → CLKin2 LOS When CLKin_PINS_POL = 0, Setting CLKin# LOS to 1 indicates loss of clock on that input.
-	-	New	0x150[1]	CLKin_SWITCH_CP_TRI	Tri-states PLL1 charge pump during switching.
HOLDOVER_EN Default = 1	0x150[0]	Changed Default	0x150[0]	HOLDOVER_EN Default = 0	Default state of this bit is 0.
-	-	New	0x15e[4:0]	HOLDOVER_EXIT_NADJ	When HOLDOVER_EXIT_MODE = 0 and holdover exits using LOS state: PLL1_R and PLL1_N are reset. The HOLDOVER_EXIT_NADJ signed 2s complement number is added to PLL1_N for reset value. However, ppm accuracy detect of input clock is lost. If HOLD_EXIT_MODE = 1, then same exit time as in LMK04828 applies and PLL1_N_ADJUST has no effect.

LOS

LOS Threshold change: below the specified frequency, LOS will assert. Higher frequencies allow for faster switching response.

LOS_TIMEOUT, 0x14b[7:6]		
Value	**LMK04828**	**LMK04832**
0 (0x00)	370 kHz	5 MHz
1 (0x01)	2.1 MHz	25 MHz
2 (0x02)	8.8 MHz	100 MHz
3 (0x03)	22 MHz	200 MHz

LOS can now control switching into/out of holdover and between clocks.

LOS is supported in clock distribution mode. LMK04828 did not support LOS for clock distribution mode.

LOS remains asserted until 4 valid clock pulses are received. LMK04828 would de-assert after one valid input clock pulse.

Other

LMK04828 Field Name	LMK04828 Location	LMK04828 to LMK04832	LMK04832 Location	LMK04832 Field Name	Definition
SYSREF_CLKin0_MUX	0x139[2]	Deleted	-	-	Direct analog bypass of CLKin0 to outputs is not possible with LMK04832.
PLL1_R_DLY	0x15E[5:3]	Deleted	-	-	PLL1 R Delay
PLL1_N_DLY	0x15E[2:0]	Deleted	-	-	PLL1 N Delay
SYSREF_REQ_EN	0x16A[6]	Displaced	0x139[4]	SYSREF_REQ_EN	No behavioral change from LMK04828.
PLL2_LF_R3	0x16C[2:0]	Deleted	-	-	Integrated R3 is now fixed
PLL2_LF_R4	0x16C[5:3]	Deleted	-	-	Integrated R4 is now fixed
PLL2_LF_C3	0x16D[3:0]	Deleted	-	-	Integrated C3 is now fixed
PLL2_LF_C4	0x16D[7:4]	Deleted	-	-	Integrated C4 is now fixed
<no name>	0x171[7:0]	Deleted	-	-	No longer required to program
<no name>	0x172[7:0]	Deleted	-	-	No longer required to program
RB_PLL1_LD_LOST	0x182[2]	Displaced	0x183[3]	RB_PLL1_LD_LOST	No behavioral change from LMK04828.
RB_PLL1_LD	0x182[1]	Displaced	0x183[2]	RB_PLL1_LD	No behavioral change from LMK04828.
CLR_PLL1_LD_LOST	0x182[0]	Displaced	0x182[1]	CLR_PLL1_LD_LOST	No behavioral change from LMK04828.
RB_PLL2_LD_LOST	0x183[2]	Displaced	0x183[1]	RB_PLL2_LD_LOST	No behavioral change from LMK04828.
RB_PLL2_LD	0x183[1]	Displaced	0x183[0]	RB_PLL2_LD	No behavioral change from LMK04828.
CLR_PLL2_LD_LOST	0x183[0]	Displaced	0x182[0]	CLR_PLL2_LD_LOST	No behavioral change from LMK04828.
SPI_LOCK	0x1FFD to 0x1FFF	Compressed and Displaced	0x555	SPI_LOCK	Writing SPI_LOCK to a value > 0 causes SPI transactions to be disabled for all registers except 0x555. SPI_LOCK cannot be read back.
-	-	Added	0x169[0]	PLL2_DLD_EN	PLL2 DLD circuitry is enabled when the PLL2 DLD is used to provide an output to a lock detect status pin. PLL2_DLD_EN allows enabling the PLL2 DLD circuitry without needing to provide PLL2_DLD to a status pin. This enables PLL2 DLD status to be read back using SPI while allowing the status pins to be used for other purposes. 0: PLL2 DLD circuitry is only on if PLL2 DLD or PLL1 + PLL2 DLD signal is output from a Status_LD_MUX 1: PLL2 DLD circuitry is forced on.

New LMK04832 Features

CLKinX for PLL2 reference

The actively selected reference clock, CLKinX, can now also be used as a reference for PLL2.
PLL2 doubler is only available for OSCin, and will not double CLKinX inputs.

LMK04828 Field Name	LMK04828 Location	LMK04828 to LMK04832	LMK04832 Location	LMK04832 Field Name	Definition
-	-	New	0x13F[7]	PLL2_RCLK_MUX	0: Select OSCin for PLL2 reference 1: Select CLKinX for PLL2 reference

PLL2 N-Prescaler for PLL1 N-divider

In addition to the previously available choices of OSCin and FB_MUX, the output of the PLL2 N-Prescaler may be used in the feedback path to PLL1.

LMK04828 Field Name	LMK04828 Location	LMK04828 to LMK04832	LMK04832 Location	LMK04832 Field Name	Definition
PLL1_NCLK_MUX	0x13F[3]	Expanded	0x13F[4:3]	PLL1_NCLK_MUX	Selects the input to the PLL1 N Divider. 0: OSCin 1: Feedback Mux 2: PLL2 Prescaler 3: Reserved
PLL2_NCLK_MUX	0x13F[4]	Displaced	0x13F[5]	PLL2_NCLK_MUX	Selects the input to the PLL2 N Divider. 0: PLL2 Prescaler 1: Feedback Mux

SYNC Bypass

SYNC pin input path has been improved for performance to assist in maximum setup and hold time by allowing the SYNC signal from pin 6 to bypass SYNC_POL and SYNC_MODE by setting 0x139[3] = 1

LMK04828 Field Name	LMK04828 Location	LMK04828 to LMK04832	LMK04832 Location	LMK04832 Field Name	Definition
-	-	New	0x139[3]	SYNC_BYPASS	Bypass SYNC_POL and SYNC_MODE for PLL1 R or PLL2 R divider reset.

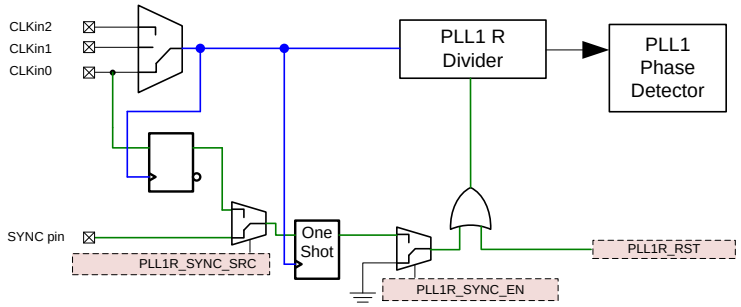
PLL1 R Sync

SYNC pin (pin 6) or CLKin0 (pins 37/38) can be used to reset PLL1 R.

To utilize the reset for the PLL1 R divider circuit, first set PLL1R_SYNC_EN = 1 and configure PLL1R_SYNC_SRC to select either SYNC pin or CLKin0 as the divider reset signal. The PLL1 R divider is then armed for reset using the PLL1R_RST control, by toggling 0x177[5] = 1 momentarily. PLL1 will remain unlocked until a rising edge is sent on the SYNC pin or CLKin0. The rising edge must meet setup and hold time.

The SYNC_POL bit has no effect on SYNC polarity for PLL1 R synchronization.

LMK04828 Field Name	LMK04828 Location	LMK04828 to LMK04832	LMK04832 Location	LMK04832 Field Name	Definition
-	-	New	0x145[6]	PLL1R_SYNC_EN	Enable synchronization for PLL1 R divider.
-	-	New	0x145[5:4]	PLL1R_SYNC_SRC	Selectable source for PLL1 R divider synchronization: 0: Reserved 1: SYNC Pin 2: CLKin0 3: Reserved
-	-	New	0x177[5]	PLL1R_RST	When set, PLL1 R divider will be held in reset. PLL1 will be unlocked while PLL1R_RST=1.



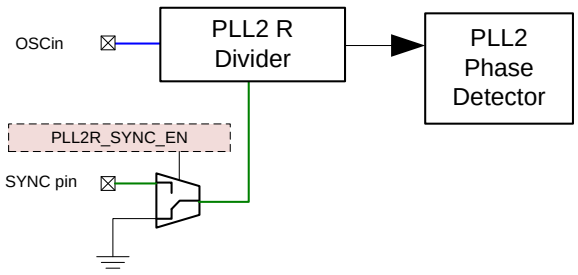
PLL2 R Sync

SYNC pin (pin 6) can be used to reset PLL2 R. (CLKin0 cannot be used).

Must meet setup and hold time. When PLL2R_SYNC_EN = 1, SYNC pin asserted will hold divider in reset until released.

The SYNC_POL bit has no effect on SYNC polarity for PLL1 R synchronization.

LMK04828 Field Name	LMK04828 Location	LMK04828 to LMK04832	LMK04832 Location	LMK04832 Field Name	Definition
-	-	New	0x145[3]	PLL2R_SYNC_EN	Enable synchronization for PLL2 R divider. Synchronization for PLL2 R always comes from the SYNC pin.

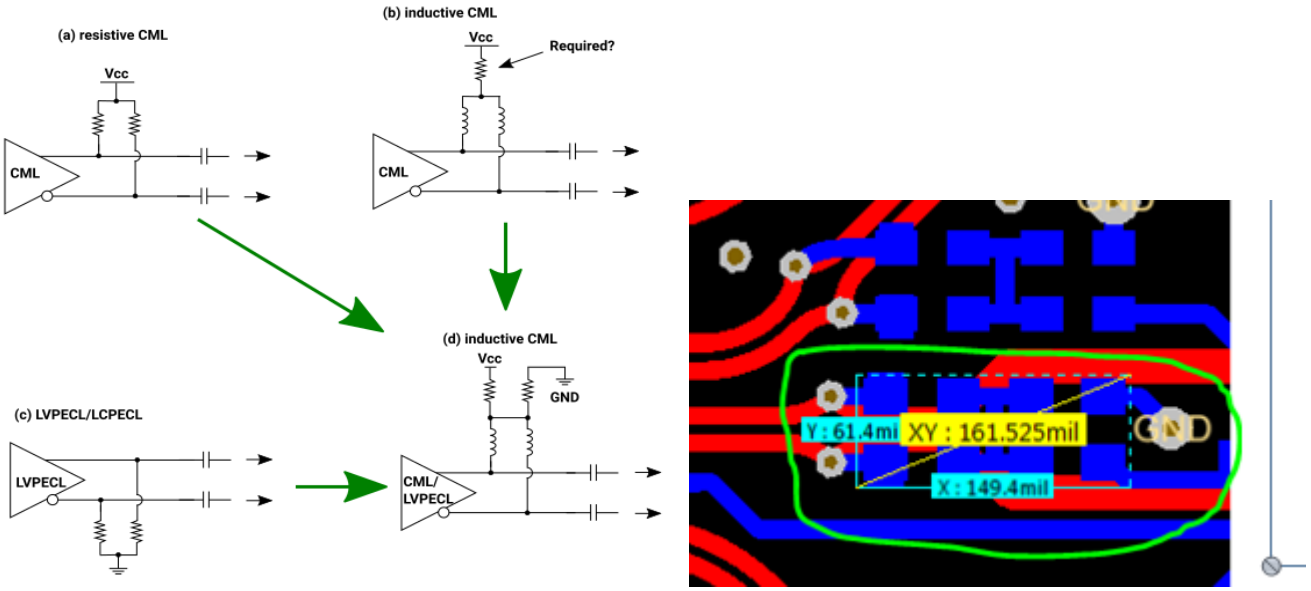


CML

CML outputs are added new to LMK04832. CML outputs are intended to provide an output format suitable for directly outputting the VCO frequency. They have 3 programmable format options: **CML 16 mA**, **CML 24 mA**, or **CML 32 mA**.

All odd-numbered outputs (1, 3, 5, 7, 9, 11, 13) have CML output formats available for standard use. Even-numbered outputs (0, 2, 4, 6, 8, 10, 12) cannot use the CML output formats unless the output is in high-performance bypass mode, and in high-performance bypass mode even-numbered outputs can only use CML output formats. Note that this high-performance bypass mode is different from using the CML output format with a divider set to 1: in high-performance bypass mode, the channel divider, digital delay, and Device Clock/SYSREF mux are bypassed on the even-numbered output. For optimal performance, the digital delay and divider blocks are disabled; when even-numbered outputs are in high-performance bypass mode, odd-numbered outputs can only be used with the SYSREF source. If high-performance bypass mode is active on CLKout6 or CLKout8, these outputs cannot be used as sources for the FB_MUX in zero-delay mode. CLKoutX_Y_IDL and DCLK0_1_POL effects are still applied to the high-performance bypass mode outputs.

If high-performance bypass mode is used, or if CML output format is used, TI recommends option (b) or option (d) below with 68-nH inductors and a common 20-Ω pull-up resistor. Option (b) is recommended when the design exclusively uses CML format. Option (d) is a flexible configuration that allows the use of both CML with common pull-up, or LVPECL with common 0-Ω pull-down, depending on the populated components. Possible layout implementation is shown to right.



0x103[3] DCLKX_Y_BYP in LMK04828 → DCLKX_BYP in LMK04832

LVDS/HSDS Shunt Resistor Omitted

For LMK04828 outputs used with AC-coupled LVDS/HSDS format, 560-Ω shunt resistors are required between P/N terminals on the output to create a DC-bias path in the LVDS/HSDS driver on startup, in addition to standard 100-Ω termination. In the LMK04832, the LVDS/HSDS driver circuit no longer requires a shunt resistor for startup biasing. Proper 100-Ω differential termination is still required.