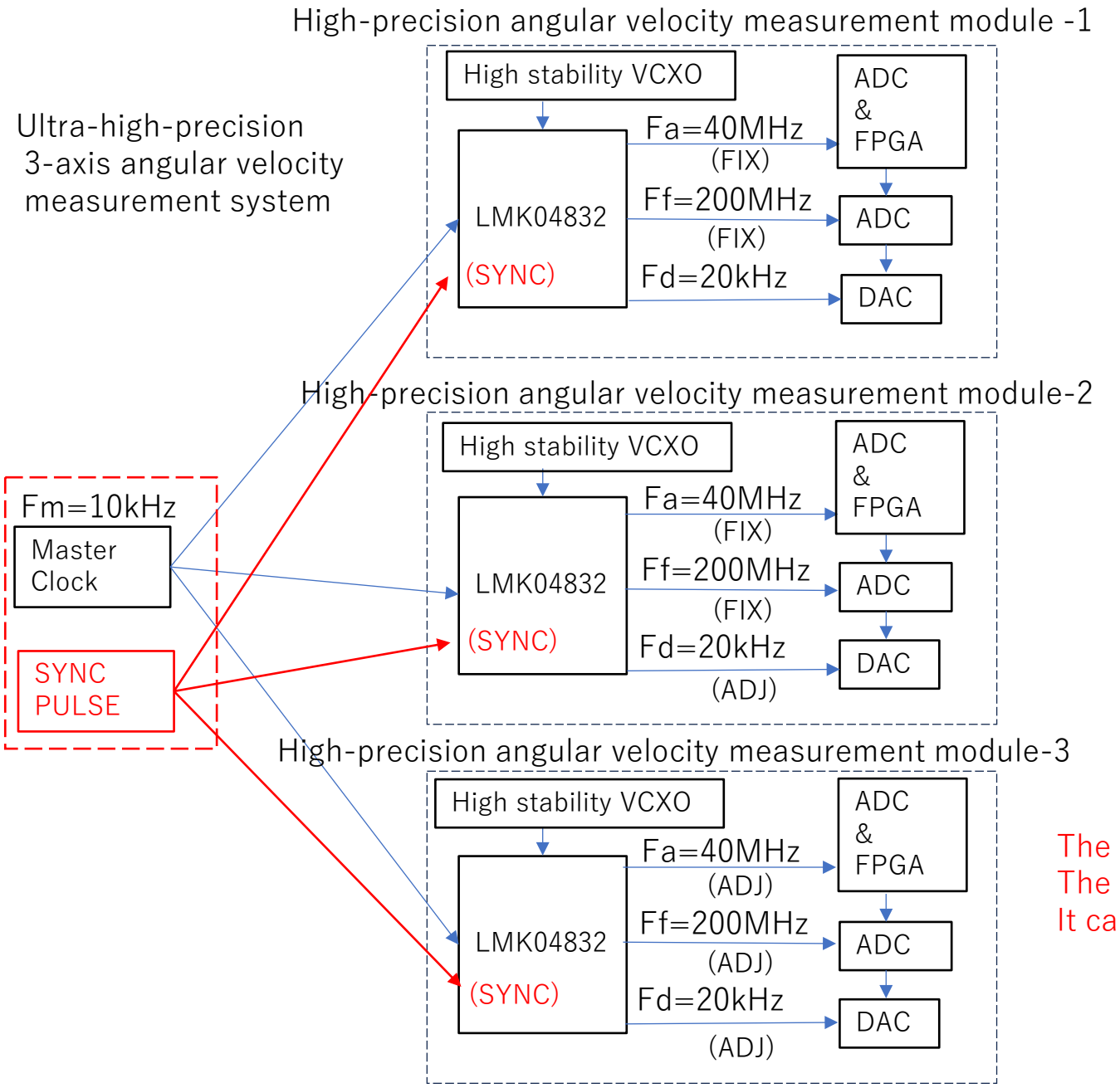
Multiple Synchronous Clock Generation 2025.11.30 Intermind Inc.



All ADC, FPGA, and DAC clocks must be synchronized.
The diagram on the left shows the initial

values.Fa=40MHz, Ff=200MHz are fixed.
10kHz × 4000=4MHz. 10kHz × 20000=200MHz.
Fd is variable ± in approximately 10Hz steps.
The clocks to the ADC, FPGA, and DAC must have low jitter.
The above are the conditions.

Fd=20kHz ± ADJ
40MHz/2000=20.00kHz.
40MHz/2001=19.99kHz.
40MHz/1999=20.01kHz.

The outputs of three LMK04832 are synchronized with a SYNC pulse.
The three ADCs and FPGA are synchronized with the SYNC pulse.
It can be done by synchronizing once at startup.