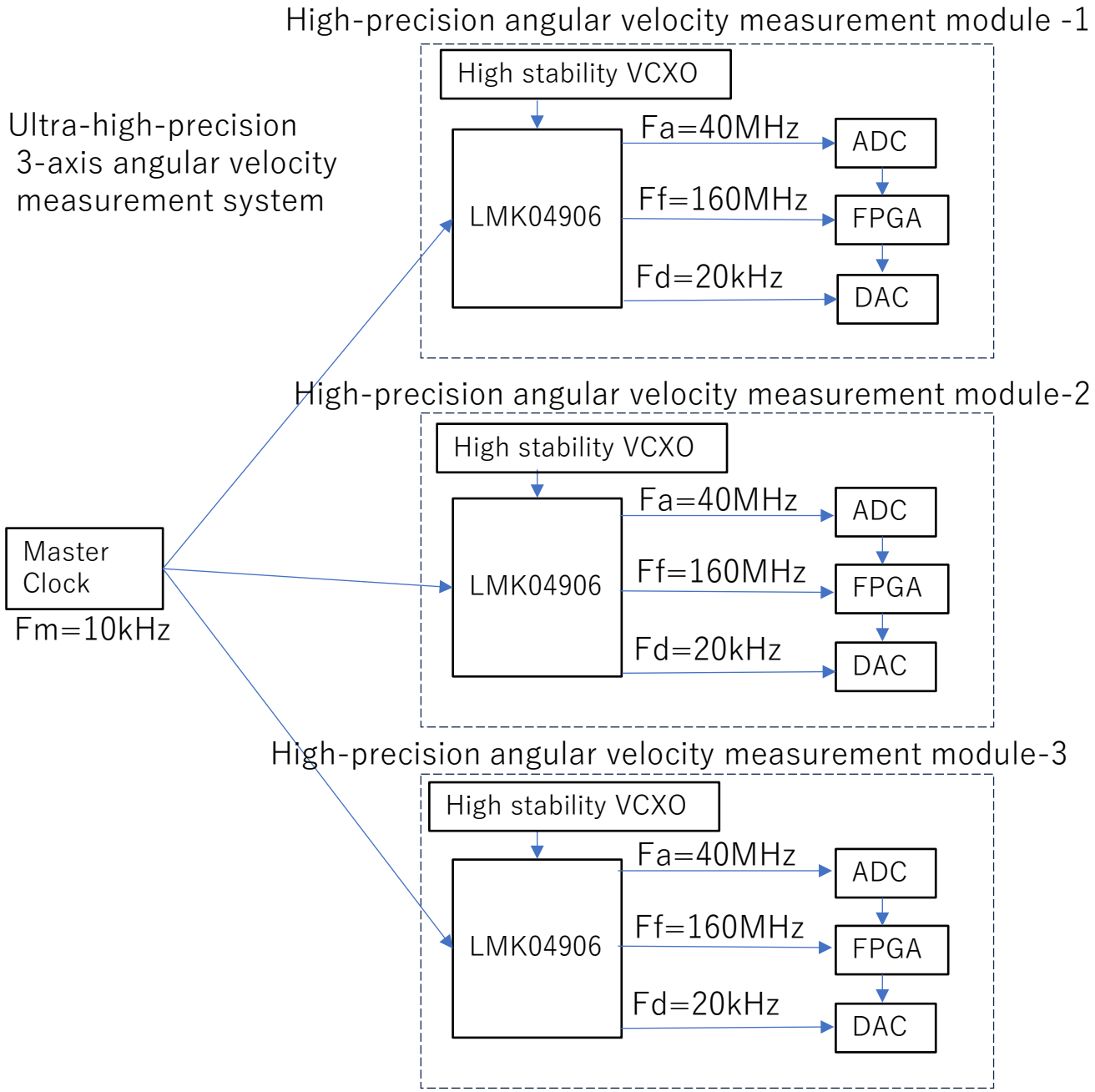
Multiple Synchronous Clock Generation 2025.11.18 Intermind Inc.



All ADC, FPGA, and DAC clocks must be synchronized.
The diagram on the left shows the initial

values.Fa=40MHz, Ff=160MHz are fixed.
Fd is variable ± in approximately 5Hz steps.
The clocks to the ADC, FPGA, and DAC must have low jitter.
The above are the conditions.

Use the LMK04906 to vary Fd.
To do this, set the LMK04906's PLL.
However, do not change Fa=40MHz and Ff=160MHz.
For example, Fd=20kHz×8000=160MHz,
÷4=40MHz.Fd=20.005kHz×7998=160MHz,
÷4=40MHz.Fd=19.995kHz×8002=160MHz,
÷4=40MHz.However, this cannot be achieved with Fm fixed at

10 kHz.Therefore, the Fm frequency must be changed by the same amount as Fd is changed.
For example, when Fd=20.005 kHz, Fm=10.0025 kHz.
When Fd=19.995 kHz, Fm=19.9975 kHz.

(1) A high-stability VCXO is required for each LMK04906?

(2) Is this type of usage possible with the LMK04906?

(3) Is the LMK04906 optimal, or are there other recommended PLL devices?

Register settings for the LMK04906 are made using an FPGA or a separate external microcontroller (not shown in this diagram).