

LMK05318B DPLL REF Lock Testing

CTS Apps

Test Setup

- PRIREF/SECREF center frequency = 80566406 Hz
- Shifting input frequency:
 - +/- 20 ppm
 - +/- 40 ppm
- Procedure:
 - Change input frequency by changing SigGen input to PRIREF/SCREF, the output would follow this change when in lock.
 - No need to adjust PRIREF/SECREF on TICS Pro software and recalculate DPLL settings for frequency shifting.

Status Page

- While shifting the input reference, the output will follow the shift as it stays in lock.
- LOPL_DPLL and LOFL_DPLL are low.

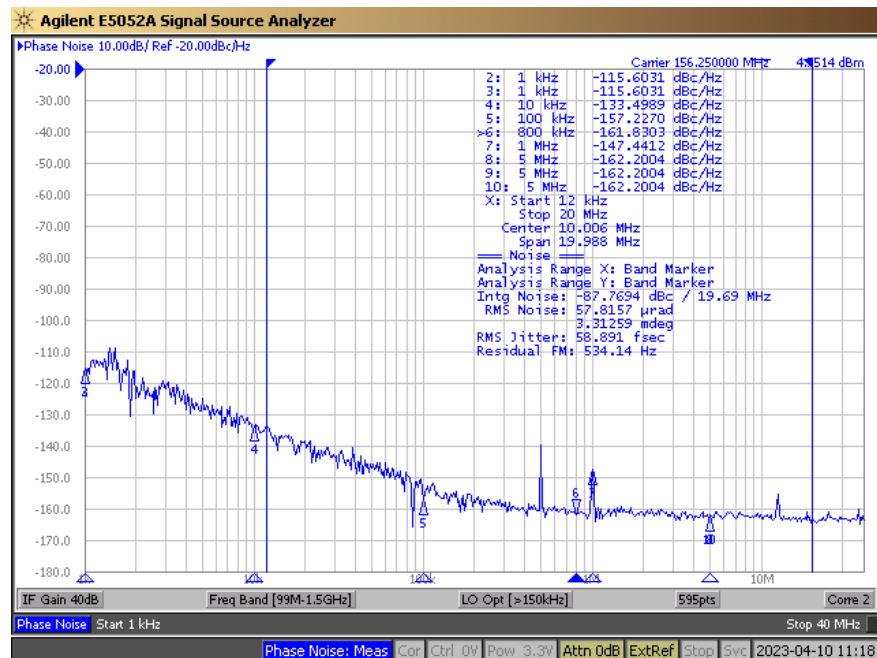
The screenshot displays the 'Status Page' configuration interface. At the top, there is a 'Read Status' button and a 'Live Status Bits' section. The main area is divided into several panels:

- INTR Source Live Status (read only):** A list of checkboxes for various status bits, including LOS_FDET_XO, LOL_PLL1, LOL_PLL2, LOS_XO, LOPL_DPLL, LOFL_DPLL, HIST, HLDQVR, REFSWITCH, LOR_MISSCLK, LOR_FREQ, and LOR_AMP.
- INTR Flag Polarity:** A section with a legend (0 = Flag on low level, 1 = Flag on high level) and checkboxes for the same status bits as the source section.
- INTR Sticky Status (Uncheck to clear):** A section with a 'Clear All Flags' button and checkboxes for the same status bits.
- INTR Status Mask:** A section with a legend (0 = Disable Mask, 1 = Enable Mask) and checkboxes for the same status bits.
- Registers interacting with status bits:** A section with checkboxes for XO_FDET_BYP.
- Other PLL Status Registers:** A section with checkboxes for BAW_LOCK, PLL1_VM_INSIDE, and PLL2_VM_INSIDE.
- Reference Validated?:** A section with checkboxes for PRIREF_VALSTAT and SECREF_VALSTAT, and a note: 'DPLL will not lock until a reference is validated.'
- Active Reference/Holdover:** A dropdown menu currently showing 'PRIREF'.

At the bottom, there are configuration options for Status0 pin, Status1 pin, and GPIO2 pin, all set to 'CMOS'. There are also dropdowns for STAT0_SEL (DPLL Loss of Lock (LOFL)) and STAT1_SEL (DPLL Holdover Active).

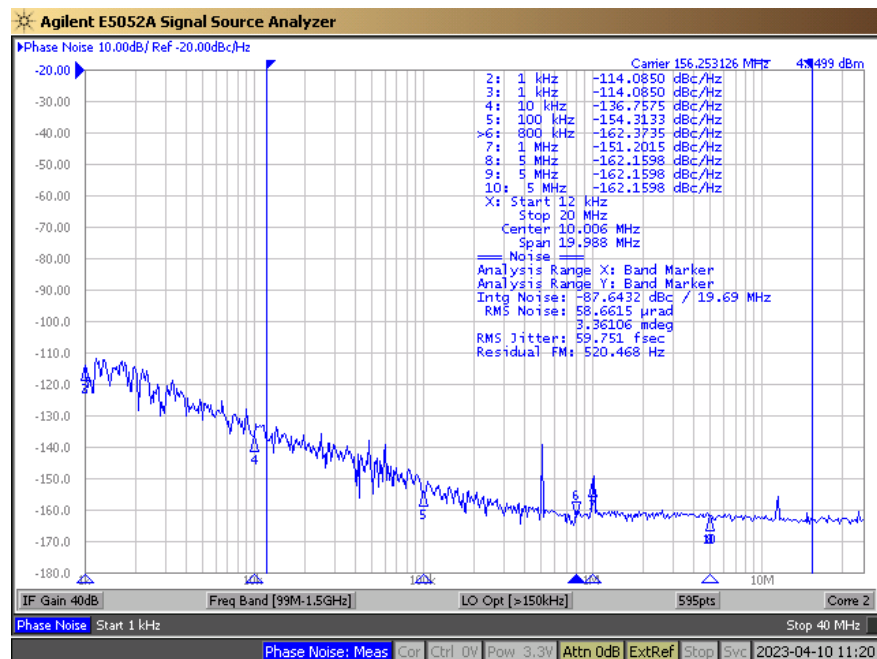
PRIFREF/SECREF = 80566406 Hz

- OUT0 156.25 MHz locks to center frequency 80566406 Hz.



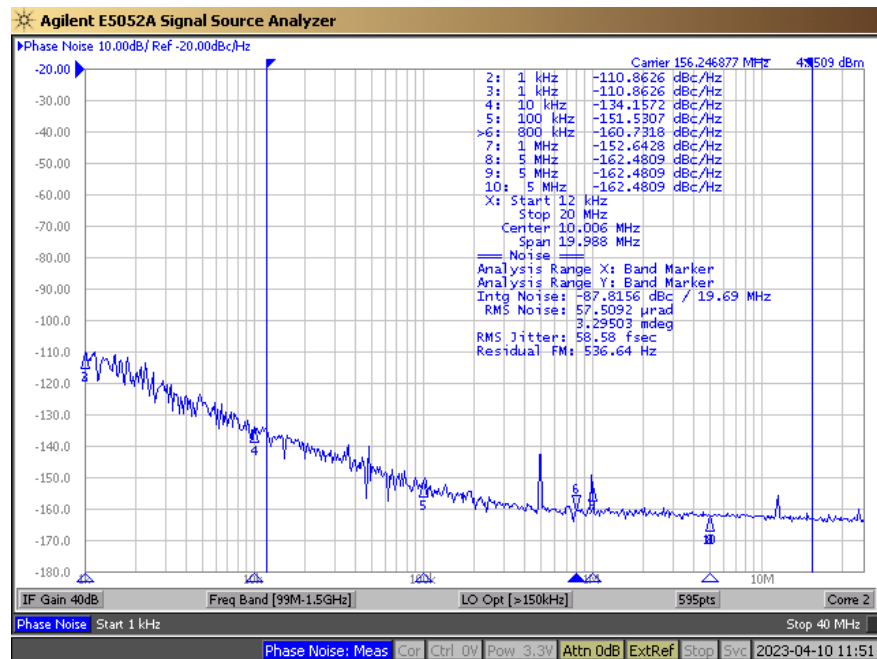
PRIREF/SECREF = 80566406 Hz + 20 ppm

- OUT0 156.25 MHz follows +20 ppm drift on the reference 80566406 Hz.
 - 80566406 Hz + 20 ppm = 80568017 Hz
 - 156.25 MHz + 20 ppm = 156.253125 MHz



PRIREF/SECREF = 80566406 Hz - 20 ppm

- OUT0 156.25 MHz follows -20 ppm drift on the reference 80566406 Hz.
 - 80566406 Hz - 20 ppm = 80564795 Hz
 - 156.25 MHz - 20 ppm = 156.246875 MHz



PRIREF/SECREf = 80566406 Hz +/- 40 ppm

80566406 Hz + 40 ppm = 80569629 Hz

156.25 MHz + 40 ppm = 156.256250 MHz

80566406 Hz - 40 ppm = 80563183 Hz

156.25 MHz - 40 ppm = 156.243750 MHz

