

LMK05318B TICS Pro GUI Overview

2022-05-03

CTS Apps & Systems

Introduction

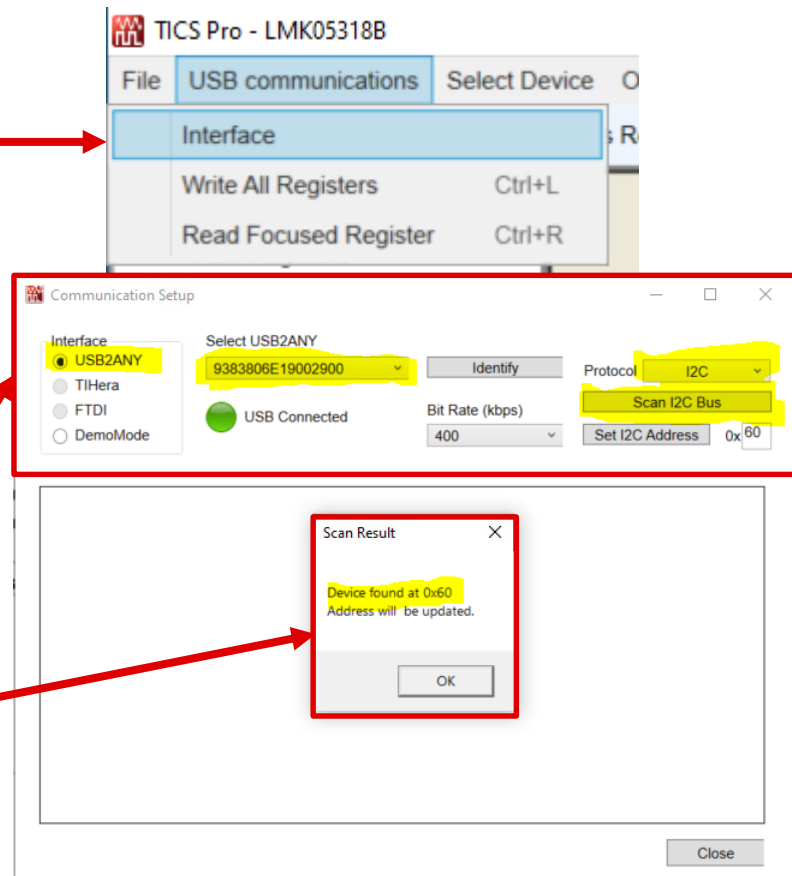
In order to program the LMK05318B using TICS Pro, the following procedure must be performed:

1. Establish communication between the LMK05318B and TICS Pro
2. Initialize key features of the device on the Wizard home page
3. Configure the XO input
4. Set the outputs
5. Set the reference and its validation detectors
6. Configure the DPLL

Step 1: Establish Connection

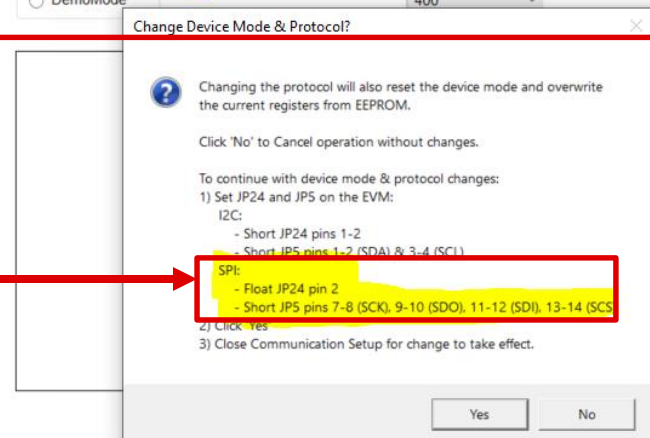
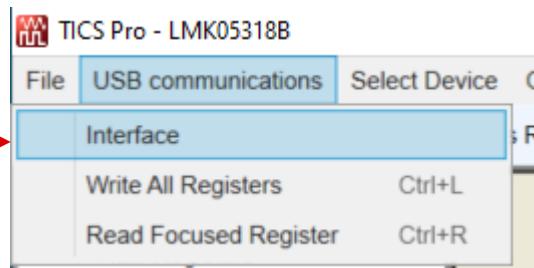
Step 1: Establish Connection between TICS Pro and the LMK05318B (I2C)

- To establish connection between the device and GUI, navigate to **USB communications** → **Interface** in the toolbar.
- Once **Interface** has been selected, a communication setup window will appear.
 - In the window, select the **USB2ANY** interface, select a USB2ANY ID number, set the protocol to **I2C** and then press **Scan I2C Bus**.
 - Once the I2C bus has been scanned and a address is found, you will have obtain successful connection.



Step 1: Establish Connection between TICS Pro and the LMK05318B (SPI)

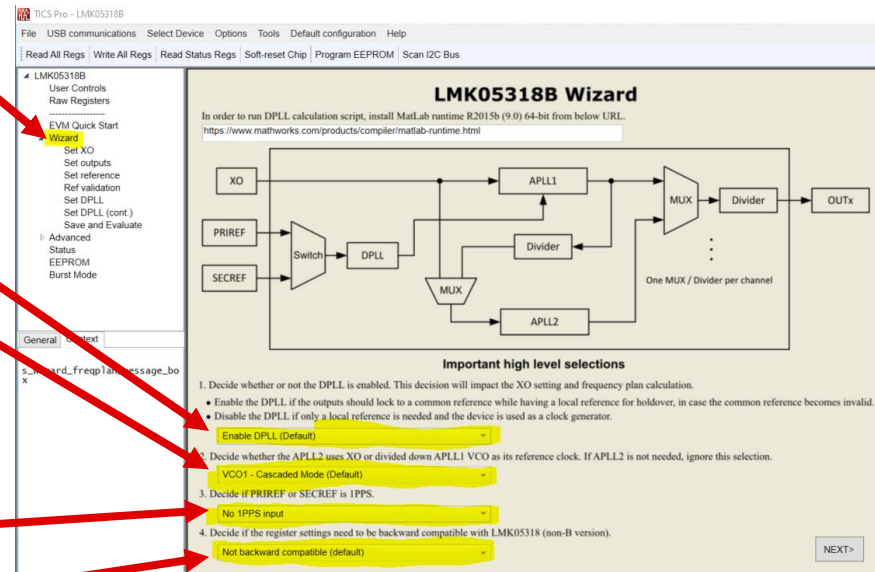
- To establish connection between the device and GUI, navigate to **USB communications** → **Interface** in the toolbar.
- Once **Interface** has been selected, a communication setup window will appear.
 - In the window, select the **USB2ANY** interface, select a USB2ANY ID number, and then set the protocol to **SPI**.
 - When using SPI, ensure that the jumpers are set as shown here:



Step 2: Initialize key features of the device on the Wizard home page

Step 2: Initialize key features of the device on the Wizard home page

- Navigate to the Wizard home page
 - The wizard home page will be used to initialize key devices.
- Key features:
 - Select whether the DPLL will be used.
 - Determine APLL2's reference clock.
 - VCO1 – Cascaded Mode
 - Recommended setting as it will result in better output phase noise performance for APLL2 clocks.
 - XO
 - Decide if PRIREF or SECREF is 1PPS.
 - Decide if the register settings need to be compatible with the non-B version.



Step 3: Configure the XO input

Step 3: Configure the XO input

- Navigate to the Set XO page
 - The Set XO page is used to configure the XO input
- Enter your desired XO frequency
- Enter your desired XO interface type
 - Interface options are:
 - DIFF (no term.)
 - Used for AC or DC coupled differential input types where terminations are external to the input.
 - DIFF (100 Ohm)
 - Used for AC or DC coupled differential input types. 100 ohm termination set internal to LMK05318B, so no external termination required.
 - DIFF (50 Ohm)
 - Used for DC-coupled HCSL input.
 - SE (no term.)
 - Used for DC-coupled LVCMOS input.
 - SE (50 ohm)
 - Used for DC-coupled LVCMOS input and places a 50 ohm to GND on XO_P pin.
- The Instructions message box provides more information on how to configure your XO input.

LMK05318B Wizard

Step 1: Set XO

XO frequency (Hz): 48.0048e6

XO interface type: DIFF (100 Ohm)

INSTRUCTIONS

1. Set XO frequency in Hz. Example frequency formats:

48e6
100e6 / 3
48e6 * (1 + 100e-6)

If DPLL is disabled, then XO frequency can be 25 MHz or 50 MHz for APLL1 to work in integer mode.

If DPLL is enabled then recommended XO frequencies are 12.8 MHz, 19.2 MHz, 24 MHz, 30.72 MHz, 38.88 MHz, 48 MHz and 48.0048 MHz. For 1-pps reference input, low frequency and high stability XO is recommended. For example, 12.8 MHz TCXO or OCXO.

2. The XO doubler and R divider are automatically set. To manually set the R divider and XO doubler, go to tab 'Advanced' -> 'APLL1'. If the DPLL is disabled, then there's no restriction on PFD frequency, as long as it's within the PFD frequency range (10.0 MHz to 100.0 MHz). If the DPLL is enabled, however, two conditions must be met.

XO Interface Type Selection Tips

DIFF (no term.)

DIFF (100 Ohm)

DIFF (50 Ohm)

SE (no term.)

SE (50 Ohm)

1. The 3 types of differential input buffer (no termination, 100 Ω differential or 50 Ω to ground) can accept both AC- and DC- coupled incoming signals. This is because the internal weak bias helps avoid voltage floating between two capacitors. The two types of single-ended input buffer (no termination or 50 Ω to ground) only accept DC coupled input.

2. For single-ended input buffer, the XO_N pin needs to be tied to ground externally.

3. For single-ended input buffer, the allowed input voltage range is between 1 V and 2.6 V. Therefore, 1.8-V and 2.5-V CMOS signals can be directly injected into XO_P. For 3.3-V CMOS signal, however, external resistor divider is needed. Example resistor values are 125 Ω and 375 Ω . The resulted voltage swing is: $3.3V \cdot 375 / 500 = 2.48 V$.

Show Instructions

BACK NEXT>

Step 4: Set the output frequencies and output format types

Step 4: Set the output frequencies and output format types

- Navigate to the **Set Outputs** page
- Enter your desired output frequencies
- Select your desired output formats
 - Format options are:
 - AC-LVDS
 - AC-LVPECL
 - AC-CML
 - HCSL (external 50 ohm)
 - HCSL (internal 50 ohm)
 - OUT 4 to OUT7 also support CMOS
- Once you have set the output frequencies and formats, press **Calculate frequency plan**
 - The APLL configuration of the device will now be completed.
 - The APLL settings will be shown in the instruction box
- If you would like to use different VCO frequencies from the ones automatically calculated, you can select them in the manual selection box.
 - Then press **Apply selected solution** for the new VCO settings to be applied.

LMK05318B Wizard

Step 2: Set Output Frequency Plan

Channel	Target freq (Hz)	Source	Output format	Actual freq
CH0_1	156.25e6	APLL1	AC-LVPECL	156.25 MHz
CH2_3	312.5e6	APLL1	AC-LVDS	156.25 MHz
CH4	100e6	APLL1	AC-CML	312.5 MHz
CH5	25e6	APLL1	HCSL(ext. 50R)	312.5 MHz
CH6	155.52e6	APLL2	HCSL(int. 50R)	100.0 MHz
CH7	155.52e6	APLL2	CMOS(+-)	25.0 MHz
			CMOS(+/-)	155.52 MHz
			CMOS(HZ/+)	155.52 MHz

Calculate frequency plan

Frequency plan completed!

Selected frequency plan:

VCO1 frequency = 2500.0 MHz
VCO2 frequency = 6065.28 MHz

APLL1 settings:

PFDFreq = 48004800 Hz

Numerator = 8589918525
Denominator = 1099511627776
Post divider = 1

APLL2 settings:

APLL2 reference source is VCO1
N divider = 43
Numerator = 10469
Denominator = 15625
Post divider 1 = 3
Post divider 2 = 3

Apply selected solution

Step 5: Set the reference and its validation detectors

Step 5A: Set the reference

- Navigate to the **Set reference** page
- Enable or disable PRIREF and SECREF as needed. **If DPLL is not used, then disable both references and skip this page.**
- Type the frequencies of PRIREF and / or SECREF in Hz.
- Enter your desired REF interface type
 - Interface options are:
 - DIFF (no term.)
 - Used for AC or DC coupled differential input types where terminations are external to the input.
 - DIFF (100 Ohm)
 - Used for AC or DC coupled differential input types. 100 ohm termination set internal to LMK05318B, so no external termination required.
 - DIFF (50 Ohm)
 - Used for DC-coupled HCSL input.
 - SE (no term.)
 - Used for DC-coupled LVCMOS input.
 - SE (50 ohm)
 - Used for DC-coupled LVCMOS input and places a 50 ohm to GND on the _P pin of the reference
- Select the input switching mode and priorities inside **red box** in image
 - descriptions of each mode are shown here
- The Instructions message box provides more information on how to configure your reference inputs. Please read for greater details.**

LMK05318B Wizard

Step 3: Set DPLL References

☒ Enable PRIREF ☒ Enable SECREF

PRIREF frequency (Hz): 25e6 SECREF frequency (Hz): 25e6

PRIREF interface type: DIFF (100 Ohm) SECREF interface type: SE (50 Ohm)

AC hysteresis = 200 mV AC hysteresis = 200 mV

Input switching mode: Auto non-revertive

☒ Prioritize PRIREF

Input Switching Mode Selection Guide

1. Auto Non-Revertive: The DPLL automatically selects the valid input with the highest priority. If a higher priority input becomes valid, the DPLL will not switch over until the currently selected input becomes invalid.
2. Auto Revertive: The DPLL automatically selects the valid input with the highest priority. If a higher priority input becomes valid, the DPLL will automatically switch over to that clock.
3. Manual Failback: The manually selected reference is the active reference until it becomes invalid. If the reference becomes invalid, the DPLL will automatically fallback to the highest priority input that is valid. If no input is valid, the DPLL will enter holdover mode (if tuning word history is valid) or free-running mode. The DPLL will exit holdover mode when the selected input becomes valid.
4. Manual Holdover: The manually selected reference is the active reference until it becomes invalid. If the reference becomes invalid, the DPLL will automatically enter holdover mode (if tuning word history is valid) or free-running mode. The DPLL will exit holdover mode when the selected input becomes valid.

Instructions

1. Enable or disable PRIREF and SECREF as needed. If DPLL is not used, then disable both references and skip this page.
2. Type the frequencies of PRIREF and / or SECREF in Hz. Example frequency formats:
1. 25e6
100e6 / 3
3. Select interface type. AC or DC buffer is auto-selected based on reference frequency. If reference frequency is below 5 MHz, then use DC buffer. Otherwise, use AC buffer. To select interface types for AC buffer, refer to the Interface Type Selection Tip in the XO wizard page. The same can be applied to PRIREF and SECREF.
4. Select the input switching mode. The input switching mode is auto-selected based on the states of PRIREF and SECREF enable. When both references are enabled, then Auto non-revertive is selected. If only one reference is enabled, then manual holdover is selected. However, it is highly recommended to read through the Input Switching

<BACK NEXT>

Step 5B: Set the reference validation detectors overview

- If DPLL is disabled, then skip this page.
- All reference validation methods have been enabled or disabled automatically based on reference frequency and interface type.
 - However, it is highly recommended to read through the instructions and loose or tighten the thresholds according to application needs.
- The **Frequency Detect Threshold, Early Window Detector, and Late/Missing Window Detector** are only valid for reference frequencies ≥ 2 kHz.
- The **1-PPS Phase Detector** is only valid for reference frequencies < 2 kHz.
- For 1-pps input, only enable the **1-pps phase detector** and disable all other detectors.

LMK05318B Wizard
Step 4: Set Reference Validation

	Validation Timer	Amplitude Detector
Enable	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
PR1	102.4 ms	Amplitude Detector Mode
SEC	102.4 ms	Amplitude Detector Mode

	Frequency Detect Threshold	Early Window Detector	Late / Missing Window Detector	1 PPS Phase Detector
Valid (ppm)	100	110	10	2
Invalid (ppm)	110	10	2	4.17 ms
Accuracy (ppm)	10	2	4.17 ms	1
Average (count)	2	4.17 ms	1	6.40 ns
Meas time	4.17 ms	1	6.40 ns	0
Enable	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
PR1	100	110	10	2
SEC	100	110	10	2

Early / Late Window Detector
Reference clock is valid if the next edge falls within this range
Ideal next edge
t = 0
T_{EARLY}
T_{LATE}

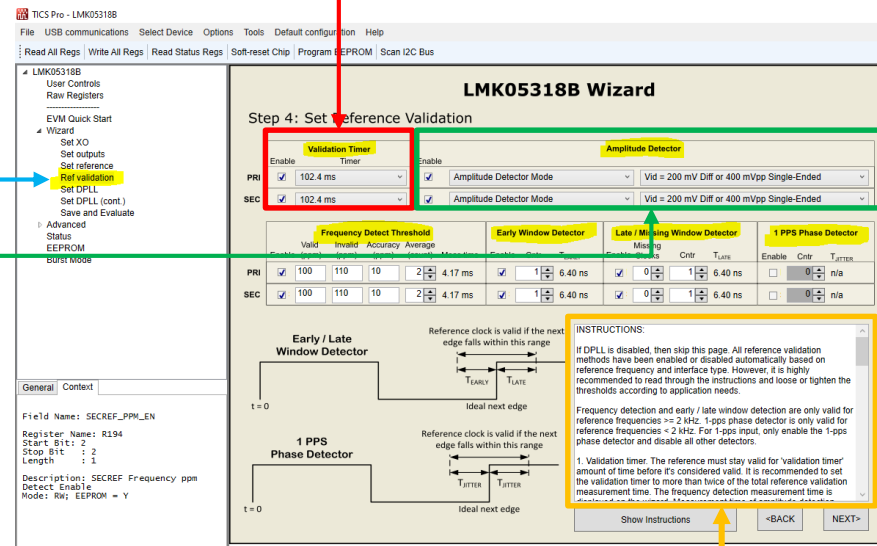
1 PPS Phase Detector
Reference clock is valid if the next edge falls within this range
Ideal next edge
t = 0
T_{1PPS}
T_{1PPS}

INSTRUCTIONS:
If DPLL is disabled, then skip this page. All reference validation methods have been enabled or disabled automatically based on reference frequency and interface type. However, it is highly recommended to read through the instructions and loose or tighten the thresholds according to application needs.
Frequency detection and early / late window detection are only valid for reference frequencies ≥ 2 kHz. 1-pps phase detector is only valid for reference frequencies < 2 kHz. For 1-pps input, only enable the 1-pps phase detector and disable all other detectors.
1. Validation timer. The reference must stay valid for "validation timer" amount of time before it's considered valid. It is recommended to set the validation timer to more than twice of the total reference validation measurement time. The frequency detection measurement time is...

Show Instructions <BACK NEXT>

Step 5C: Set the reference validation detectors configuration

- Navigate to the **Ref validation** page
- Set the Validation Timer
 - The validation timer setting determines the amount of time the reference must stay valid before it's considered valid.
- Set the Amplitude Detector
 - There are two modes: amplitude detector mode and CMOS slew rate detector mode
 - In amplitude detector mode, the reference is considered valid if the signal swing is higher than the selected threshold.
 - In CMOS slew rate detector mode, the detection method can be either slew rate detection or VIH / VIL detection.
 - For slew rate detection, the input slew rate must be faster than 0.2 V/ns.
 - For VIH / VIL detection, the input high level must be above 1.8 V and the low level must be below 0.6 V.
- **The Instructions message box provides more information on how to configure your reference validation settings. Please read for greater details.**



Step 5C: Set the reference validation detectors configuration (continued)

- For reference frequencies ≥ 2 kHz
 - Set the Frequency Detect Threshold
 - Frequency detection needs 4 parameters:
 - Valid threshold in ppm
 - Invalid threshold in ppm
 - Accuracy in ppm
 - Average count
 - Please read the instruction box (bullet 3) for more details on how to configure the frequency detector parameters.
 - Set the Early Window Detector
 - Determines T_{early}
 - Set the Late/Missing Window Detector
 - Determines T_{late}
 - The reference input is considered valid if its next clock edge falls within the T_{early} and T_{late} range
 - Please read the instruction box (bullet 4) for more details on how to configure the early and late detector parameters.
- For a 1PPS reference
 - Set the 1PPS Phase Detector
 - Determines T_{jitter}
 - The reference input is considered valid if its next clock edge falls within the T_{jitter} range

LMK05318B Wizard

Step 4: Set Reference Validation

Validation Timer

Enable	Timer	Enable	Amplitude Detector Mode	Vid = 200 mV Diff or 400 mVpp Single-Ended
<input checked="" type="checkbox"/>	102.4 ms	<input checked="" type="checkbox"/>	Amplitude Detector Mode	
<input checked="" type="checkbox"/>	102.4 ms	<input checked="" type="checkbox"/>	Amplitude Detector Mode	

Frequency Detect Threshold

Valid (ppm)	Invalid (ppm)	Accuracy (ppm)	Average (count)	Meas time
<input checked="" type="checkbox"/>	100	110	10	2 4.17 ms
<input checked="" type="checkbox"/>	100	110	10	2 4.17 ms

Early Window Detector

Enable	Cntr	T_{EARLY}
<input checked="" type="checkbox"/>	1	6.40 ns
<input checked="" type="checkbox"/>	1	6.40 ns

Late / Missing Window Detector

Enable	Cntr	T_{LATE}
<input checked="" type="checkbox"/>	0	6.40 ns
<input checked="" type="checkbox"/>	1	6.40 ns

1 PPS Phase Detector

Enable	Cntr	T_{JITTER}
<input type="checkbox"/>	0	n/a
<input type="checkbox"/>	0	n/a

Early / Late Window Detector

Reference clock is valid if the next edge falls within this range

$t = 0$

T_{EARLY} T_{LATE}

Ideal next edge

1 PPS Phase Detector

Reference clock is valid if the next edge falls within this range

$t = 0$

T_{JITTER} T_{JITTER}

Ideal next edge

INSTRUCTIONS:

If DPLL is disabled, then skip this page. All reference validation methods have been enabled or disabled automatically based on reference frequency and interface type. However, it is highly recommended to read through the instructions and loosen or tighten the thresholds according to application needs.

Frequency detection and early / late window detection are only valid for reference frequencies ≥ 2 kHz. 1-pps phase detector is only valid for reference frequencies < 2 kHz. For 1-pps input, only enable the 1-pps phase detector and disable all other detectors.

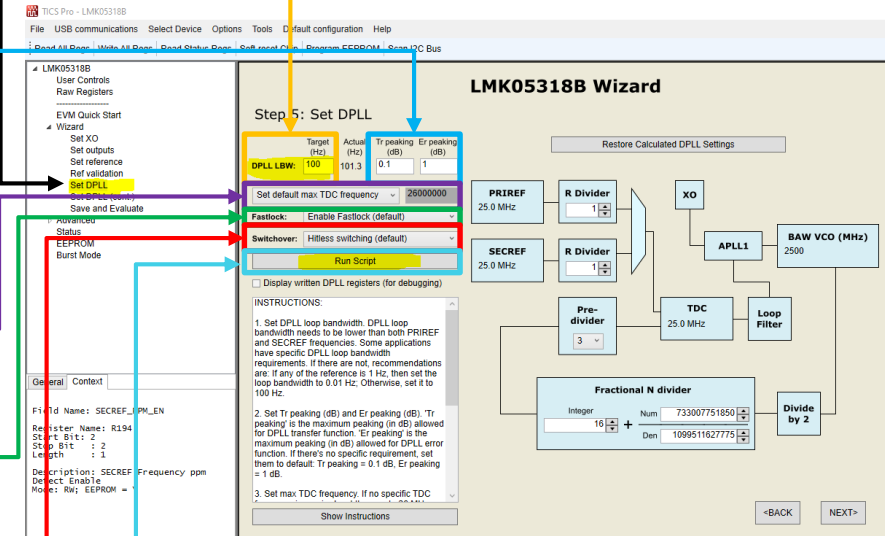
1. Validation timer. The reference must stay valid for "validation timer" amount of time before it's considered valid. It is recommended to set the validation timer to more than twice of the total reference validation measurement time. The frequency detection measurement time is defined as the time between two consecutive clock edges.

Show Instructions -BACK NEXT>

Step 6: Configure the DPLL

Step 6: Configure the DPLL

- Navigate to the **Set DPLL** page
- Set the DPLL loop bandwidth
 - The DPLL loop bandwidth needs to be lower than both PRREF and SECREF frequencies
- Set Tr peaking (dB) and Er peaking (dB)
 - Tr peaking is the maximum peaking (in dB) allowed for DPLL transfer function
 - default: Tr peaking = 0.1 dB
 - Er peaking is the maximum peaking (in dB) allowed for DPLL error function.
 - Default: Er peaking = 1 dB
- Set max TDC frequency
 - If no specific TDC frequency is required, set the max to 26 MHz
- Fastlock should only be disabled for 1pps input
- For most use cases, switchover method should always be set to 'hitless switching'.
- Click 'Run Script' button and wait for 1 ~ 2 minutes while the script is running. Make sure that the MATLAB runtime is installed as instructed in the first wizard page.



Step 6: Configure the DPLL (continued)

- Navigate to the **Set DPLL (cont.)** page
- Configure the BAW Frequency Lock Detect
 - Disable if DPLL is enabled
 - Used to determine if BAW (VCO1) is locked
- Configure the DPLL Frequency Lock Detect
 - Used to determine if DPLL is frequency locked
- Configure the DPLL Phase Lock Detect
 - Used to determine if DPLL is phase locked
- Configure the Tuning Word History
 - This block sets the tuning word history for holdover.
 - Refer to datasheet section '9.3.7.4 Tuning Word History' for details.
- **The Instructions message box provides more information on how to configure the lock detectors and tuning word history settings. Please read for greater details.**

The screenshot shows the LMK05318B Wizard software interface. The title bar indicates 'TICS Pro - LMK05318B'. The menu bar includes 'File', 'USB Communications', 'Select Device', 'Options', 'Tools', 'Default configuration', and 'Help'. The toolbar contains 'Read All Regs', 'Write All Regs', 'Read Status Regs', 'Soft-reset Chip', 'Program EEPROM', and 'Scan I2C Bus'. The left sidebar shows a tree view with 'LMK05318B' expanded, containing 'User Controls', 'Raw Registers', 'EVM Quick Start', 'Wizard', 'Set XO', 'Set outputs', 'Set reference', 'Ref validation', 'Set DPLL', 'Set DPLL (cont.)', 'Save and Evaluate', 'Advanced', 'Status', 'EEPROM', and 'Burst Mode'. The main area is titled 'LMK05318B Wizard' and 'Step 6: Set DPLL (cont.)'. It features an 'INSTRUCTIONS' panel on the left and a configuration area on the right. The configuration area includes sections for 'BAW Frequency Lock Detect', 'DPLL Frequency Lock Detect', 'DPLL Phase Lock Detect', and 'Tuning Word History'. Each section has checkboxes for enabling/disabling and 'Set Default' buttons. The 'DPLL Phase Lock Detect' section has a 'Recommended' button. The 'Tuning Word History' section has a 'Min Values Required' button. The bottom of the configuration area has '<BACK' and 'NEXT>' buttons.

LMK05318B Wizard
Step 6: Set DPLL (cont.)

INSTRUCTIONS:

All lock detect settings are set to either default or recommended values after the DPLL script is run. Still, it is highly recommended to go through the instructions and make the adjustments.

1. BAW frequency lock detect. Disable this if DPLL is enabled. This detector is only useful if the DPLL is disabled and the device works in free-running mode. Enter lock threshold in ppm, unlock threshold in ppm, average count (min value = 2) and accuracy in ppm. The BAW (VCO1) is considered to be locked if the frequency error between the BAW and the XO is within lock threshold. Once the BAW is locked, it's considered to be unlocked if the frequency error exceeds the unlock threshold. The step size of lock and unlock threshold in ppm = accuracy / average. If there's no specific requirement for BAW lock detect, click 'Set Default'.

2. DPLL frequency lock detect. Enter lock and unlock thresholds in ppm, average count (min value = 2) as well as accuracy in ppm. The DPLL is considered to be frequency locked if the frequency error between the VCO1 and the reference is within the lock threshold. While the DPLL is frequency locked, it's considered to be frequency unlocked if the frequency error exceeds the unlock threshold. The step size of lock and unlock threshold = accuracy / average. If there's no specific requirement for DPLL frequency lock detect, click 'Set Default'.

3. DPLL phase lock detect. Set lock and unlock threshold counters. The actual lock and unlock thresholds in second are then calculated accordingly. The DPLL is considered as phase locked if the phase difference between the two inputs of TDC (divided reference and divided VCO1) is within the lock threshold. While the DPLL is phase locked, it's considered as phase unlocked if the phase difference exceeds the unlock threshold. Use recommended values for this. The lock and unlock counters should not be manually set, and they are only used for intermediate debugging purposes.

BAW Frequency Lock Detect ☒ enable

Lock ppm	Unlk ppm	Average	Acry (ppm)	Meas time
5	10	2	1	19.2000 ms

DPLL Frequency Lock Detect ☒ enable

Lock ppm	Unlk ppm	Average	Acry (ppm)	Meas time
1	10	10	1	96.0000 ms

DPLL Phase Lock Detect

Lock cnt	Lock thresh	Unlk cnt	Unlk thresh	Meas time
28	384.96 ps	32	6.16 ns	9.87 ms

Tuning Word History ☒ enable

Hist cnt	Avg time	Delay cnt	Delay time
0	115.34 ms	44	20.28 ms

HIST_INTMD No intermediate update

DPLL_TUNING_FREE_RUN 0

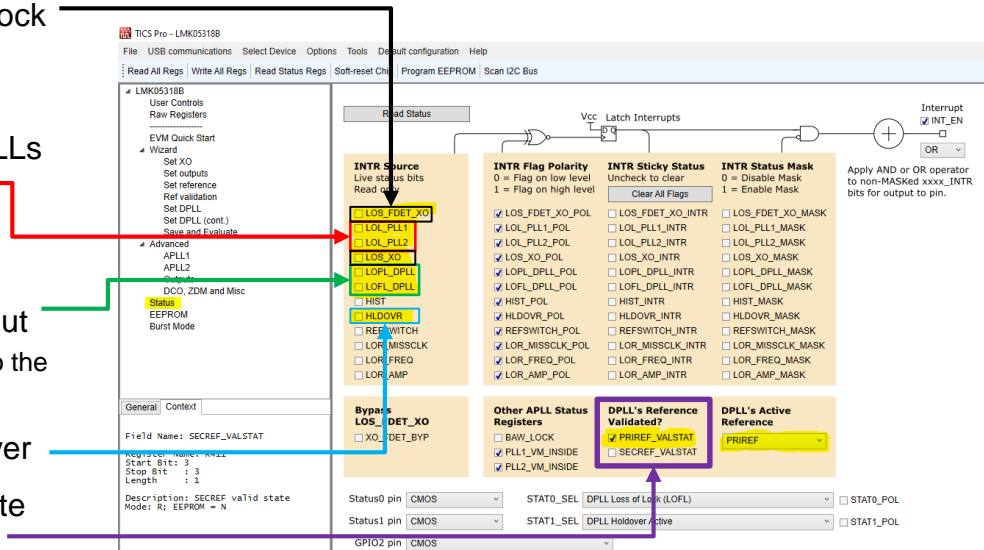
Appendix: Additional GUI Features

Appendix Introduction

- The following appendix slides will display additional features of the LMK05318B.
- Please note that these are features are not required for obtaining an initial configuration, but can be beneficial features after the initial configuration is created by following steps 1 to 6 on the previous slides.
- The additional features include:
 - Status page
 - DCO and ZDM page
 - Outputs page
 - EEPROM page
 - APLL1 page
 - APLL2 page
 - User controls page
 - Raw registers page

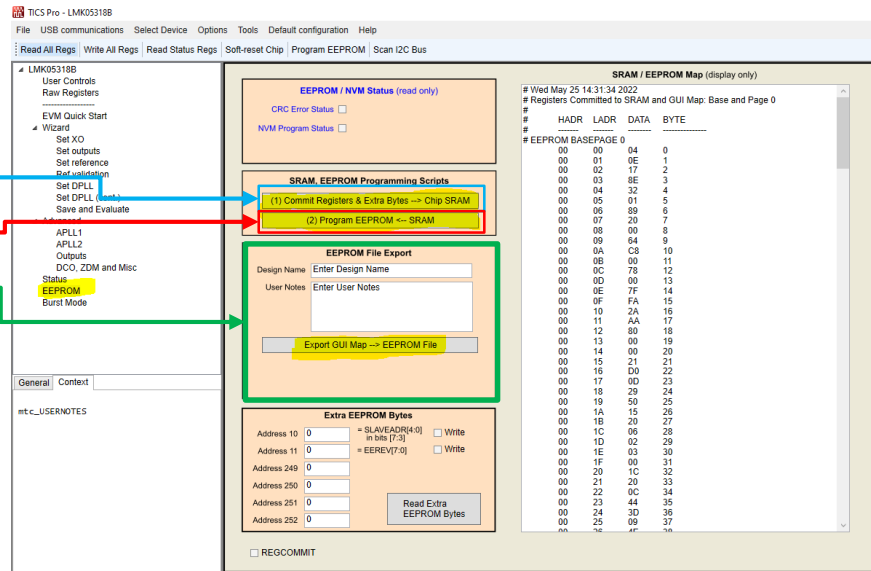
Status Page

- The Status Page can be used to validate the device is locking properly
- LOS_FDET_XO and LOS_XO indicate whether a clock is present at the XO input for the APLLs to lock to
 - When the bits are low, the XO is present and valid
- LOL_PLL1 and LOL_PLL2 indicate whether the APLLs are locking to the XO input
 - When the bits are low, the APLLs are locked properly
- LOPL_DPLL and LOFL_DPLL indicate whether the DPLL is frequency and phase locked to the REF input
 - When the bits are low, the DPLL has successfully locked to the REF input
- HLDOVR indicates whether the device is in holdover
- PRIREF_VALSTAT and SECREF_VALSTAT indicate whether the PRIREF or SECREF are present and validated by the reference validation detectors set in step 5
 - When the bits are high, the reference is valid



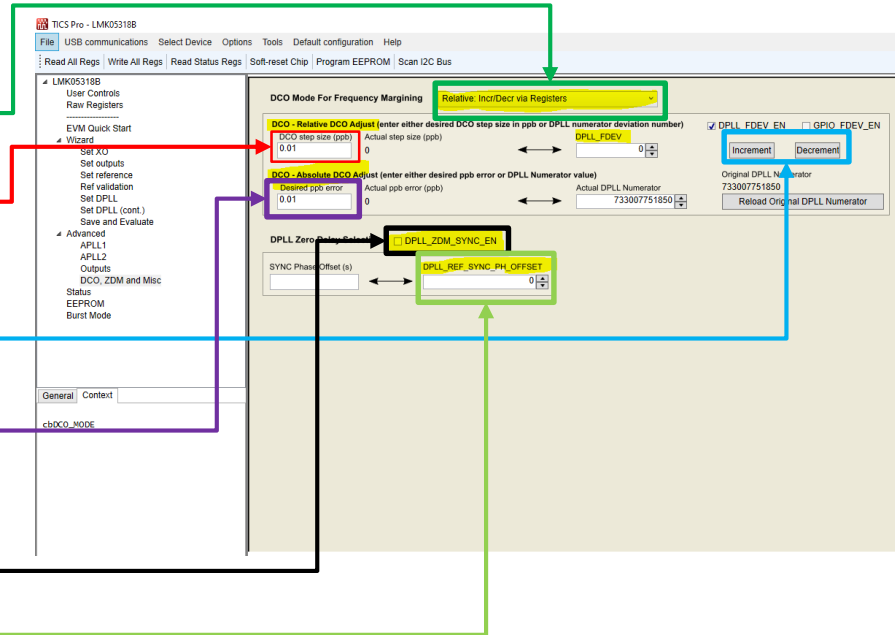
EEPROM Page

- The EEPROM page contains the following features:
 - Program the EEPROM
 - To program the EEPROM, you must
 - Commit the register to the SRAM
 - Program the EEPROM
 - Export the GUI Map to a EEPROM file



DCO and ZDM Page

- The DCO and ZDM Page can be used to:
 - Perform frequency/phase adjustments with the DCO
 - DCO adjustments can be performed relatively or absolutely
 - Select whether a relative or absolute adjustment is required
 - Relative adjustment
 - Enter a ppb adjustment that is required and a DPLL_FDEV will be calculated
 - The DPLL_FDEV will be the numerator deviation that will be adjusted from the DPLL numerator to result in the required ppb adjustment
 - Press the Increment or decrement button to add or subtract the required ppb adjustment
 - Absolute adjustment
 - Enter a ppb adjustment that is required and the output clock will automatically be adjusted by that ppb value
 - Enable zero-delay mode to achieve phase alignment between the input clock and output clock on OUT7
 - When the DPLL_ZDM_SYNC_EN is set, ZDM is enabled to achieve input and output phase alignment
 - The DPLL_REF_SYNC_PH_OFFSET can be used to adjust the phase offset between the input and output clocks



Outputs Page

- The channel muxes, channel dividers, output formats, and output frequencies shown on the outputs page are configured in step 4
- The outputs page provides the following additional features:
 - Output clock synchronization
 - Output sync can be accomplished by enabling the CHx_SYNC_EN bits **highlighted** in the image to the right
 - For the synchronization to take place, the SYNC_SW bit must be toggled (turned on/off)

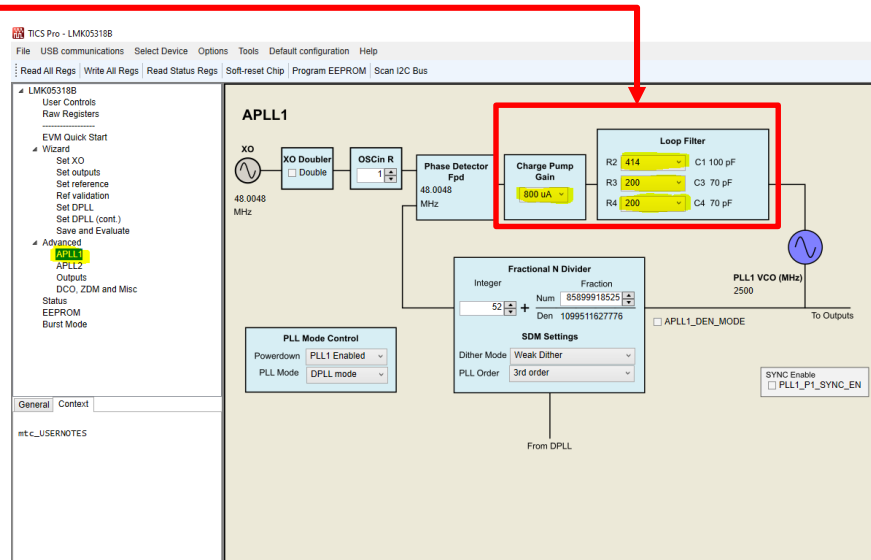
The screenshot shows the TI CICS Pro - LMK053188 Outputs page. The left sidebar contains a tree view with 'Raw Registers' expanded, showing 'EVM Quick Start' and 'Wizard'. The main area is divided into sections: 'Outputs', 'Channel Muxes, Powerdowns', 'Channel Dividers and Synchronization', and 'Output Drivers, Mute Options'. The 'Outputs' section shows PLL1 VCO (2500 MHz) and PLL2 VCO (6065.28 MHz). The 'Channel Dividers and Synchronization' section shows a table of channel configurations. The 'Output Drivers, Mute Options' section shows a table of output drivers and their frequencies. The SYNC_SW bit is highlighted in the PLL1 VCO section. The CHx_SYNC_EN bits are highlighted in the Channel Dividers and Synchronization section. The output frequencies are listed in the Output Drivers section.

Channel Muxes, Powerdowns	Channel Dividers and Synchronization	Output Drivers, Mute Options	OUT
APLL1 P1 CH0_1_PD	16 CH0_1_SYNC_EN DIV0_1_DYN_DIV_SW	AC-LVPECL CH0_MUTE AC-LVDS CH1_MUTE	OUT0 156.25 MHz OUT1 156.25 MHz
APLL1 P1 CH2_3_PD	8 CH2_3_SYNC_EN DIV2_3_DYN_DIV_SW	AC-CML CH2_MUTE HCSL(ext. 50R) CH3_MUTE	OUT2 312.5 MHz OUT3 312.5 MHz
APLL1 P1 CH4_PD	25 CH4_SYNC_EN DIV4_DYN_DIV_SW	HCSL(int. 50R) CH4_MUTE	OUT4 100.0 MHz
APLL1 P1 CH5_PD	100 CH5_SYNC_EN DIV5_DYN_DIV_SW	CMOS(+-) CH5_MUTE	OUT5 25.0 MHz
APLL2 P1 CH6_PD	13 CH6_SYNC_EN DIV6_DYN_DIV_SW	CMOS(+-HIZ) CH6_MUTE	OUT6 155.52 MHz
APLL2 P1 CH7_PD	13 CH7_SYNC_EN DIV7_DYN_DIV_SW	CMOS(+-HIZ) CH7_MUTE	OUT7 155.52 MHz

Arrange PLL Post Dividers and Output Channels carefully to optimize jitter/spurs:
 - Preferred channel assignment: PLL1 to OUT[0:3] bank, PLL2 to OUT[4:7] bank
 - Group identical frequencies on adjacent channels
 - Separate channels where (F_{OUT1} - F_{OUT2}) falls within the jitter integration BW (eg. 12 kHz - 20 MHz)
 - Avoid / isolate CMOS outputs, or else use CMOS(+-) or CMOS(+-HIZ)

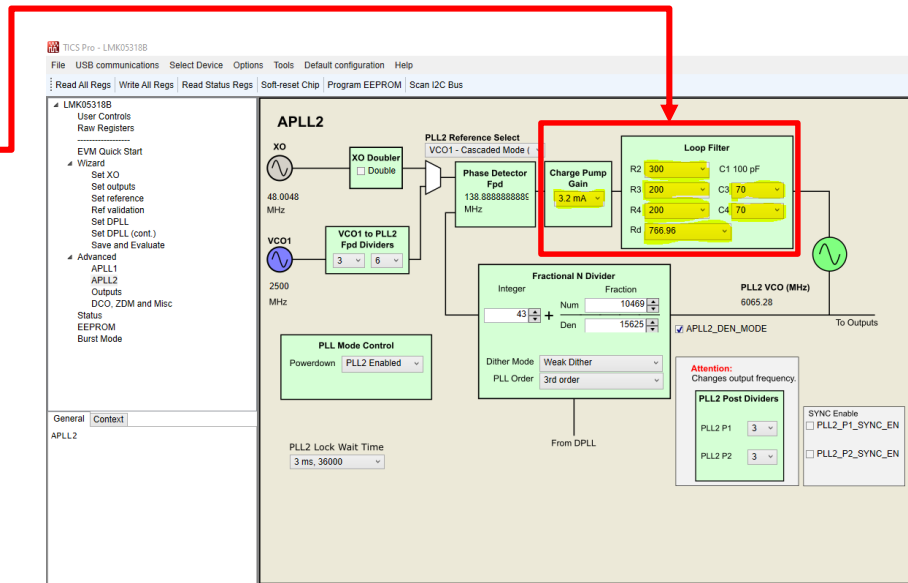
APLL1 Page

- The APLL1 page can be used to configure the charge pump current and loop filter to optimize the output clocks performance
- The rest of the controls on this page will be configured in step 4 and should not be change



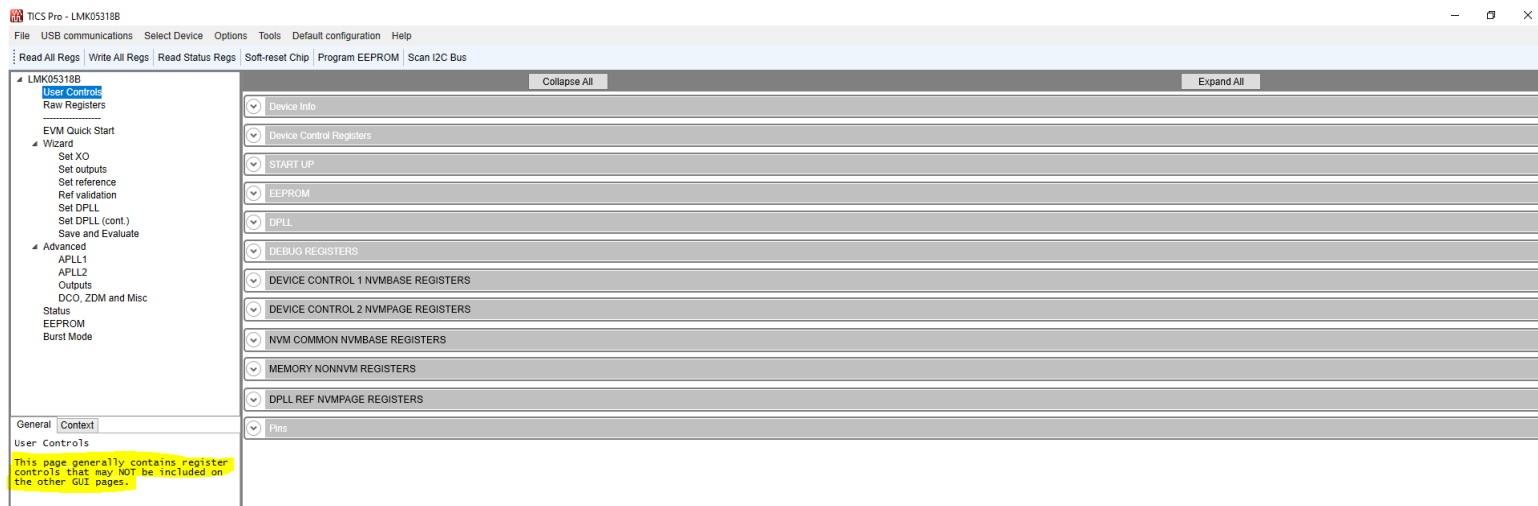
APLL2 Page

- The APLL2 page can be used to configure the charge pump current and loop filter to optimize the output clocks performance
- The rest of the controls on this page will be configured in step 4 or step 2 and should not be change



User Controls Page

- The user control page contains register controls that may not be included on the other GUI pages
 - For example, the device info registers such as PRTID, PRODID, etc.



Raw Registers Page

- The raw register page allows for low-level register write/read operations by register address

The screenshot displays the 'Raw Registers' page in the TICS Pro software for the LMK05118B device. The left sidebar contains a tree view with categories like 'User Controls', 'Wizard', 'Advanced', and 'Raw Registers'. The main area features a table with columns for 'Register Name', 'Address/Value', and 'Data'. The table lists registers from R0 to R53, each with a hexadecimal address and a 16-bit value. The right-hand panel includes input fields for 'Data', 'Register/Field Name', and 'Value', along with buttons for 'Write Register', 'Read Register', 'Read All Registers', 'Write All Registers', 'Import Register Map', and 'Export Register Map'. A 'Read' button is also present at the bottom of the right panel.

Register Name	Address/Value	Data
R0	0x000010	0x0000000000000000
R1	0x000018	0x0000000000000000
R2	0x000020	0x0000000000000000
R3	0x000028	0x0000000000000000
R4	0x000030	0x0000000000000000
R5	0x000038	0x0000000000000000
R6	0x000040	0x0000000000000000
R7	0x000048	0x0000000000000000
R8	0x000050	0x0000000000000000
R9	0x000058	0x0000000000000000
R10	0x000060	0x0000000000000000
R11	0x000068	0x0000000000000000
R12	0x000070	0x0000000000000000
R13	0x000078	0x0000000000000000
R14	0x000080	0x0000000000000000
R15	0x000088	0x0000000000000000
R16	0x000090	0x0000000000000000
R17	0x000098	0x0000000000000000
R18	0x0000A0	0x0000000000000000
R19	0x0000A8	0x0000000000000000
R20	0x0000B0	0x0000000000000000
R21	0x0000B8	0x0000000000000000
R22	0x0000C0	0x0000000000000000
R23	0x0000C8	0x0000000000000000
R24	0x0000D0	0x0000000000000000
R25	0x0000D8	0x0000000000000000
R26	0x0000E0	0x0000000000000000
R27	0x0000E8	0x0000000000000000
R28	0x0000F0	0x0000000000000000
R29	0x0000F8	0x0000000000000000
R30	0x000100	0x0000000000000000
R31	0x000108	0x0000000000000000
R32	0x000110	0x0000000000000000
R33	0x000118	0x0000000000000000
R34	0x000120	0x0000000000000000
R35	0x000128	0x0000000000000000
R36	0x000130	0x0000000000000000
R37	0x000138	0x0000000000000000
R38	0x000140	0x0000000000000000
R39	0x000148	0x0000000000000000
R40	0x000150	0x0000000000000000
R41	0x000158	0x0000000000000000
R42	0x000160	0x0000000000000000
R43	0x000168	0x0000000000000000
R44	0x000170	0x0000000000000000
R45	0x000178	0x0000000000000000
R46	0x000180	0x0000000000000000
R47	0x000188	0x0000000000000000
R48	0x000190	0x0000000000000000
R49	0x000198	0x0000000000000000
R50	0x0001A0	0x0000000000000000
R51	0x0001A8	0x0000000000000000
R52	0x0001B0	0x0000000000000000
R53	0x0001B8	0x0000000000000000