LMK5C33216 EEPROM Programming

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CTS Apps & Systems

EEPROM Overlay Overview

- Allows POR configuration of registers related to APLL and output configuration
- If the field ROM_PLUS_EE is 1, then an EEPROM overlay is loaded and many fields controlling APLL and output clock configuration will be loaded from the EEPROM.

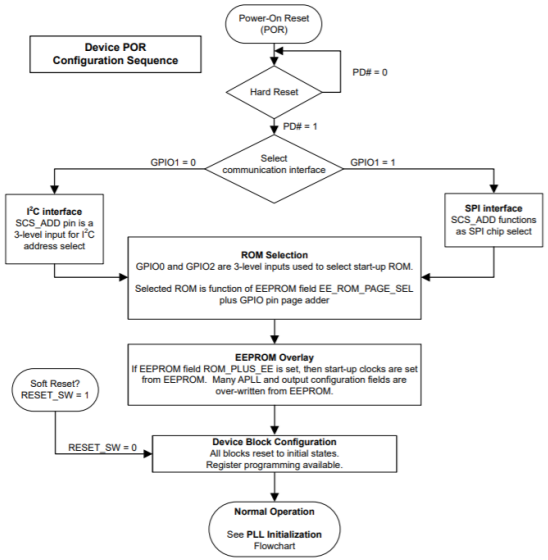

Figure 9-36. Device POR Configuration Sequence

Steps for Performing EEPROM Overlay with REGCOMMIT

- Perform a PD# cycle
  - Set PD# = 0 and the set PD# = 1
- Load EEPROM registers
  - Set ROM_PLUS_EE = 1
  - Set REGCOMMIT = 1
  - Set NVMUNLK = 0xEA
  - Set NVMERASE = 1 and NVMPROG = 1
  - Set NVMUNLK = 0
- Wait for EEPROM programming to finish

```
# Use EEPROM overlay with ROM
R20     0x001480


# Write EEPROM sequence
# REGCOMMIT, regs to SRAM, self clearing
R171    0x00AB40

## NVMUNLK = 234 (0xea)
#R180   0x00B4EA

## NVMERASE & PROG = 1, self clearing
#R171   0x00AB43

## NVMUNLK = 0
#R180   0x00B400
```

R20 ROM_PLUS_EE and EE_ROM_PAGE_SEL

```
# Use EEPROM overlay with ROM
R20     0x001480
```

→ ROM_PLUS_EE = 1
EE_ROM_PAGE_SEL = 0

1.8 R20 Register (Offset = 0x14) [Reset = 0x0]

R20 is shown in Table 1-10.

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Table 1-10. R20 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ROM_PLUS_EE	R/W	0x0	When set, the thin EEPROM settings are loaded. This is user writeable to EEPROM only through SRAM register address 14. ROM=N, EEPROM=Y
6:3	EE_ROM_PAGE_SEL	R/W	0x0	EE_ROM_PAGE_SEL value is added to the GPIO pin value for selecting the start-up ROM. ROM=N, EEPROM=Y
2:0	RESERVED	R	0x0	Reserved

R171 REGCOMMIT

```
# Write EEPROM sequence
# REGCOMMIT, regs to SRAM, self clearing
R171    0x00AB40
```

REGCOMMIT = 1

1.95 R171 Register (Offset = 0xAB) [Reset = 0x0]

R171 is shown in Table 1-97.

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Table 1-97. R171 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	REGCOMMIT	R/WSC	0x0	Copy fields which also exist in SRAM to SRAM memory. The REGCOMMIT bit is automatically cleared to 0 when the transfer is complete. Next an EEPROM programming operation may be performed to update NVM EEPROM. When programming to alter an NVM profile, it is suggested to toggle PD# to assure default conditions, change the desired fields, then assert the REGCOMMIT bit. ROM=N, EEPROM=N

R180 NVMUNLK

```
## NVMUNLK = 234 (0xea)
#R180   0x00B4EA
```

NVMUNLK = 0xEA

1.99 R180 Register (Offset = 0xB4) [Reset = 0x0]

R180 is shown in Table 1-101.

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Table 1-101. R180 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVMUNLK	R/W	0x0	NVM Prog Unlock. The NVMUNLK register must be written immediately prior to setting the NVMERASE and NVMPROG bit, otherwise the Erase/Program cycle will not be triggered. NVMUNLK must be written with a value of 0xEA. ROM=N, EEPROM=N

R171 NVMERASE and NVMPROG

```
## NVMERASE & PROG = 1, self clearing
#R171   0x00AB43
```

REGCOMMIT = 1
NVMERASE = 1
NVMPROG = 1

Table 1-97. R171 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	NVMCRCERR	R	0x0	NVM CRC Error Indication. The NVMCRCERR bit is set to 1 if a CRC Error has been detected when reading back from on-chip EEPROM during device configuration. ROM=N, EEPROM=N
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	NVMBUSY	R	0x0	NVM Program Busy Indication. The NVMBUSY bit is 1 during an on-chip EEPROM Erase/Program cycle. While NVMBUSY is 1 the on-chip EEPROM cannot be accessed. Toggling PD# or removing power while NVMBUSY is asserted will corrupt the EEPROM. ROM=N, EEPROM=N
1	NVMERASE	R/WSC	0x0	NVM Erase Start. The NVMERASE bit is used to begin an on-chip EEPROM Erase cycle. The Erase cycle is only initiated if the immediately preceding I2C/SMBus transaction was a write to the NVMUNLK register withthe appropriate code. The NVMERASE bit is automatically cleared to 0.
0	NVMPROG	R/WSC	0x0	NVM Program Start. The NVMPROG bit is used to begin an on-chip EEPROM Program cycle. The Program cycle is only initiated if the immediately preceding I2C/SMBus transaction was a write to the NVMUNLK register withthe appropriate code. The NVMPROG bit is automatically cleared to 0.

R180 NVMUNLK

```
## NVMUNLK = 0
#R180   0x00B400
```

NVMUNLK = 0

1.99 R180 Register (Offset = 0xB4) [Reset = 0x0]

R180 is shown in Table 1-101.

Return to the Summary Table.

Table 1-101. R180 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVMUNLK	R/W	0x0	NVM Prog Unlock. The NVMUNLK register must be written immediately prior to setting the NVMERASE and NVMPROG bit, otherwise the Erase/Program cycle will not be triggered. NVMUNLK must be written with a value of 0xEA. ROM=N, EEPROM=N