-Changes:

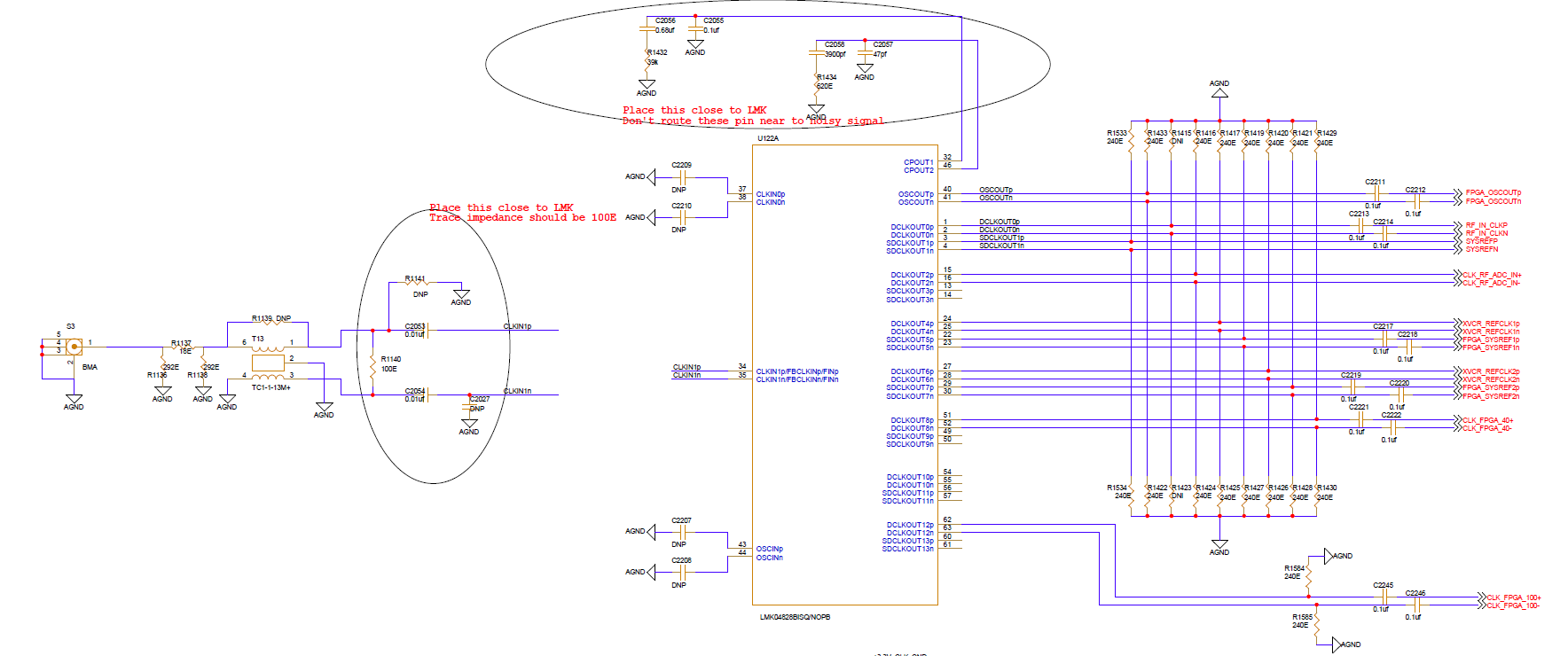
CLKIN/OSCIN frequency – 300MHz,

C2211 – 0.1uF is mounted,

R1433 – 50ohm is mounted,

C2208 – 0.1uF is mounted,

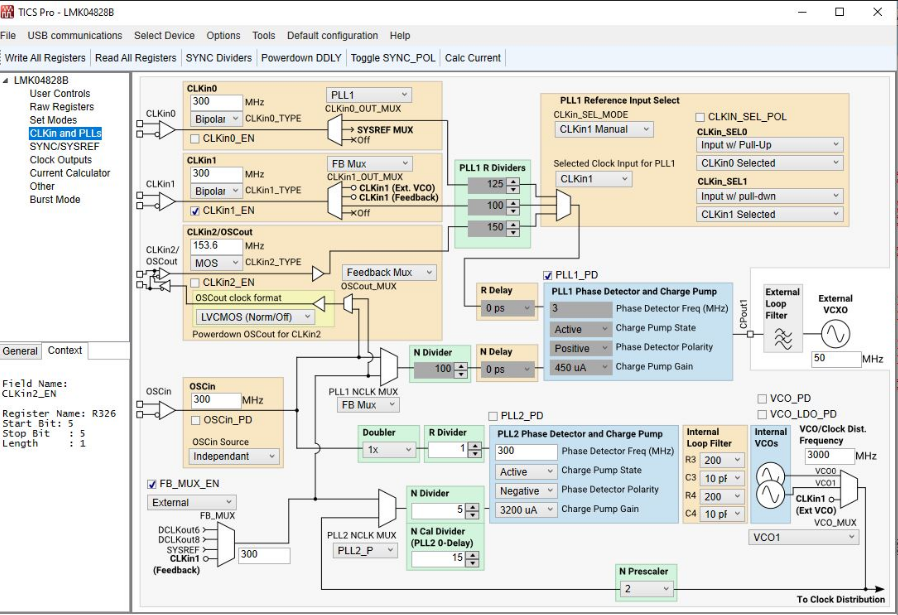
C2211 is connected to OSCINP(simple wire) after disconnecting the FPGA\_OSCOUT signal



100MHz

300MHz

**GUI settings**



**Intel Quartus 20.2:**

* In signal tap we captured xcvr clock(300MHz) @ sampling clock of 600MHz generated using on board crystal clock 25MHz
* **DCLKOUT4** and **DCLKOUT6** clocks from clock conditioner are used as xcvr clocks

 - By using this xvcr ref clk as input clock to ATX PLL ip core, lock output is high.

- Can we proceed jesd interface using this xcvr\_ref\_clk.