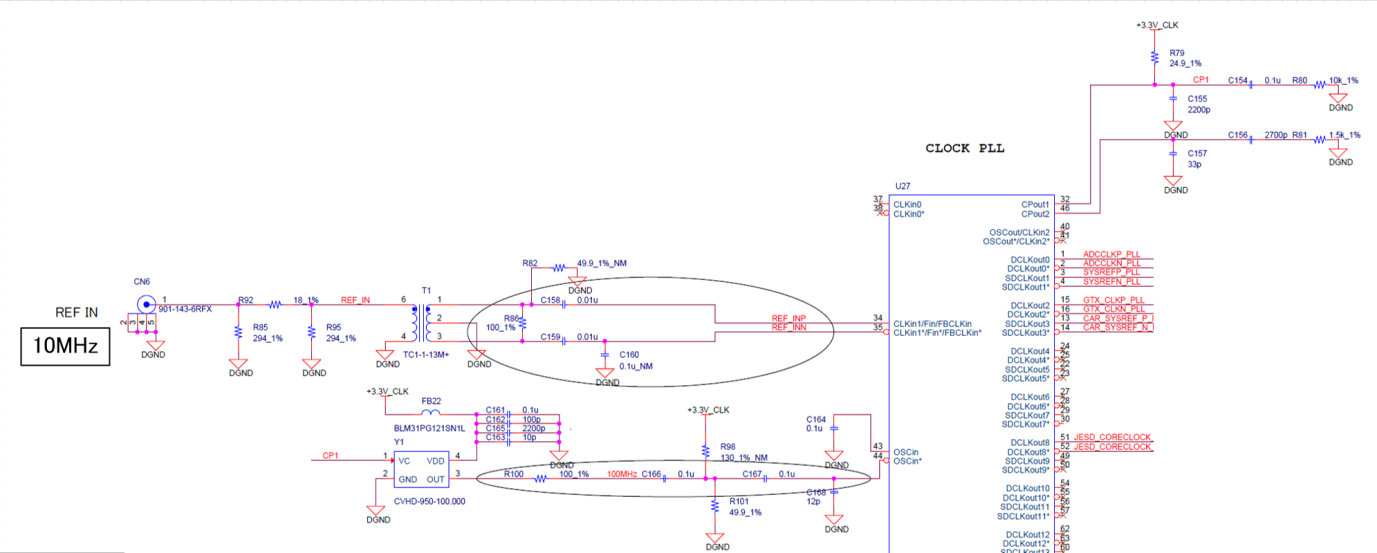
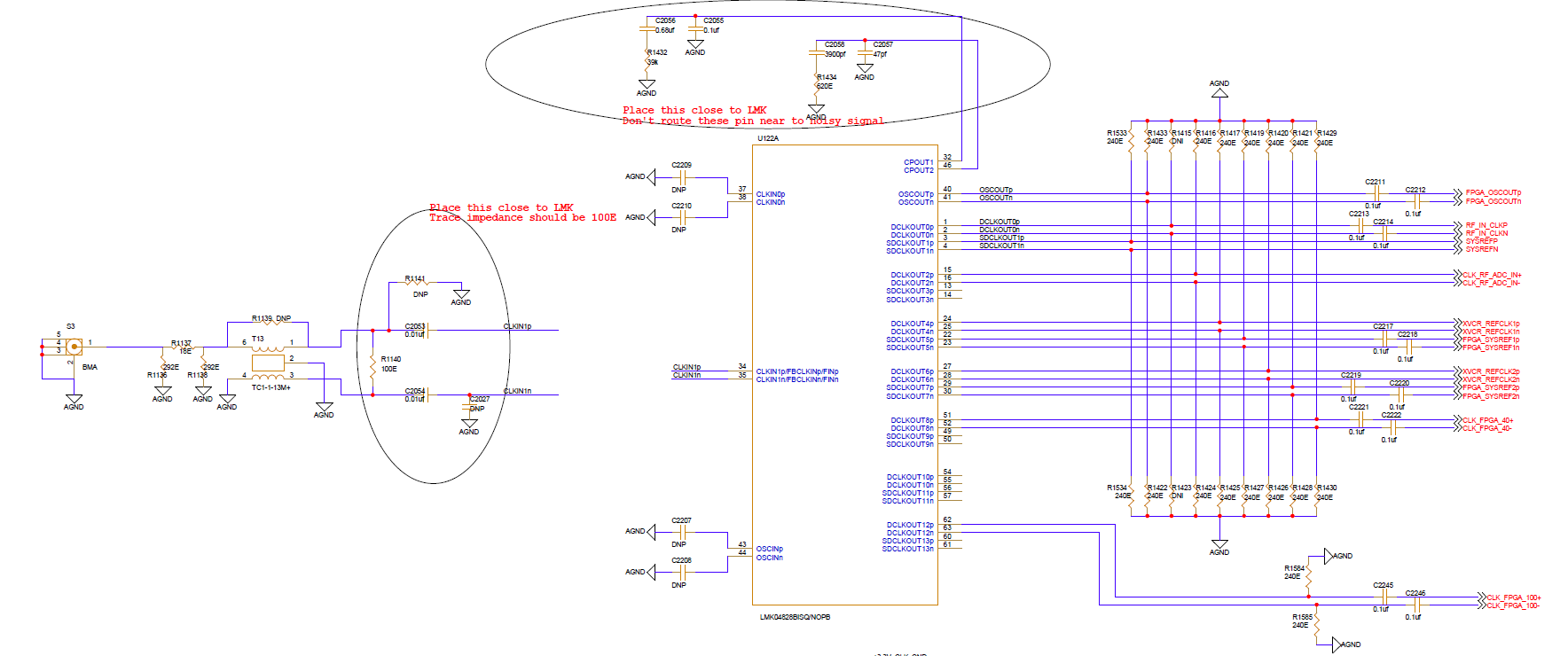
* **Clock generator block in reference schematic design:**



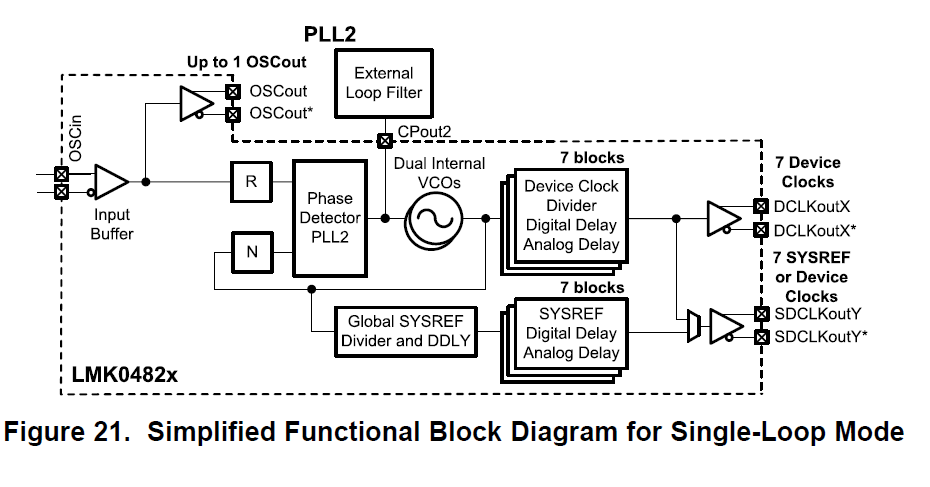
* **Clock generator block in our schematic design:**



100MHz

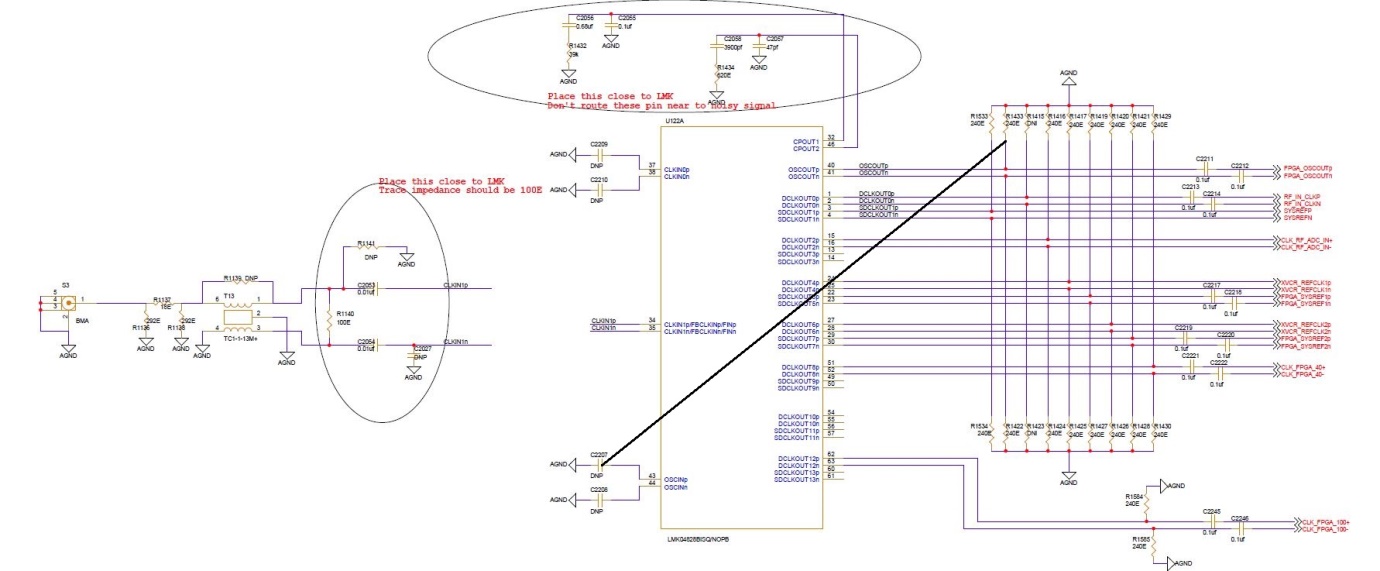
* **Changes done in clock generator block in our board after PCB assembled:**

We are working in this below configuration (only pll2 locking status)



In our schematic, crystal clock is not connected at the OSCIN, none of the output clocks are giving output.

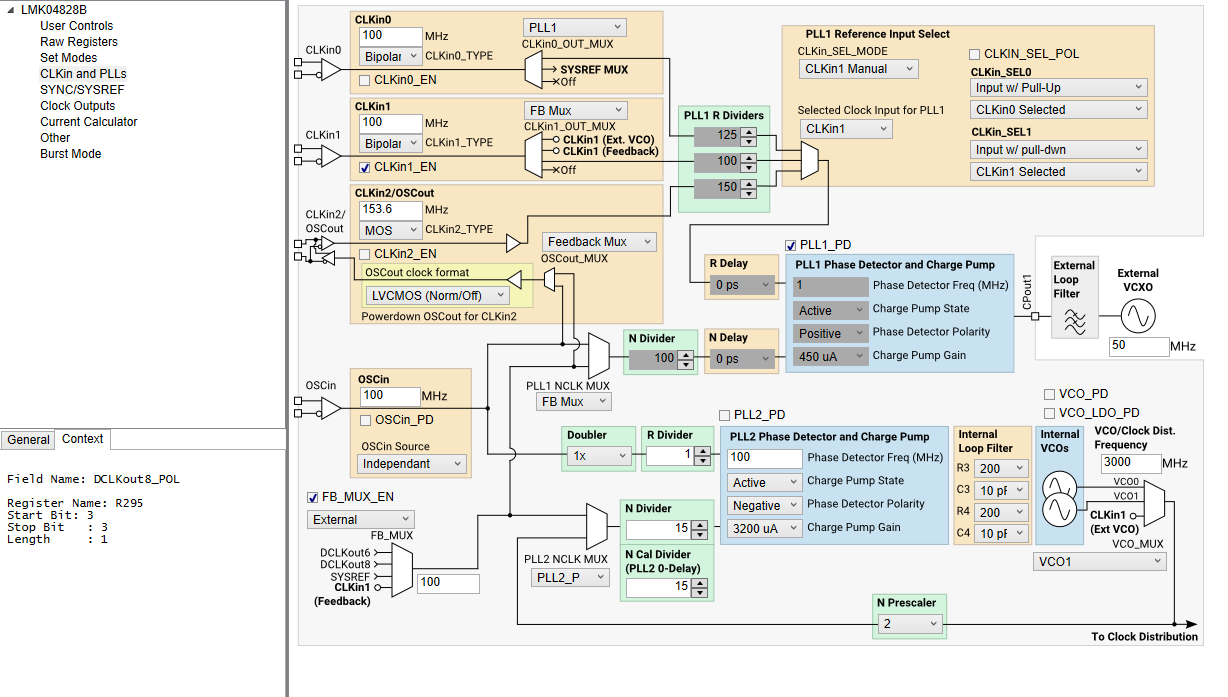
So jumper(simple wire) is connected in PCB between C2207 and R1433. Kept C2211 and C2212 as DNP.

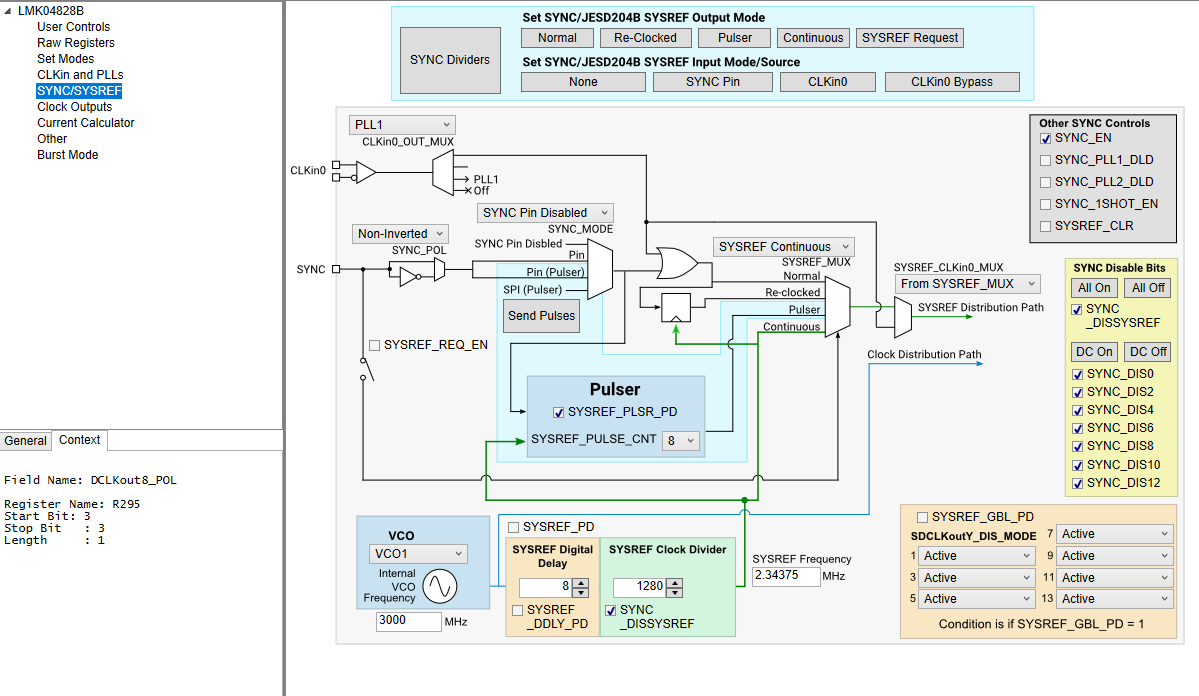


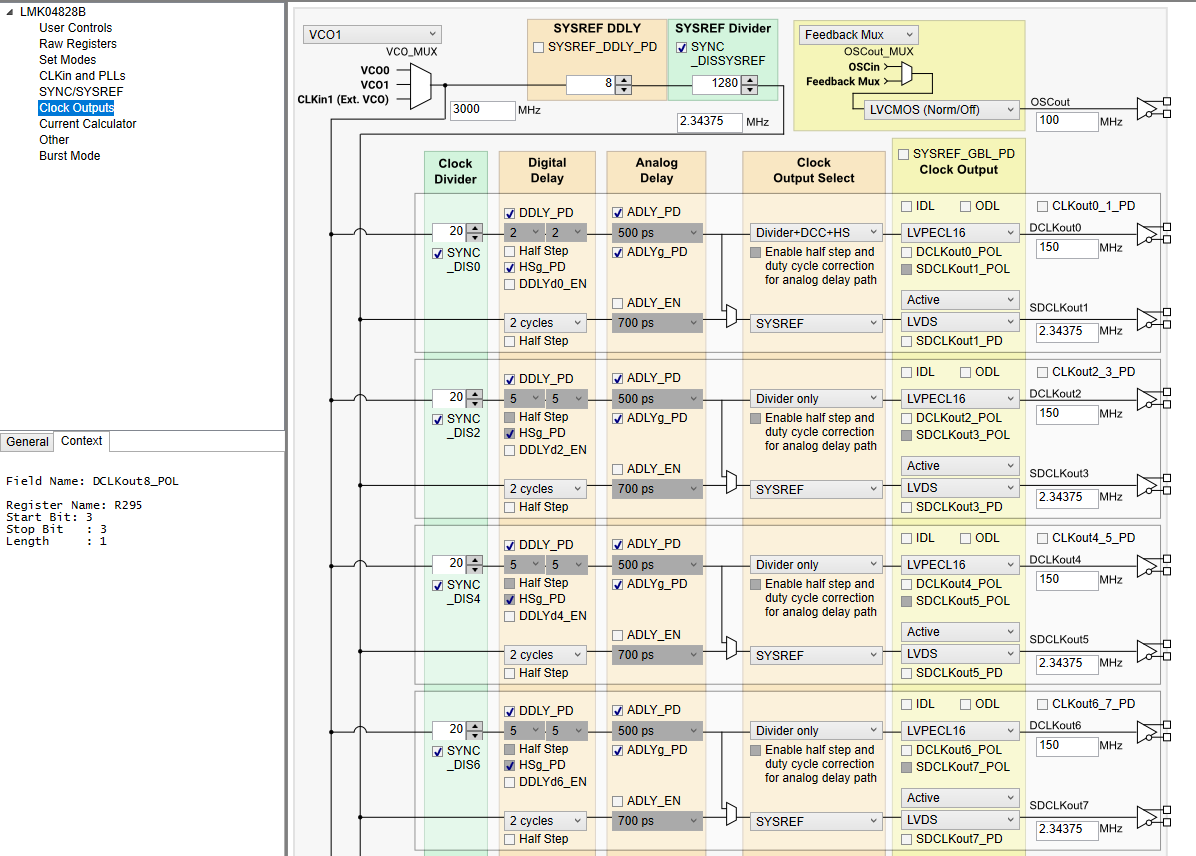
100MHz

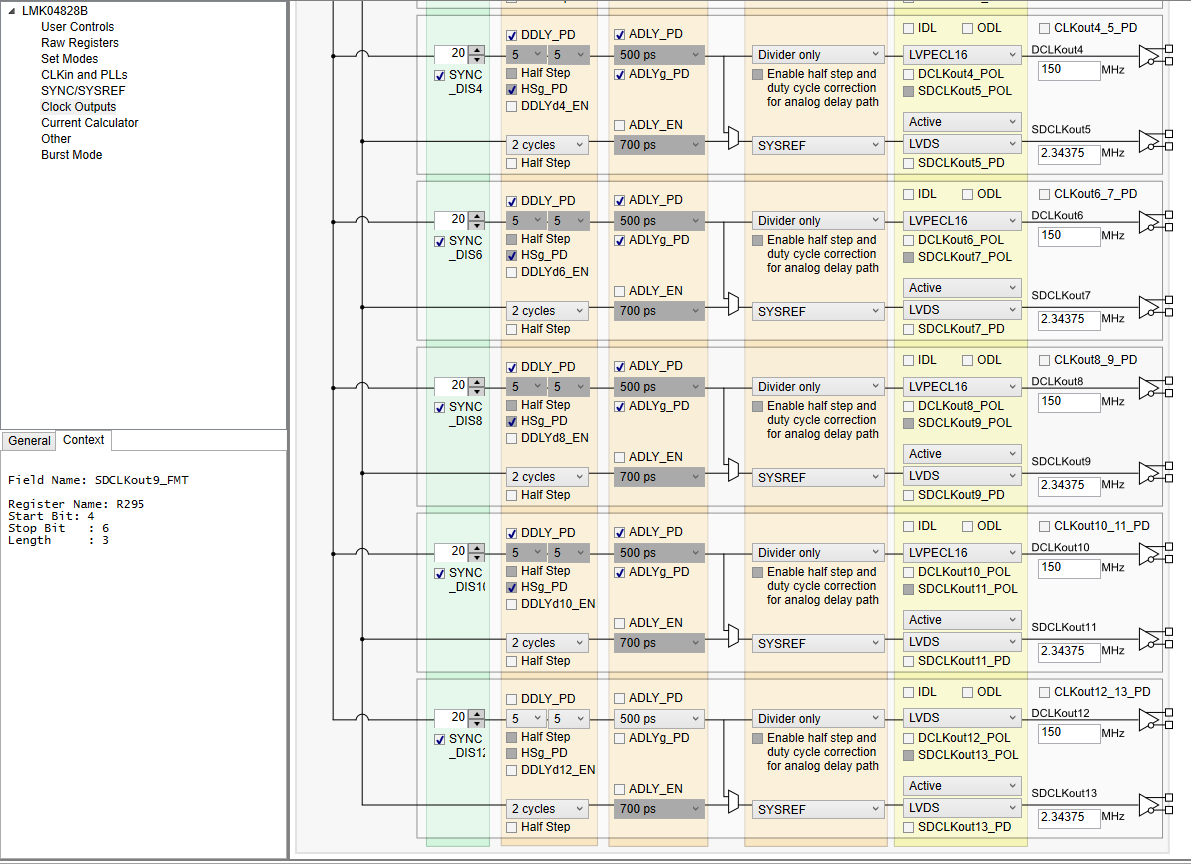
Then **Status PLL 2** is locked.

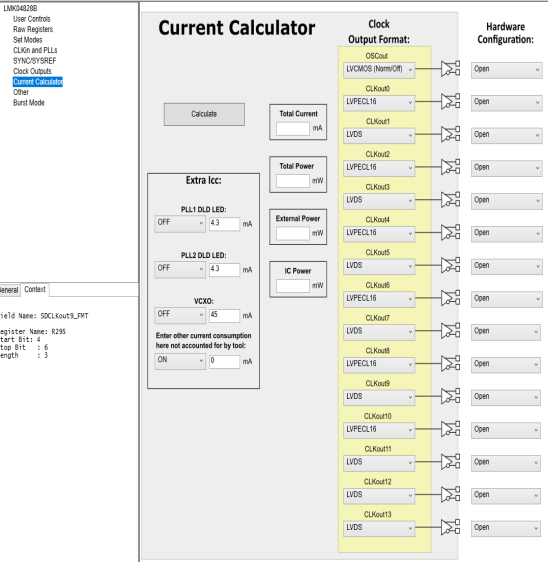
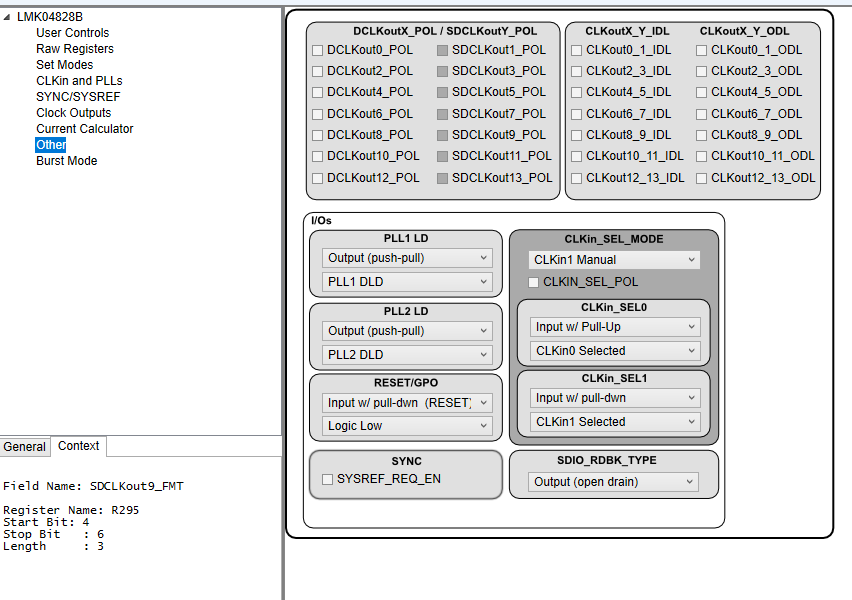
**LMK04828 GUI Settings:**









**Intel Quartus 20.2:**

* In signal tap we captured xcvr clock (150MHz) @ sampling clock of 300MHz generated using on board crystal clock 25MHz
* **DCLKOUT4** and **DCLKOUT6** clocks from clock conditioner are used as xcvr clocks







* As xcvr clock is not stable in signal tap, we tried to measure jitter using signal analyzer instrument with below settings.

LMK

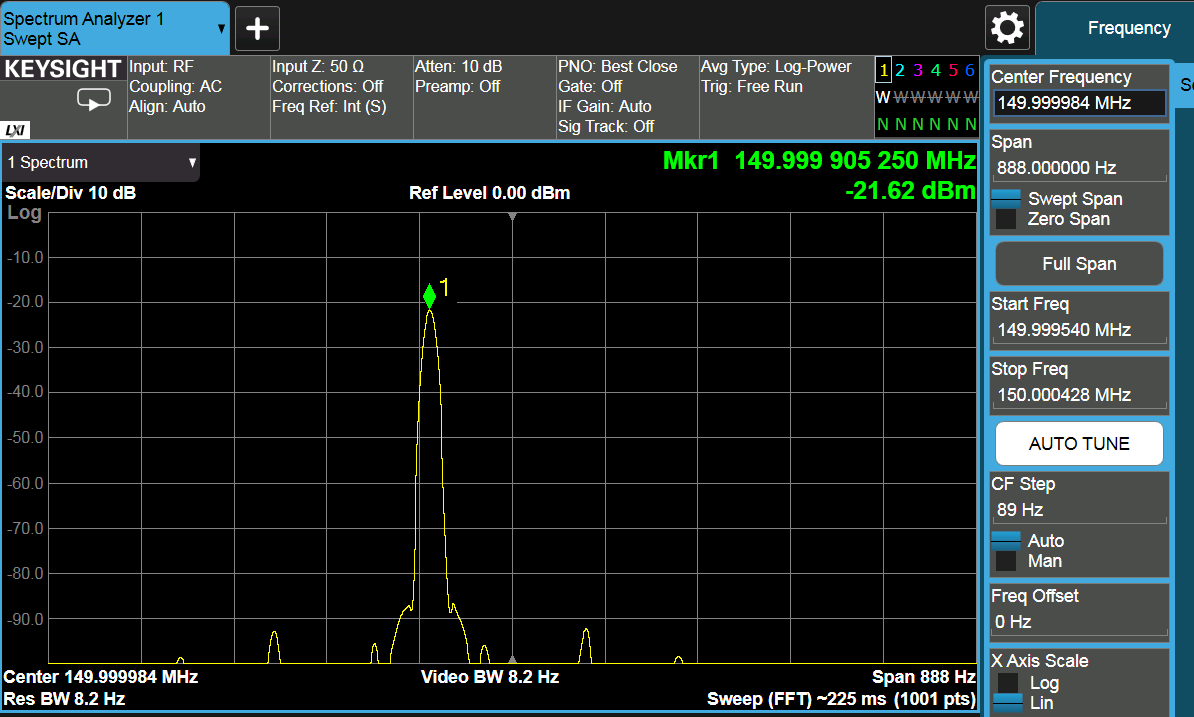
Level translator

SMA connector to Signal Analyzer

Center freq: 150MHz

Span: 1 KHz

We observed the Peak @149.999MHz which is stable always shown in below image.



1. **I/O PLL (Intel Quartus 20.2)** is getting locked with xcvr clock as input reference clock.
2. **ATX PLL (Intel Quartus 20.2)** is not locking with xcvr clock as input reference clock.