With reference to the given block diagram below.



**CASE 1:**

When we are using SYSREF (continuous) generated internally from secondary LMK and resetting 3 DACs NCO on continuous SYSREF.

All DAC NCO output are synchronized as shown for multiple power cycles.



**Does this ensure that SYSREF path from LMK is proper and synchronized?**

**CASE 2:**

Assuming in relocking mode, SYSREF from primary LMK is down streamed to secondary LMK through CLKin0.since we are using zero delay modes on secondary LMKs and we are relocking SYSREF from primary. The downstream LMK will output the SYSREF at the same time to all DACs or with some constant delay.

**SYSREF PATH**

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We have observed that in secondary LMK two DAC output are synchronized and the remaining 1DAC output is varying on power cycles as shown.

**POWER CYCLE1**



**POWER CYCLE2**

**POWER CYCLE 3**



**why this behavior is observed ?**

**CASE 3:**

we have carried out the same experiment with SYNC path and the same thing was observed.



**POWER CYCLE 1**

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**POWER CYCLE 2**

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