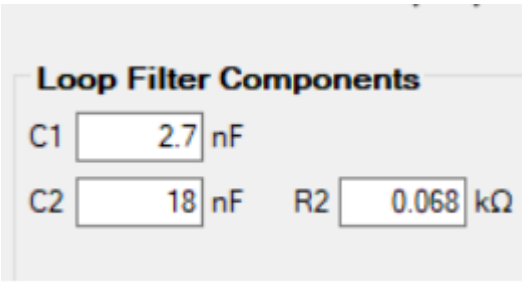
That 5μs is a typical value when switching from 7500MHz to 1500MHz. This value will vary especially with temperature as temperature will affect analog PLL lock time. For the same reason, there is no absolute lock time for a PLL. If you want tight control to the switching time, maybe you should consider to use a DAC instead of PLL.

My question: Is there a worst-case stabilization time for PLL, and in what aspects does temperature mainly affect it? This is an inherent characteristic of PLL? The temperature change in the scenario I am currently testing is not high. If it is affected by temperature, should there be a concentrated problem within a certain period of time? The probability of errors will be higher, and we now have a probability of about one in a million. In full assist mode, only one calibration is performed. Is this calibration value also problematic in scenarios where it is used for a long time? Our usage scenario is 30us per switching cycle, 10us for local oscillator locking, and 20us for communication. Is there an alternative PLL solution in this scenario.

From your timing diagram, the PLL is unlock after the second programming. Is this problem repeatable and always happen at the same frequency? If you increase the time interval between frequency switching, will this problem happen?

My question: Our usage scenario is 30us per switching cycle, 10us for local oscillator locking, and 20us for communication. PLL lock loss does not occur at a single frequency point, and the probability of this error is approximately millions of times. When used in fully assisted mode, there are two phenomena: one is that it is not locked within the specified time, and the other is that it is locked but demodulation and decoding errors occur. I have tested increasing the switching interval, and after a certain delay, the phase-locked loop will lock, but this is not suitable for our usage scenario. At the same time, I also tested 10 boards, and each board had a different status. Some boards would lock within 10us without any loss of lock status, but there would be demodulation and decoding errors. I feel that the PLL output frequency is not truly locked.Did you try using a smaller capacitor at pin 3?

For the loop filter, below configuration may return smaller PLL lock time.



My question: This has been tested and there will be the same problem. The current configuration of the loop is shown in the figure below. It is not a speed

issue, but a stability issue during pressure use. Let's focus on this issue first.

Changing the loop bandwidth cannot solve the stability problem, can it?