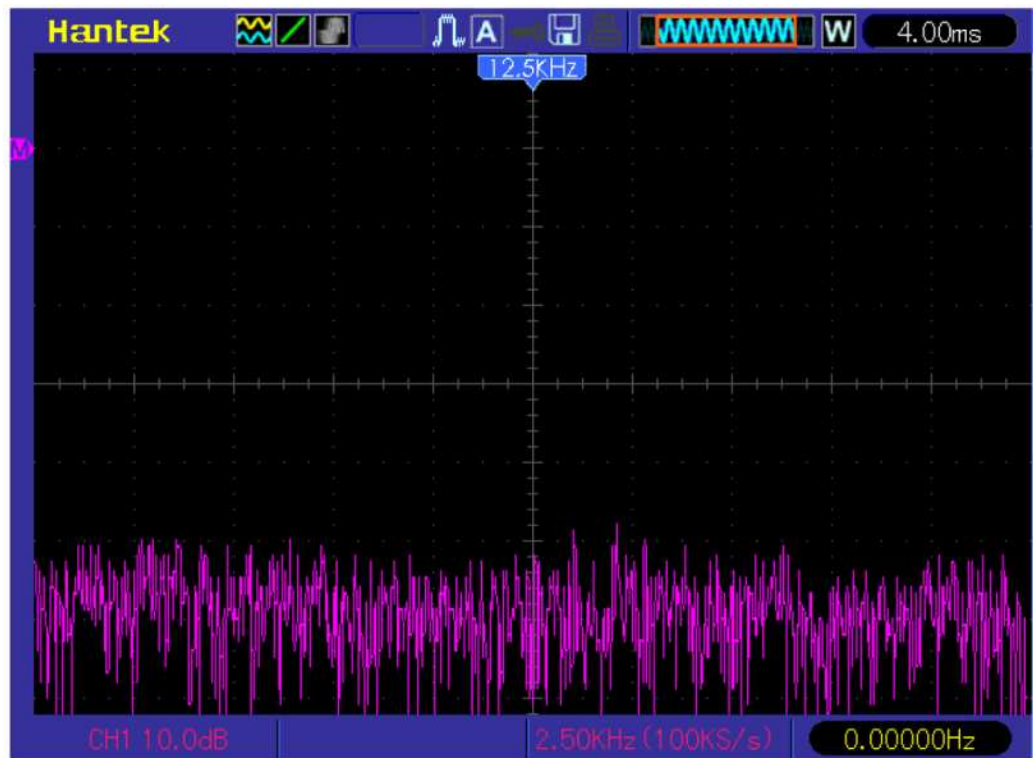
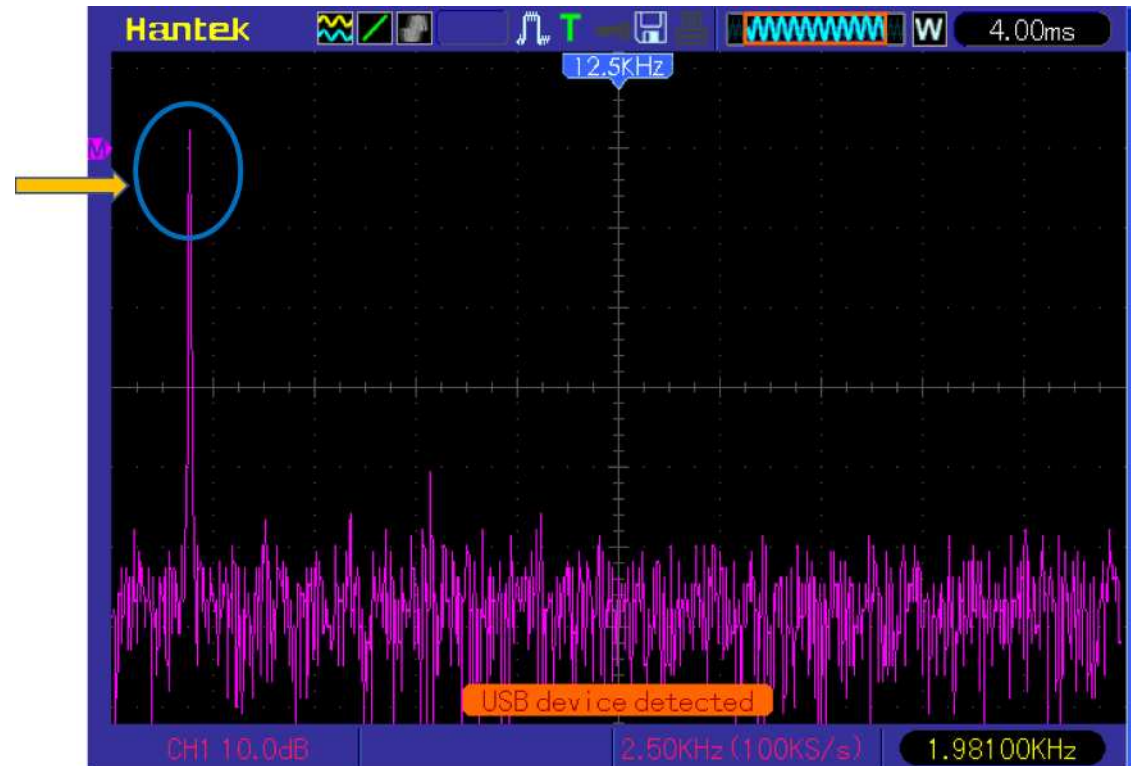


VCTCXO 20MHz Ref clock input

No modulation



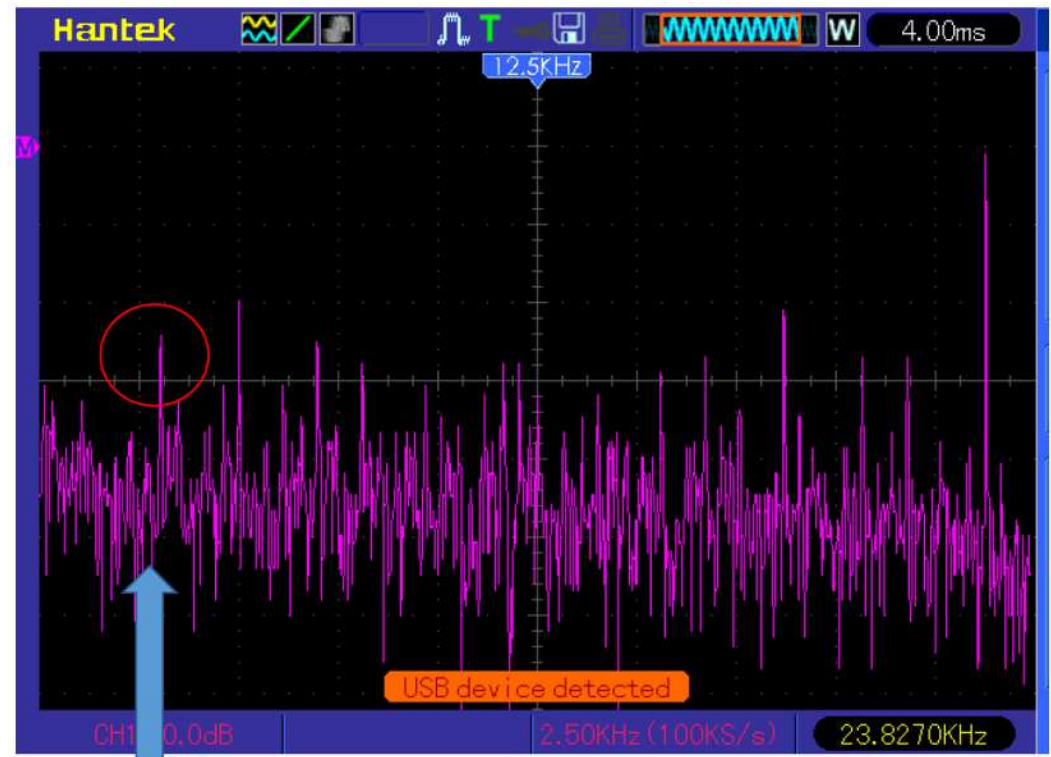
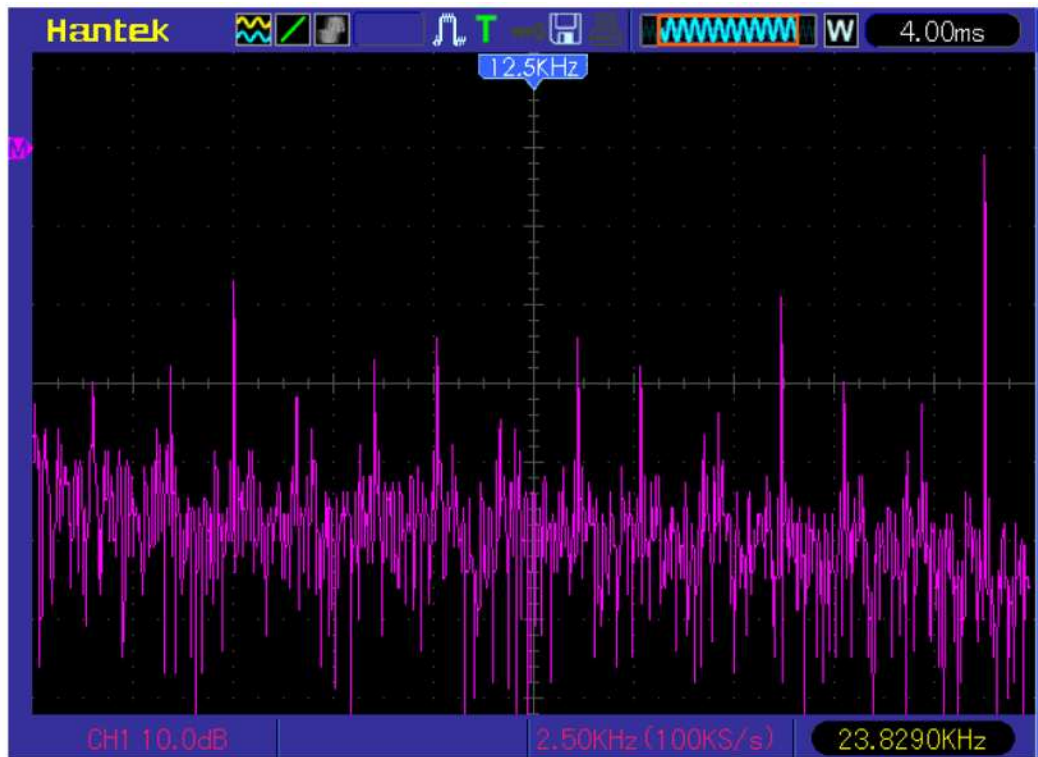
2KHz FM 5KHz deviation



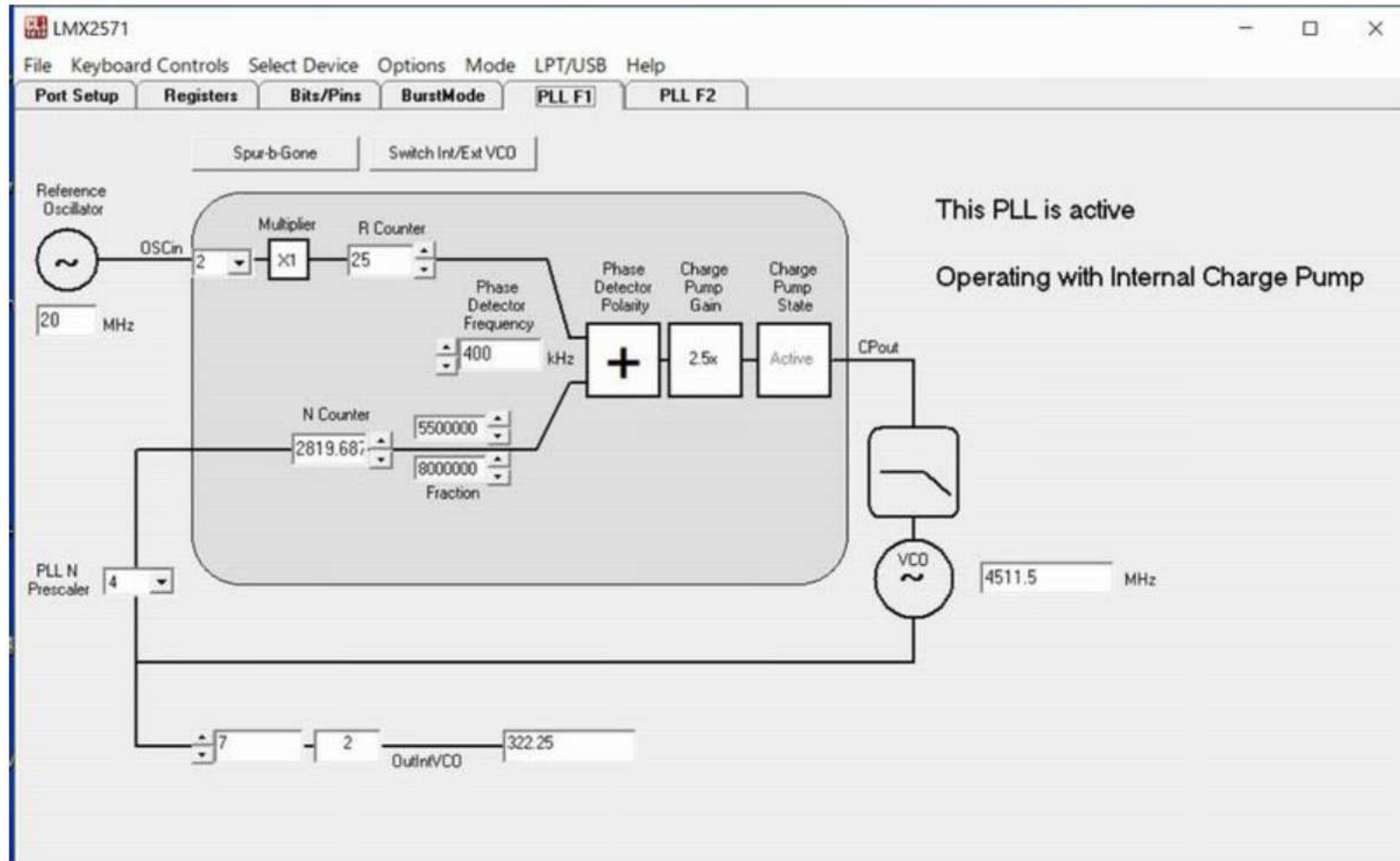
PLL output 300MHz

No modulation **Large spurious**

2KHz FM 5KHz deviation



LMX2571 EVM setting



LMX2571 EVM setting

The screenshot shows the LMX2571 configuration software interface. The 'Port Setup' tab is active, displaying the following settings:

- Communication Mode:** USB (selected), LPT (unselected). Device ID: USB2ANY - 247243510C001700. Identity button is present.
- LPT Port Setup:** Port Address: LPT1 (selected), LPT2, LPT3, Other (378). Reload Every: 10 sec.
- Pin Configuration:** A grid of 14 pins for each of the following functions: Clock Bit, Data Bit, LE Bit, CE, MUXout, TrCl, and TRIGGER. Pin 8 is selected for all functions.
- USB2ANY Port Setup:** Legend for Clock (blue), Data (green), LE (Latch Enable) (purple), Reserved (grey), Other Pins (grey), Ground (black), Address Conflict (red), and Input (yellow). A diagram of a 10/14 Pin Connector (Top View) shows Pin 1 is connected to the purple pin.

The screenshot shows the LMX2571 configuration software interface with the 'Registers' tab active. The settings are organized into several columns:

- General Config:** FCAL_EN (checked), POWERDOWN (unchecked), RESET (unchecked), SDO_LD_SEL (Lock detect output).
- Charge Pump:** CP_GAIN (2.5x), CP_IUP (1250 uA), CP_IDN (2343.0 uA), EXTVC0_CP_POL (EXTVC0_CP_GAIN), EXTVC0_CP_IUP (1250 uA), EXTVC0_CP_IDN (1250 uA).
- General PLL:** DITHERING (Medium).
- General MULT:** MULT_WAIT (390).
- Output Buffer:** OUTBUF_RX_TYPE (Push pull), OUTBUF_TX_TYPE (Push pull), OUTBUF_AUTOMUTE (Rx:TX_POL, Active LOW = TX, Rx:TX_CTRL, Program register).
- F1F2 Switch Control:** F1F2_MODE (checked), F1F2_INIT (unchecked), F1F2_CTRL (Use F1F2_SEL bit), F1F2_SEL (F1 registers).
- F1 Registers:** PLL_R_PRE_F1 (2), MULT_F1 (1), FRAC_ORDER_F1 (1st Order), PFD_DELAY_F1 (4), CHDIV1_F1 (7), CHDIV2_F1 (2), LF_R3_F1 (800 ohms), LF_R4_F1 (800 ohms).
- F2 Registers:** PLL_R_PRE_F2 (1), MULT_F2 (4), FRAC_ORDER_F2 (3rd Order), PFD_DELAY_F2 (4), CHDIV1_F2 (7), CHDIV2_F2 (2), LF_R3_F2 (800 ohms), LF_R4_F2 (800 ohms).
- General FSK Settings:** FSK_MODE_SEL1 (unchecked), FSK_MODE_SEL0 (unchecked), FSK_DEV_SPI_FAST (0), FSK_DEV_SEL (0), FSK_LEVEL (FSK disabled), FSK_I2S_CLK_POL (Rising edge), FSK_I2S_FS_POL (Active HIGH).