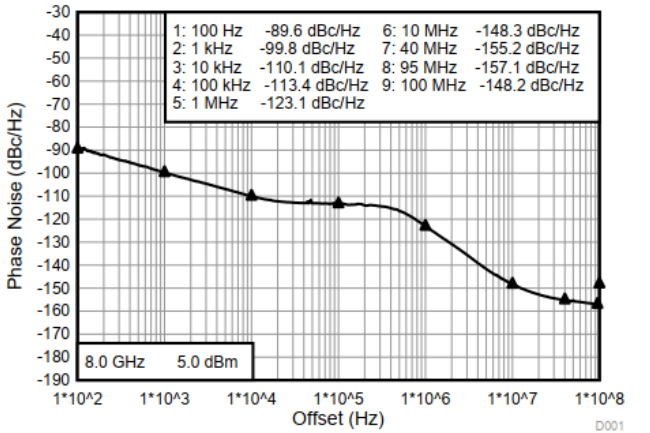
PLL – Test

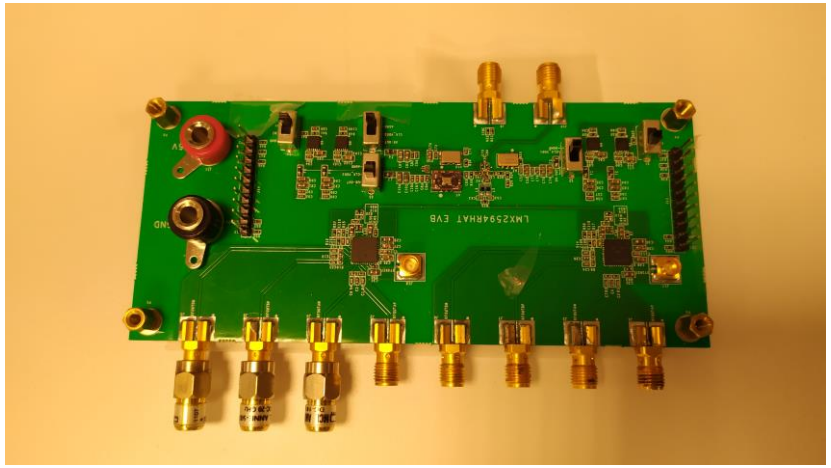
PLL – LMX2594

- Crystal Clock Measurement
- PLL Measurement



f_{OSC} = 100 MHz
f_{PD} = 200 MHz
Jitter = 46.87 fs (100 Hz - 100 MHz)

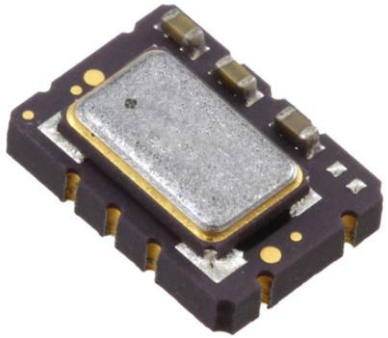
Figure 7. Closed-Loop Phase Noise at 8 GHz



TCXO - TB612

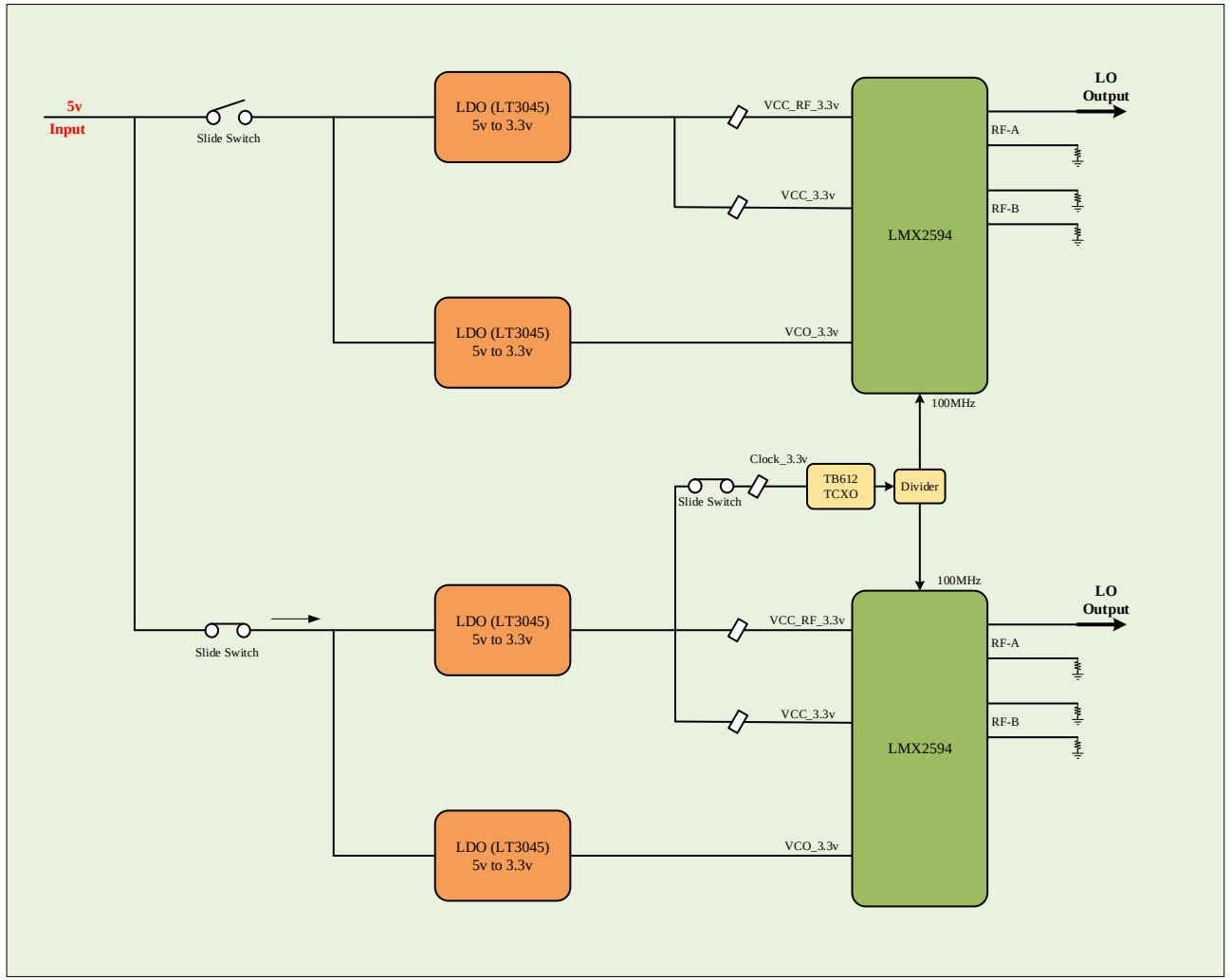
Part Number : TB612-100.0M

TVB	5	0	4	- 010.0M
Type / Package TCXO / VCTCXO Series TB = 5.0x7.0 mm 10 Pads TVB = 5.0x7.0 mm 4 Pads	Temperature Range 3 = 0 to 85 °C 5 = 0 to 70°C 6 = -40 to 85°C 7 = -20 to 70°C	Frequency Stability 0 = ±0.28 ppm 1 = ±0.50 ppm 2 = ±1.00 ppm 3 = ±2.00 ppm	Features 2 = TCXO, LVCMOS, 3.3 Vdc 3 = TCXO, Clipped Sinewave, 3.3 Vdc 4 = VCTCXO, LVCMOS, 3.3 Vdc 5 = VCTCXO, Clipped Sinewave, 3.3 Vdc 9 = VCTCXO, LVCMOS, 3.3V with reduced pull range	Output Frequency Frequency Format -xxx.xM Min* -xxx.xxxxxxM Max* *Minimum of 1 digit after the decimal point, and Maximum of 6

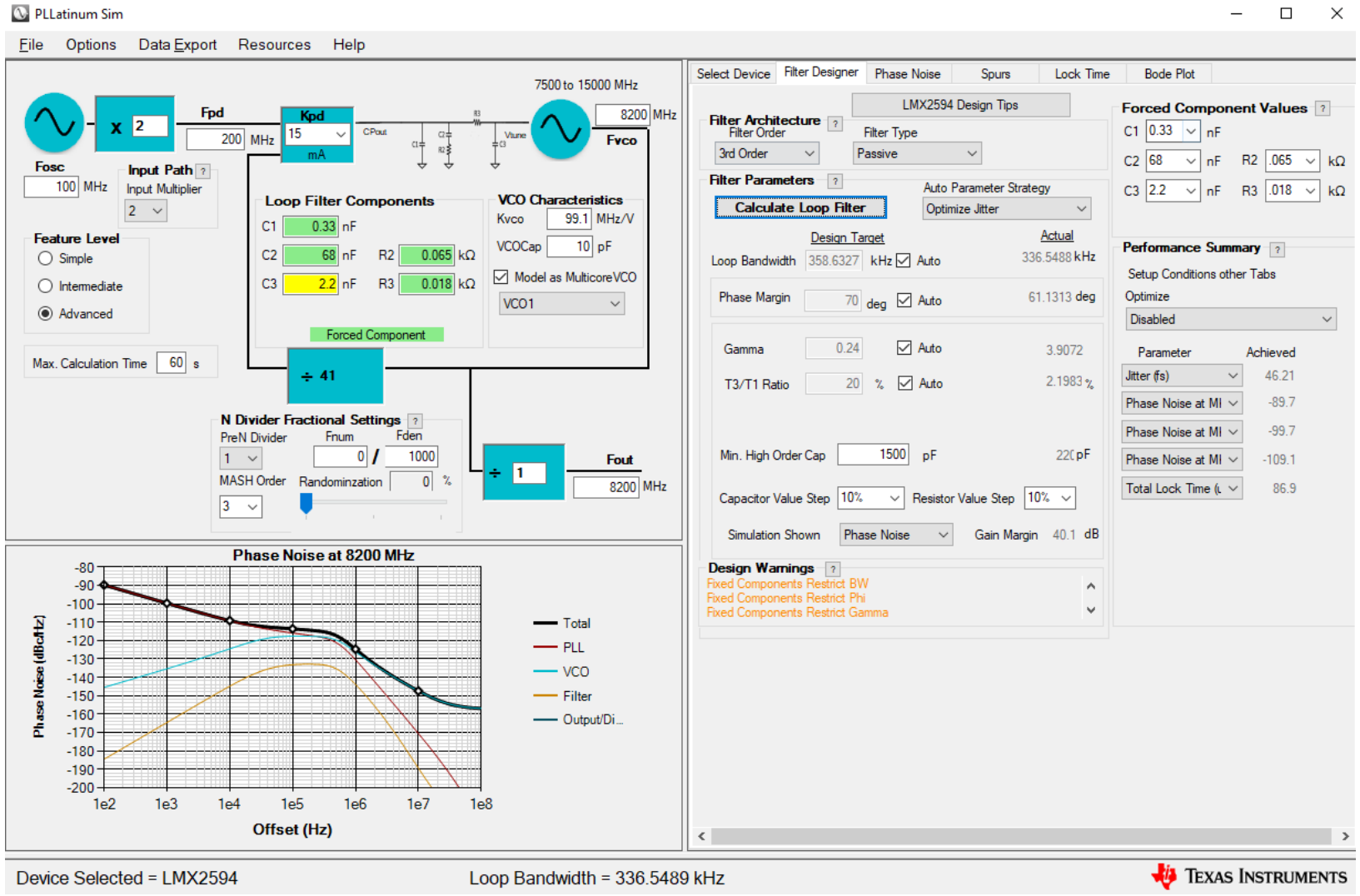


Typical SSB Phase Noise For Fo	10.0 MHz	50.0 MHz	100.0 MHz	
@ 10 Hz offset	-98	-70	-60	dBc/Hz
@ 100 Hz offset	-125	-100	-91	dBc/Hz
@ 1 KHz offset	-143	-122	-119	dBc/Hz
@ 10 KHz offset	-151	-145	-142	dBc/Hz
@ 100 KHz offset	-152	-150	-153	dBc/Hz
@ 1 MHz offset	-155	-152	-153	dBc/Hz

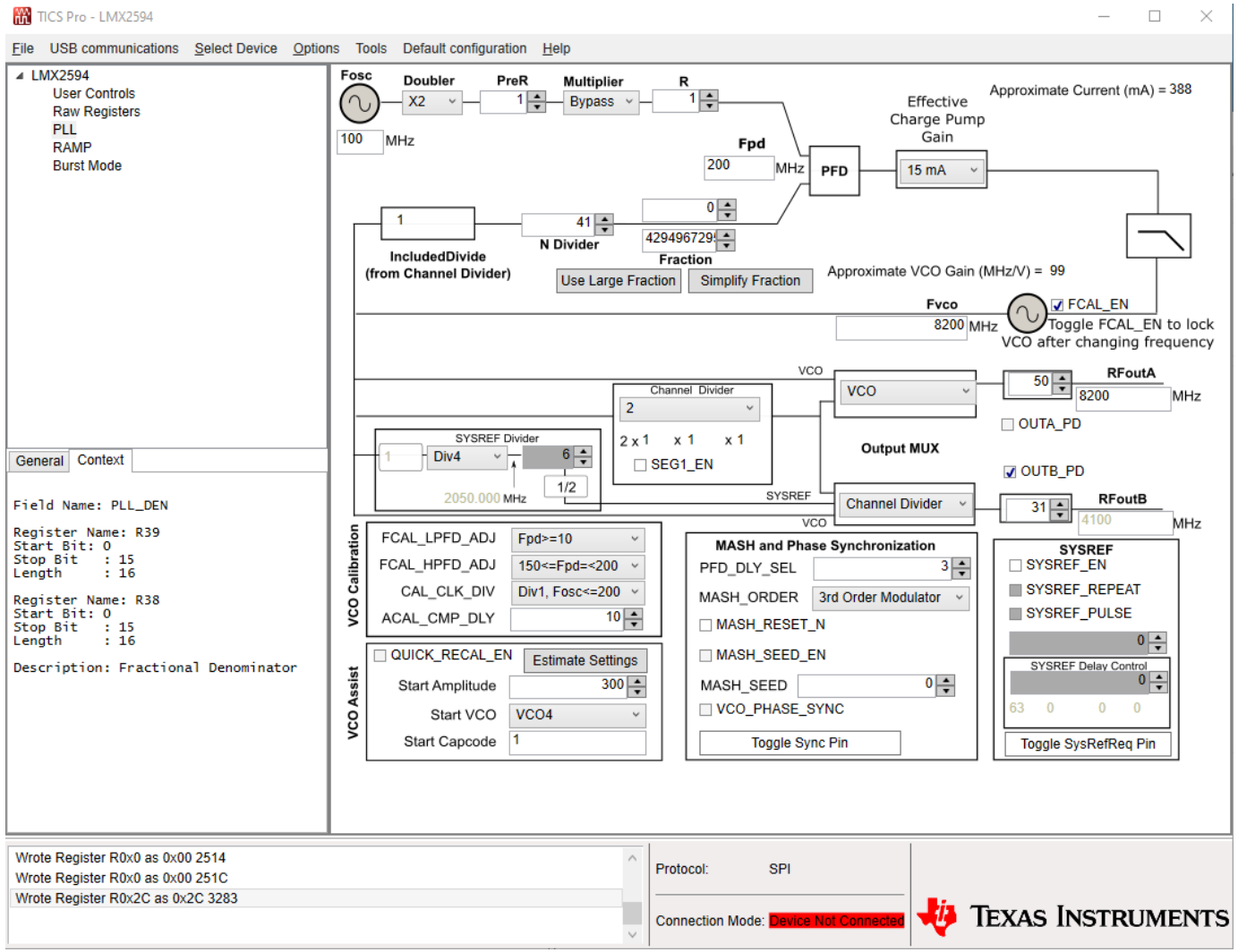
PLL Test PCB Power Rail



Loop Filter


PLLatinum Sim
File
Options
Data Export
Resources
Help
7500 to 15000 MHz
x 2
Fpd
200 MHz
Kpd
15
mA
8200 MHz
Fvco
Fosc
100 MHz
Input Path
Input Multiplier
2
Feature Level
Simple
Intermediate
Advanced
Max. Calculation Time
60 s
Loop Filter Components
C1 0.33 nF
C2 68 nF
R2 0.065 kΩ
C3 2.2 nF
R3 0.018 kΩ
VCO Characteristics
Kvco 99.1 MHz/V
VCOCap 10 pF
Model as MulticoreVCO
VCO1
Forced Component
÷ 41
N Divider Fractional Settings
PreN Divider
Fnum
Fden
1
0
1000
MASH Order
Randominzation
0 %
3
÷ 1
Fout
8200 MHz
Phase Noise at 8200 MHz
Phase Noise (dBc/Hz)
Offset (Hz)
Total
PLL
VCO
Filter
Output/Di...
Select Device
Filter Designer
Phase Noise
Spurs
Lock Time
Bode Plot
LMX2594 Design Tips
Filter Architecture
Filter Order
3rd Order
Filter Type
Passive
Filter Parameters
Calculate Loop Filter
Auto Parameter Strategy
Optimize Jitter
Design Target
Actual
Loop Bandwidth 358.6327 kHz Auto 336.5488 kHz
Phase Margin 70 deg Auto 61.1313 deg
Gamma 0.24 Auto 3.9072
T3/T1 Ratio 20 % Auto 2.1983 %
Min. High Order Cap 1500 pF 220 pF
Capacitor Value Step 10%
Resistor Value Step 10%
Simulation Shown Phase Noise
Gain Margin 40.1 dB
Design Warnings
Fixed Components Restrict BW
Fixed Components Restrict Phi
Fixed Components Restrict Gamma
Forced Component Values
C1 0.33 nF
C2 68 nF R2 .065 kΩ
C3 2.2 nF R3 .018 kΩ
Performance Summary
Setup Conditions other Tabs
Optimize
Disabled
Parameter
Achieved
Jitter (fs) 46.21
Phase Noise at MI -89.7
Phase Noise at MI -99.7
Phase Noise at MI -109.1
Total Lock Time (u 86.9
Device Selected = LMX2594
Loop Bandwidth = 336.5489 kHz
Texas Instruments

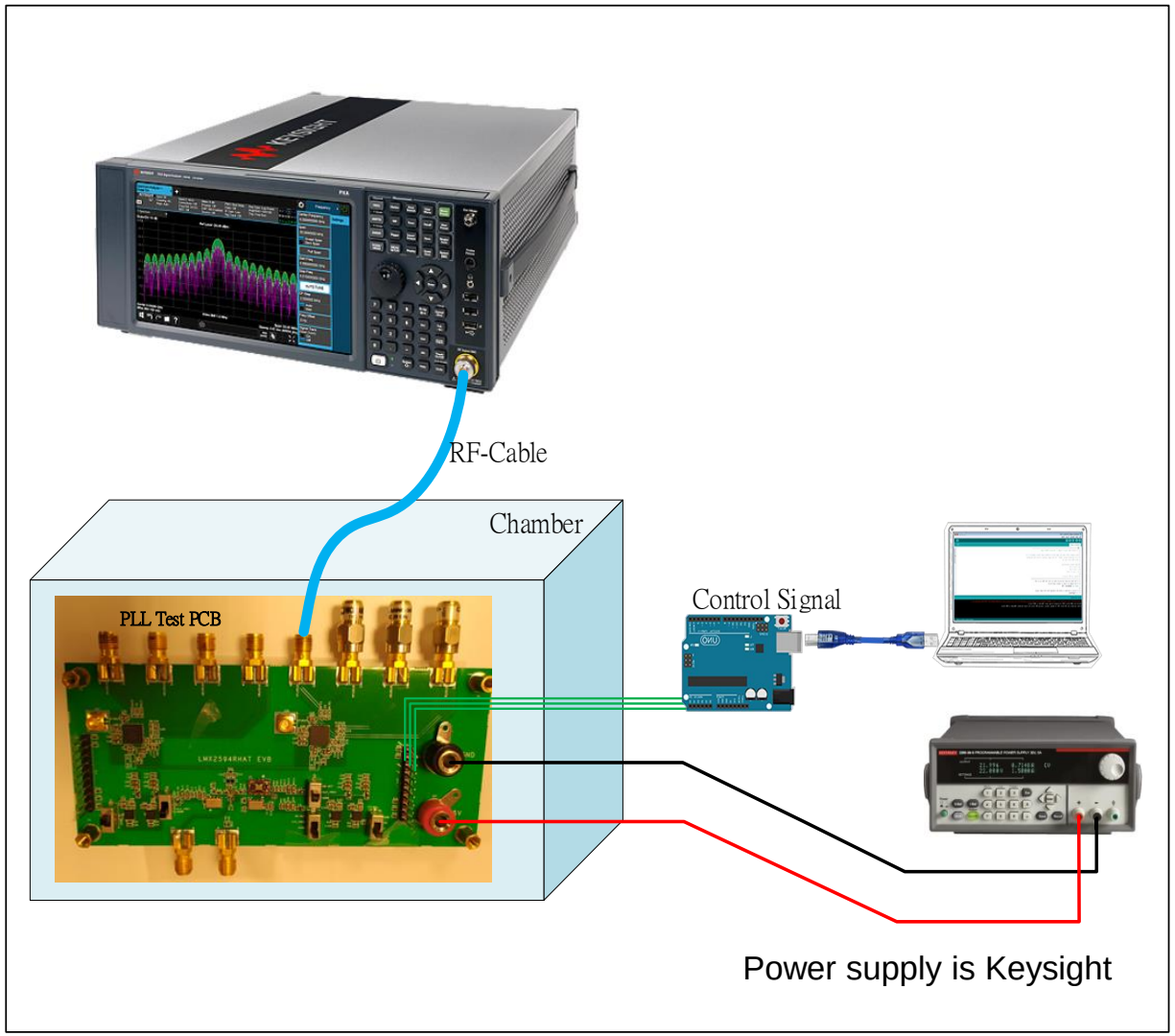
Configured Register Setup



Note:

- We exported the raw register data from Tics-Pro and send it through Arduino.

Test Setup

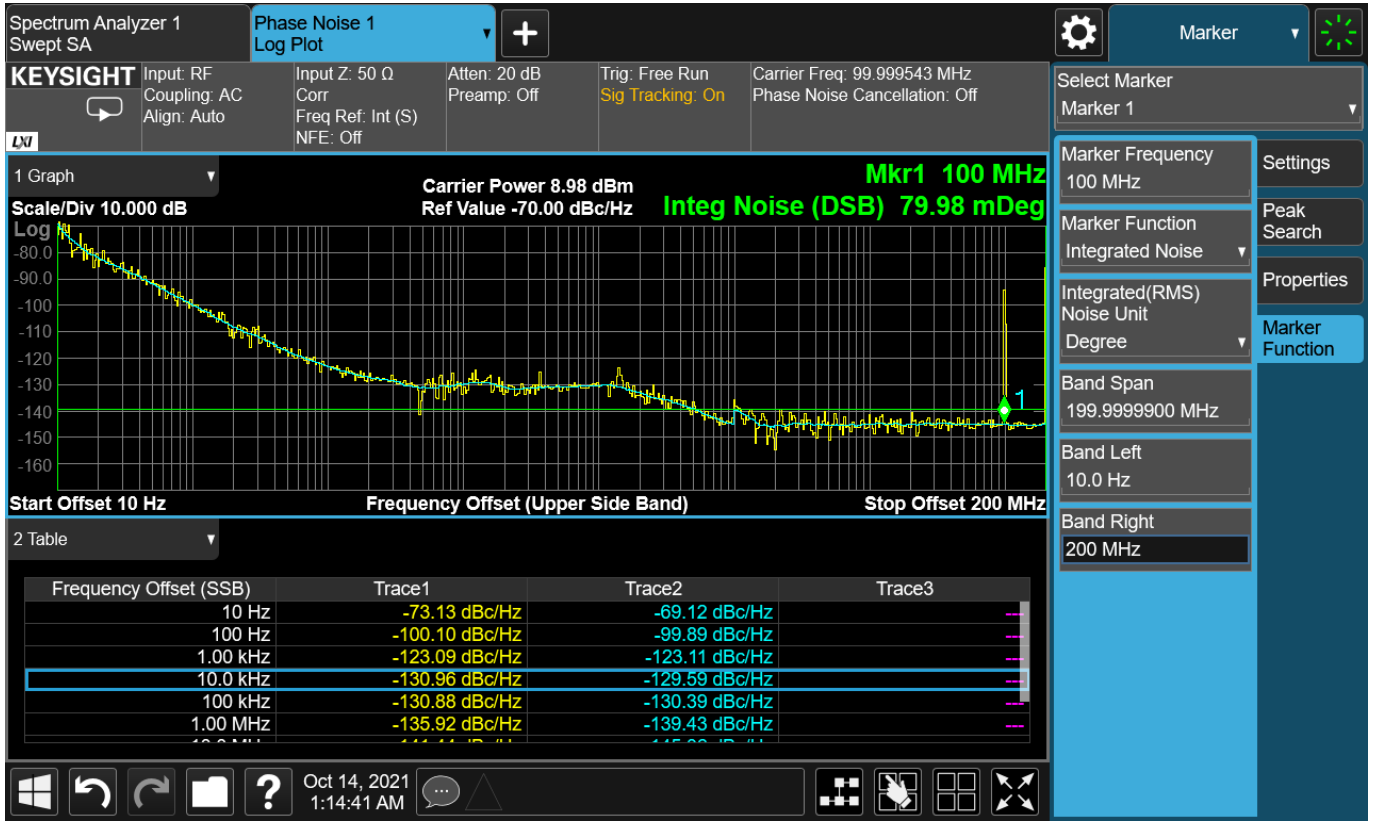


Note:

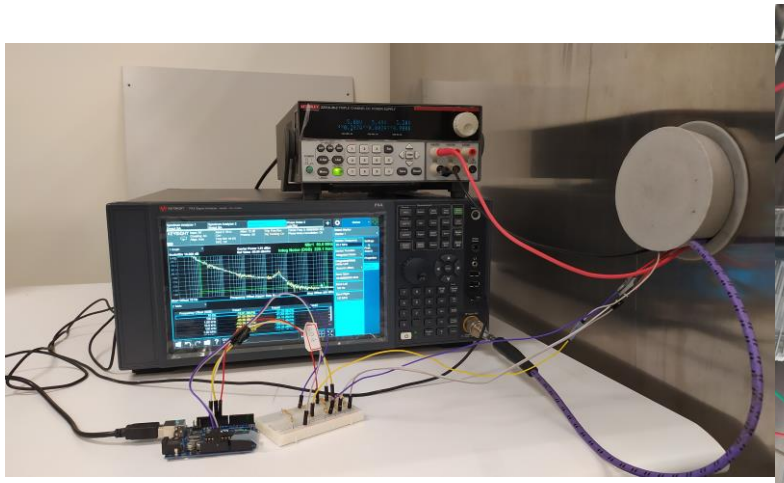
- We used Arduino + Python to send the register data

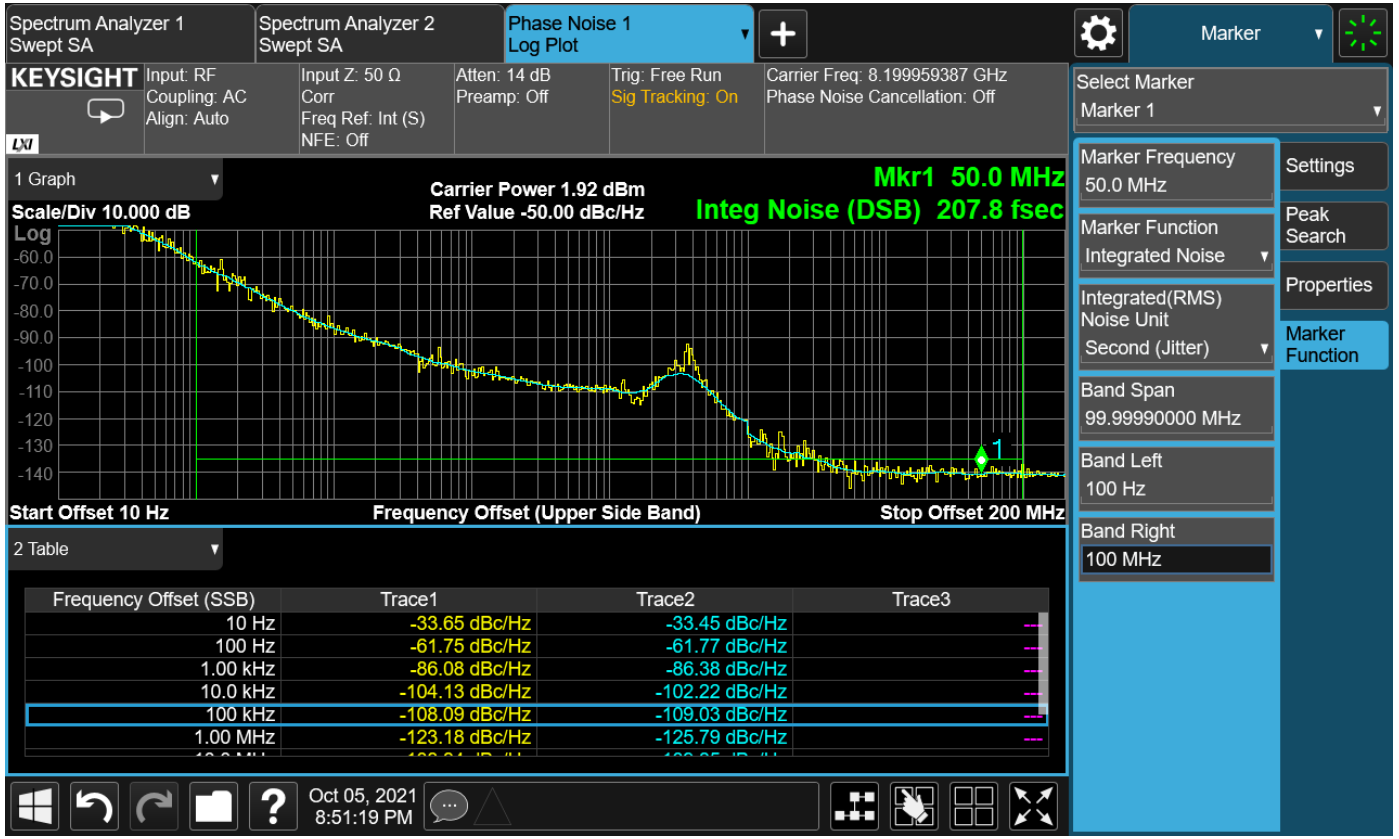
TCXO – Phase Noise

Frequency offset	Data Sheet	Measurement	Units
10Hz	-60	-73	dBc/Hz
100Hz	-91	-100	dBc/Hz
1kHz	-119	-123	dBc/Hz
10kHz	-142	-131	dBc/Hz
100kHz	-153	-130	dBc/Hz
1MHz	-153	-145	dBc/Hz



PLL Phase Noise





1. Machines Used

   Power Supply - Keithley 2231A-30-3

   Signal Analyzer - Keysight PXA Signal Analyzer N9030B

Note:

- We measured Both IC’s, both results are same. But, the Phase noise is not good at Low Frequency compared to the datasheet.
- Also, let me know if any issue in my Test setup or Layout or schematic. I amWaiting for you valuable Timed Reply.

Thank You