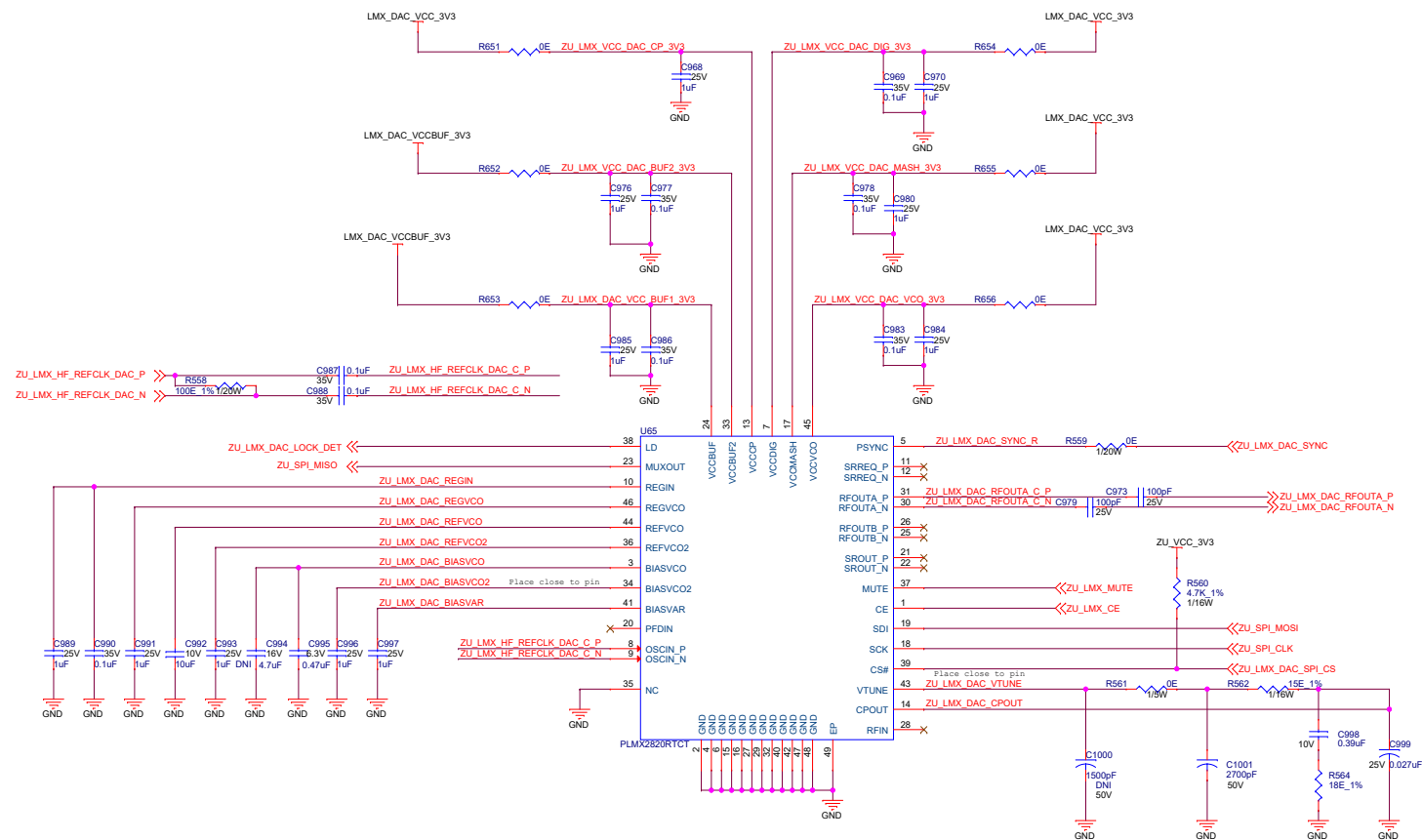
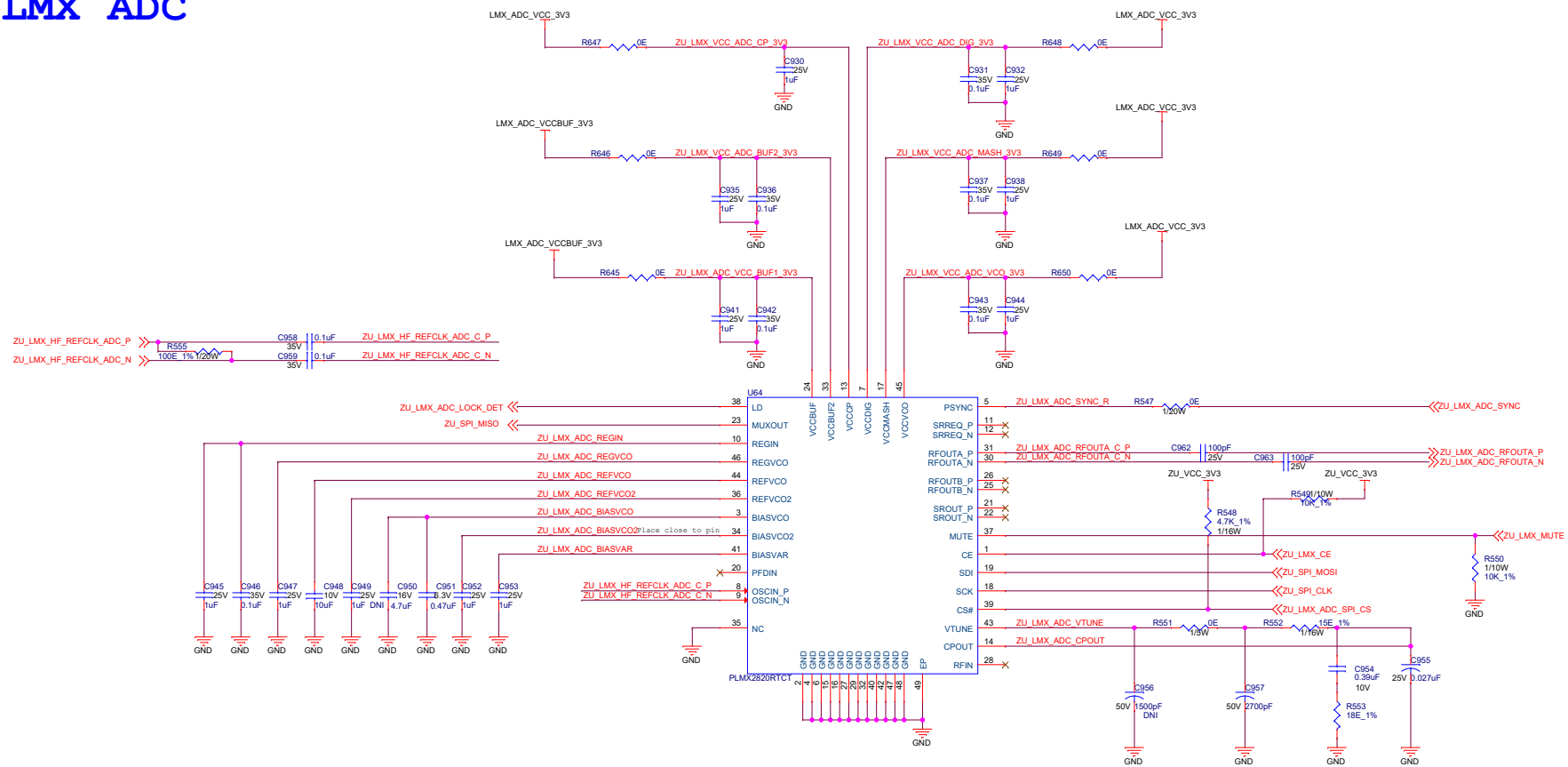


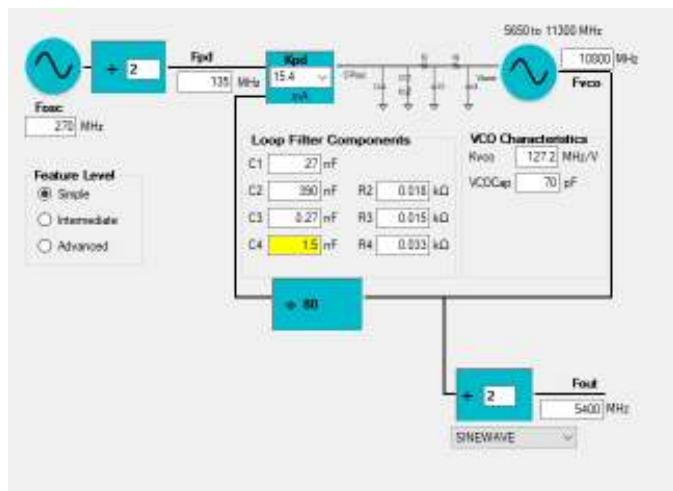
LMX DAC



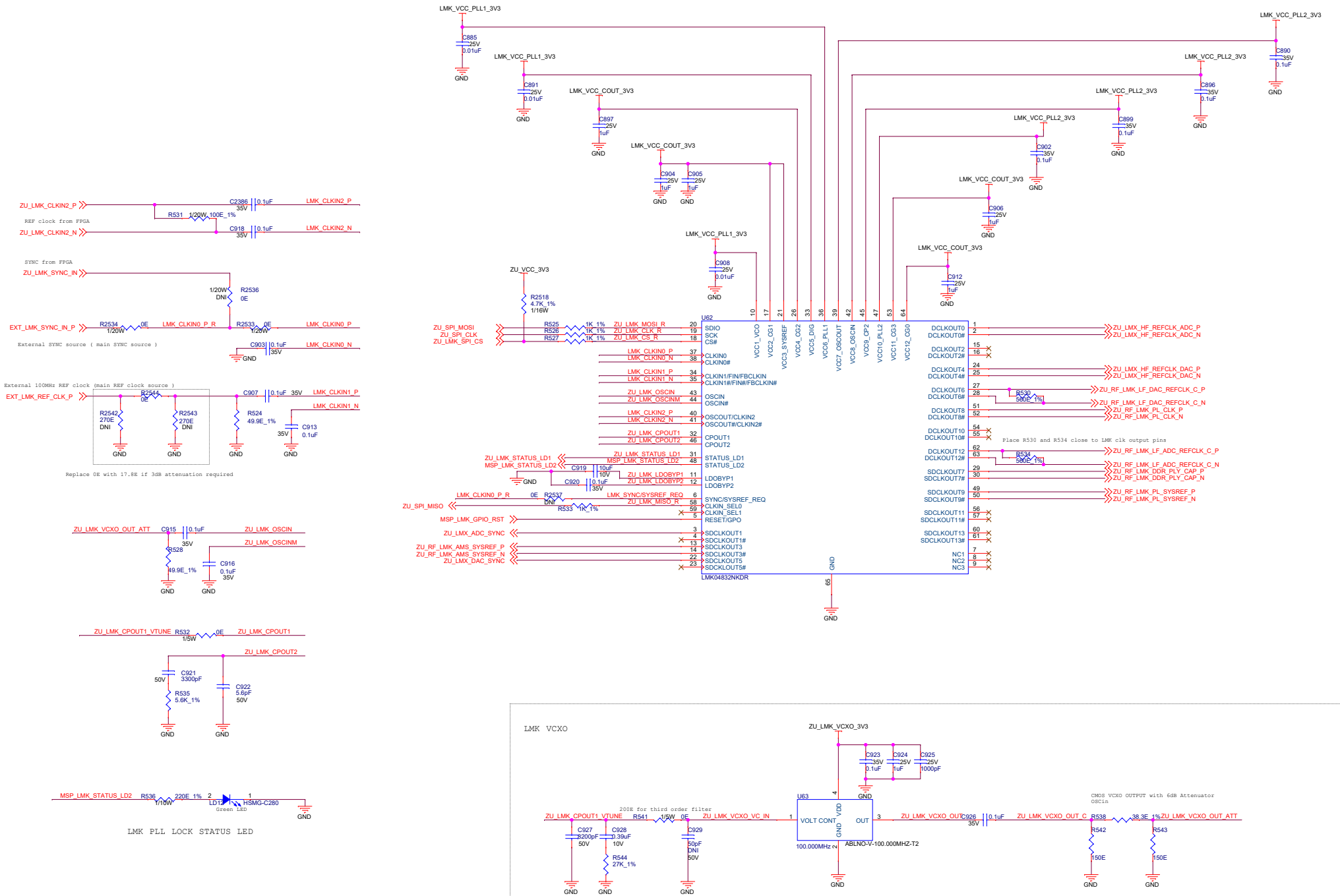
LMX ADC



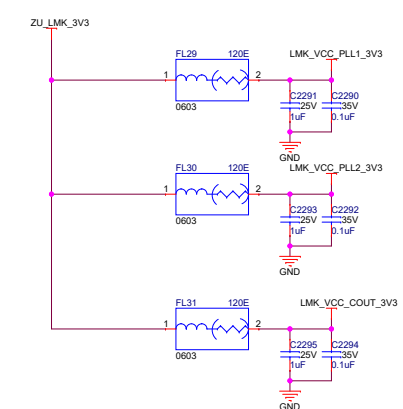
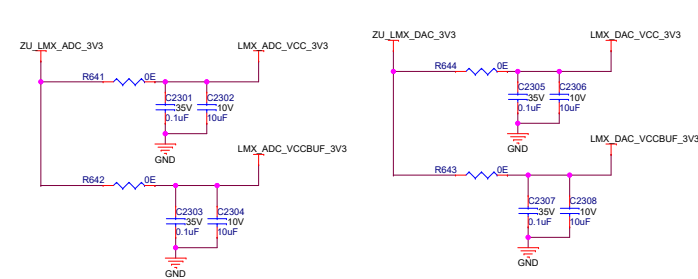
Loop Filter calculation

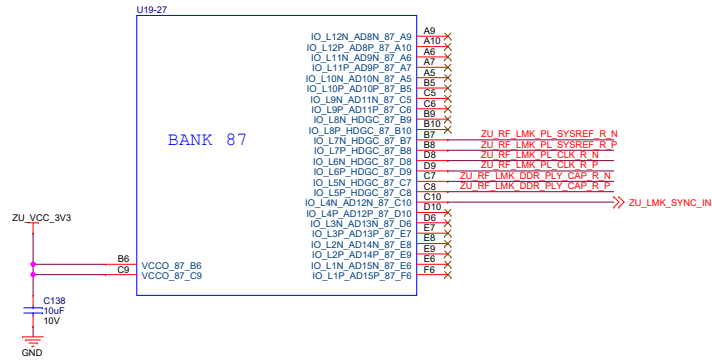


LMK CLOCK GENERATOR



The schematic diagram shows the U48 TPS7A8901RTJR regulator circuit. The input is VSYS_5V0, which is connected to the IN1_1 pin (pin 1) and the IN2_1 pin (pin 4) through a network of capacitors C738 (10uF, 10V) and C739 (10uF, 10V). The output of the regulator is connected to the ZU_LMX_DAC_3V3 pin (pin 14) and the ZU_LMX_ADC_3V3 pin (pin 15). The feedback network consists of resistors R461 (100k, 1%), R462 (100k, 1%), R464 (100k, 1%), and R465 (100k, 1%), and capacitors C737 (10.01uF, 25V), C740 (0.1uF, 25V), C741 (0.1uF, 35V), C744 (22uF, 25V), C745 (0.1uF, 35V), and C748 (0.01uF, 25V). The circuit also includes the UCD_ZU_LMX_REG_EN signal and the UCD_ZU_LMX_REG_EN pin (pin 20).





TERMINATION FOR LMK CLKs

