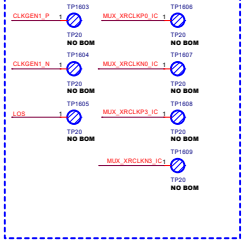
Clock Generator

NOTE: 需要額外跟LAYOUT說明Bypass MUX的電組需要lay在BOT side for減少幾段影響訊號品質

Test point



Note.

1. PT505801 GPIO 10/11 接到 clk gen (pin 3 & 4)控制 clk gen SRIS -0.25%
2. Clk gen (pin 1) 用POR或者1V8 GPIO加上RC delay緩路拉 LOW 控制 clk gen output 0 輸出給 Mux

REF_CLRL	BUF_SEL/I2C	I2C address
LOW	LOW	0X68
LOW	HIGH	0X69

REF_CLK	MODE
LOW	I2C MODE
HIGH	OTP MODE

PWRDN	MODE
LOW	PN MODE
HIGH	PG MODE

CLKIN_SEL_tri	CLKIN0	CLKIN1
LOW	V	X
MID(NOTE1)	V	V
HIGH	X	V

NOTE1: MID mode (1.8V)
CLKIN0 in for CLK0 & CLK1 out
CLKIN1 in for CLK2 & CLK3 out

Note.

1. GPIO 23 接到 Mux (pin 8)，控制 Mux CLKIN0 /1
2. CLKIN 0 default Clk gen，CLKIN 1 default Host REFCLK

ZOUTSEL	BUF_SEL
LOW	85 Ω
HIGH	100 Ω

vSMB_EN	SMB_Function	PIN_8	PIN_9
LOW	X	CKLIN_SEL_tri	OE3#
HIGH	V	SMB_DATA	SMB_CLK

OE#	CLK
LOW	V
HIGH	X

#OE# Output Enable for CLK1 Active Low

OE0對應CLK0, OE1對應CLK1以此類推