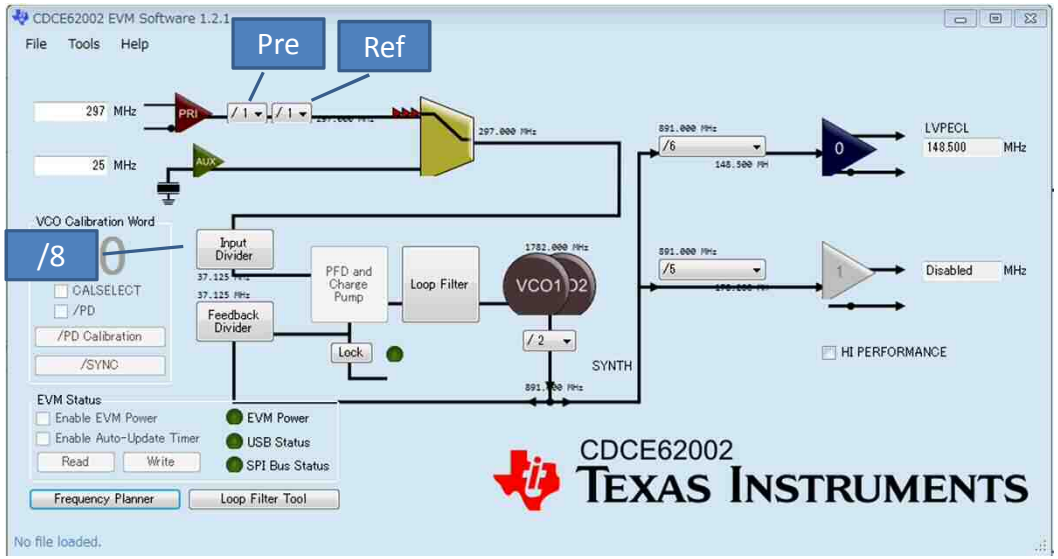
Maximum Divider Frequency



Frequency Planner generates 148.5MHz from 297MHz using the following parameters.
–Pre divider: /1
–Ref divider: /1
–Input divider: /8

However the PLL can not be locked with these parameters.
I changed some parameters as below then it can be locked.
–Pre divider: /1
–Ref divider: /2
–Input divider: /4

I think it is associated with the max spec of the divider.

7.4 Timing Requirements

over recommended ranges of supply voltage, load and operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
REF_IN REQUIREMENTS					
$f_{REF\ –\ Diff\ IN-DIV}$	Maximum clock frequency applied to reference divider when (Register 0 Bit 9 = 1)			500	MHz
$f_{REF\ –\ Diff\ REF\ DIV}$	Maximum clock frequency applied to reference divider when (Register 0 Bit 9 = 0)			250	MHz
$f_{REF–\ Single}$	For single-ended Inputs (LVCMOS) on REF_IN			250	MHz
Duty Cycle	Duty cycle of REF_IN	40%		60%	
INTERNAL TIMING REQUIREMENTS					
f_{SMUX}	Maximum clock frequency applied to smart MUX input			250	MHz
f_{INDIV}	Maximum clock frequency applied to input divider			200	MHz
AUXILARY_IN REQUIREMENTS					
$f_{REF\ –\ Crystal}$	AT-Cut crystal input	2		42	MHz
	Drive level	0.1			mW

Diff IN-DIV (Reg0 Bit9=1) Max.500MHz
Diff IN-DIV (Reg0 Bit9=0) Max.???MHz
Diff REF-DIV(Reg0 Bit9=1) Max.???MHz
Diff REF-DIV(Reg0 Bit9=0) Max.250MHz

What is different between fREF-Diff IN-DIV and fINDIV?
I would like to make sure the max spec of the dividers.