Synchronizing multiple LMK0482x devices, or providing more JESD204B outputs than a single LMK0482x device allows

2019-01-23, pre-release version, still under edit
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1 Introduction

The LMK0482x family of devices can produce clocks for up to 7 JESD204B targets such as ADCs, DACs, and FPGAs. In some applications more clocks than what a single LMK0482x can provide may be required or the system may be partitioned such that separate LMK0482x devices are required. In either case, it may be required to synchronize clocks between the multiple LMK0482x devices. In particular for JESD204B systems, the SYSREF clock needs to be deterministic between clocking devices.

This application note first discusses the theory related to synchronization of clocks in the presence of dividers and PLLs, and then examines some of the ways the LMK0482x devices can be configured to synchronize with one another and provides insight on the method to adopt for your application.

The LMK0482x device can be configured as a dual loop jitter cleaner, a single loop clock generator, or a distribution device. A system may consist of multiple LMK0482x in different modes of operation. Synchronization techniques will be discussed for each use case of the LMK0482x.

1.1 Important Terms

Clock Distribution Path – The internal path in LMK0482x which drives the SYSREF and Clock Output Dividers. Internal VCO0, Internal VCO1, or Fin/CLKin1 pins (for external VCO/Distribution) can drive the Clock Distribution path.

SYNC/SYSREF Path – The internal path in LMK0482x which will reset the internal dividers and/or drive the SYSREF outputs, as desired by programming. Possible sources to SYNC/SYSREF path are many, including but not limited to CLKin0, SYNC pin, SYSREF Divider, Pulser, Re-clocking D-Flip Flop.

SYNC – A synchronization signal to hold a divider in reset. On LMK0482x, when asserted a SYNC signal can hold a divider in reset if one shot sync is not enabled and sync disable is not be engaged.

SYNC one shot – If one shot sync is enabled (SYNC_1SHOT_EN = 1), then the a divider will be reset deterministically to the rising edge of SYNC signal. One shot mode also prevents outputs from being held in SYNC (reset). Sync disable must not be engaged for the SYNC signal to take effect.

SYSREF – In JESD204B subclass 1 systems, SYSREF is the signal whose rising edge marks the device clock rising edge which will reset the local multi-frame clock (LMFC), and possibly other dividers in a JESD204B device, provided that the SYSREF is still high when the device clock rising edge occurs.

0-Delay – A mode of operation of a PLL where an output divider is included in the PLL feedback path to lock phase of divider output with reference.

GCD – The greatest common divisor of two or more numbers is defined as the largest number which can divide into all the other numbers without a remainder.

2 Contents

3 Theory

When a clock is divided to a lower frequency, the division can introduce phase uncertainty as illustrated in Figure 1. A divider of value N will have N possible phases. The reason for this phase uncertainty is dividers implemented as counters may start dividing the reference frequency at different times or have the initial state of their counters power up at different values.

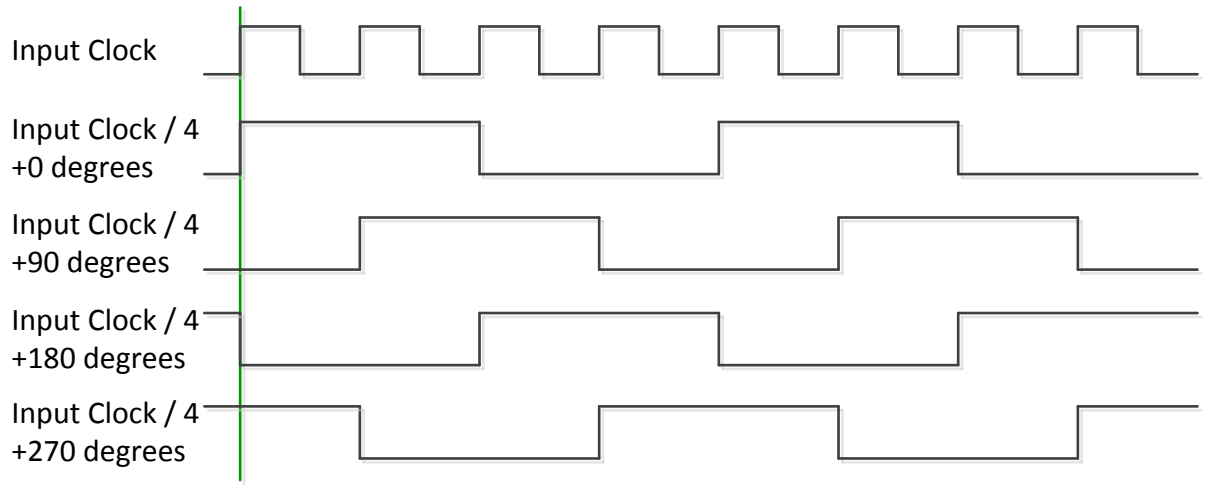

Figure 1 - Introduction of phase uncertainty by a divider

3.1 Synchronization by of Dividers by Reset

A simple solution is to reset the dividers to a common starting value. To do this a synchronization signal must reset the dividers while meeting the setup and hold time of the input clock. As the input clock frequency increases, the valid window for the reset signal becomes small and adjusting the timing of reset signal relative to input clock can be difficult.

Synchronization by divider reset is the clocking synchronization scheme used in JESD204B. The SYSREF pulse resets dividers internal to the data converters and logic devices to align the LMFC (local multi-frame clock) deterministically between all devices.

3.2 Synchronization in PLLs

A PLL (phase locked loop) as illustrated in Figure 2 will also have phase alignment between the reference input and the VCO frequency at the rate of the phase detector frequency. However the forward division of the reference frequency by the reference divider (R) can introduce phase uncertainty between the reference input and VCO output in some cases.

Phase certainty from reference input to reference output can be achieved with the reference divider equal to one. However it is not strictly required for R = 1 to have deterministic phase between reference input and VCO output. The output frequency of the VCO = Reference Frequency * (N / R). Anytime the fraction N / R reduces such that R = 1, then deterministic phase from input to VCO will occur. It is also worth noting that the maximum phase detector frequency for an integer PLL is the GCD of the reference frequency and the VCO frequency. This property can be used to differentiate systems which can have all reference clock edges phase aligned with VCO clock and those for which only every Nth reference clock edge will align with a VCO clock edge.

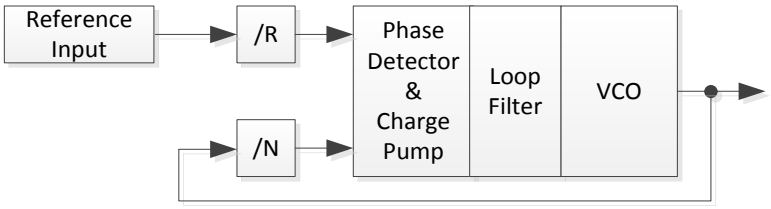

Figure 2 - Basic PLL

Example 1, all reference clocks have phase alignment to VCO

Conditions:

- Reference frequency = 40 MHz
- VCO frequency = 160 MHz
- Every reference clock edge has a corresponding VCO clock edge

To lock phase with a 10 MHz phase detector frequency, R = 4 and N = 16. Since N / R = 16 / 4 reduces to 4 / 1, the reference will always have a VCO clock in phase with it. While instantaneously it is possible to have one of four different phases (R = 4), the PLL will phase lock the output of the feedback divider to the output of the reference divider.

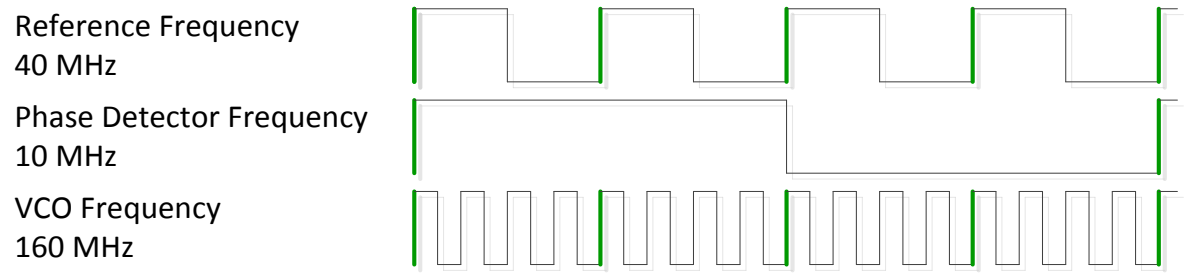

Figure 3

Example 2, some reference clocks to not have phase alignment at all VCO edges

Conditions:

- Reference frequency = 60 MHz
- VCO frequency = 160 MHz
- Every Nth reference clock edge has a corresponding VCO clock edge

To lock phase with a 10 MHz phase detector frequency, R = 6 and N = 16. Since N / R = 16 / 6 reduces to 8 / 3, the reference will have one of three different phase relationships to the VCO clock.

Recall however, because of the nature of the phase locked loop, the reference and VCO clock will always be in phase once every period of the phase detector. Depending on the application, this phase alignment may be sufficient.

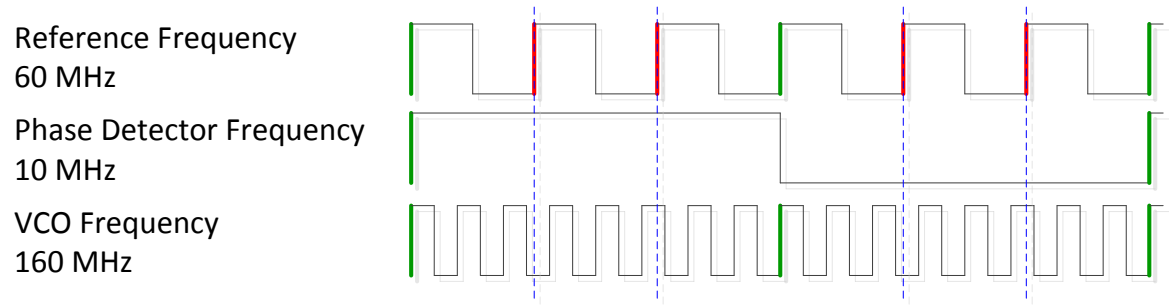

Figure 4

To summarize, the requirement for the reference frequency to have a deterministic relationship to VCO clock, is **GCD(reference frequency, VCO frequency) == reference frequency / some positive integer**. The number of possible phase relationships between the reference frequency and VCO will be = **reference frequency / GCD(reference frequency, VCO frequency)**.

3.3 Synchronization in Clocking ICs by using 0-Delay mode

Clocking ICs typically integrate a PLL and a clock distribution block with division. Figure 5 illustrates a PLL with two outputs, each output with its own divider.

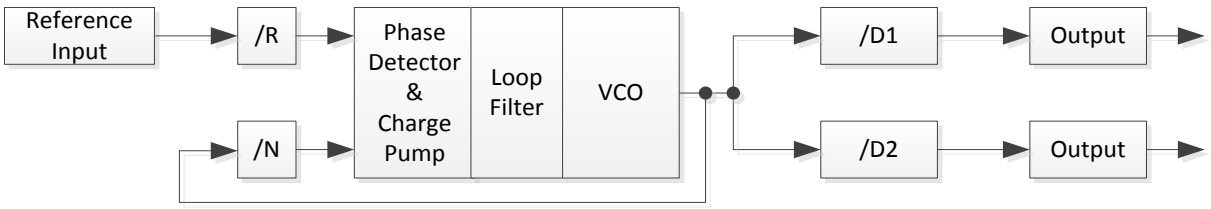

Figure 5 - Basic PLL with clock distribution. VCO frequency = Reference Frequency * N / R. Output Frequency = VCO Frequency / Dn.

Most clock generators include the ability to synchronize the phase of the dividers D1 and D2 to have no phase offset using the synchronization by divider reset technique described previously. Many clocking devices have digital and/or analog delays which allow the user to specify a fixed delay between the clock distribution dividers. For many clock generation applications, the alignment of the phases of each individual output is sufficient by this internal divider synchronization.

However if phase determinism between reference input and clock output is required, one method to achieve this is to include the clock output divider in the feedback path from VCO to phase detector. This eliminates the many possible phases of the divider driven by the VCO relative to the reference by "disciplining" the clock output phase to the reference phase through the phase detector. Otherwise the output clock will have "n" possible phase relationships between reference input and output frequency with phases spaced at the period of the VCO.

Figure 6 illustrates the output of divider 2 (D2) in the feedback path with PLL N divider to the phase detector. Only one output needs to be fed back to the phase detector because all the other outputs can share the phase determinism by synchronization with the D2 divider.

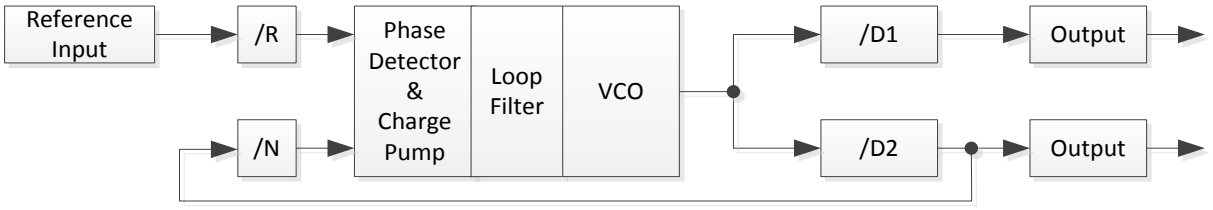

Figure 6 - Basic PLL with clock distribution. PLL feedback incorporates a clock divider in feedback path. Here VCO Frequency = Reference Frequency * (N * D2) / R.

Note, this feedback can assure deterministic phase between reference and output, but it does not alone assure a true "0-delay" from input waveform to output waveform. To achieve true delay of zero seconds it may be required to use delays on the PLL R and N paths or on the feedback output or non-feedback outputs. The requirements upon "0-delay" behavior vary by application.

3.3.1 0-Delay Rules for Determinism

3.3.1.1 1st Rule, the GCD between input and output frequency must equal input frequency

For a clock output to have deterministic phase to the clock input, it must meet the following equation:

GCD(clock input frequency, clock output frequency) == clock input frequency

If the clock output frequency is less than the clock input frequency, then a lower clock input frequency must be presented to ensure deterministic phase. Otherwise there is an implicit, unsynchronized divide between them.

If the clock output frequency is greater than the clock input frequency, but the result of the GCD of clock input and output frequency is still less than clock input frequency, the frequencies are poorly related and there is an implicit, unsynchronized divide between them.

3.3.1.2 2nd Rule, lowest output frequency requiring determinism used for 0-Delay feedback

For a clocking device with multiple clock frequencies all needing deterministic phase with the input, the frequency which must be feedback is the lowest.

3.3.2 0-Delay Examples

Next are three examples of attempting to use 0-delay to achieve deterministic phase between input and output of a clocking device. Only the first example achieves 0-delay. The first two reuse the examples from the previous PLL section. The third case highlights complications which can occur when more than one output frequency must have phase determinism with the reference clock.

3.3.2.1 Case 1, Simple case of using 0-delay to align 40 MHz reference with 40 MHz clock output

Conditions:

- Reference frequency = 40 MHz
- VCO frequency = 160 MHz
- Output frequency = 40 MHz
- 40 MHz output should have deterministic phase to 40 MHz reference

To lock phase with a 10 MHz phase detector frequency, R = 4 and Total PLL N = 16. To get an output clock frequency of 40 MHz, a divider of 4 is used from 160 MHz to achieve 40 MHz clock output. Since this 40 MHz clock frequency is fed to the PLL N divider, the PLL N divider needs to be programmed = 4. So the total N divide = 16 (as in prior example), but it is distributed between the clock divider and the PLL N divider.

Figure 7 illustrates the waveforms produced in this example. The reference frequency, phase detector frequency, and VCO frequency are as before. However the Clock Output Frequency has been added and shown to have matching phase with the reference frequency. It's worth noting that the PLL N / 4 does produce 4 possible phase of output from the PLL N divider, but no matter which edge occurs, the PLL will phase lock the other possibilities 2, 3, and 4 to have the same phase as 1, which matches the phase shown for the 10 MHz Phase Detector Frequency above. Finally, if 0-delay was not use, the bottom of Figure 7 illustrates the other 3 possible phase relationships the output clock could have to the input

clock making a total of 4 cases. Any number of possible phase relationships greater than one constitutes as non-deterministic.

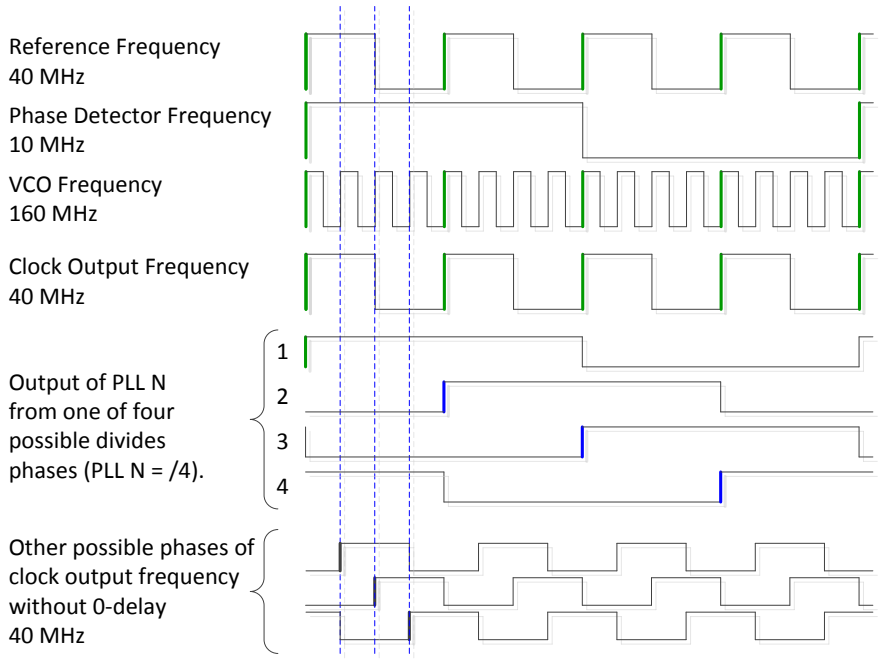

Figure 7 - Output Waveforms for 0-Delay with input frequency equal to output frequency

3.3.2.2 Case 2, 0-delay to align 60 MHz reference with 40 MHz clock output.

Note it would have been interesting to illustrate a 60 MHz clock output with deterministic phase (or not) to a 60 MHz clock input. However this is not possible to divide from 160 MHz to 60 MHz using an integer divider, 160 MHz / 60 MHz = 2 + 2/3. It is worth noting that this circumstance has arisen because of the forward division by the PLL R divider not being reducible to 1. If the VCO frequency were changed to 120 MHz or 180 MHz, both of which could produce 60 MHz using an integer clock output divide value, then the PLL N value would have allowed the PLL R value to be reduced to 1.

Note: It is always possible to phase lock any two rational frequencies because there is a frequency which can divide evenly into both the reference frequency and the VCO frequency. This frequency is the greatest common divisor (GCD) of the reference frequency and VCO frequency.

This case occurs when going between different “clock domains.” This situation may occur in an application when it is desired to lock a 122.88 MHz VCXO to a 10 MHz reference. For an integer PLL to lock phase between these domains, an 80 kHz phase detector frequency must be used! GCD(122.88 MHz, 10 MHz) = 80 kHz.

Back to the case at hand, based on PLL synchronization case 2, alignment of a 60 MHz reference input to a 40 MHz clock output.

Conditions:

- Reference frequency = 60 MHz
- VCO frequency = 160 MHz

- Output frequency = 40 MHz
- Every Nth reference clock edge has a corresponding clock output edge

To lock phase with a 10 MHz phase detector frequency, R = 6 and Total PLL N = 16. To get an output clock frequency of 40 MHz, a divider of 4 is used from 160 MHz to achieve 40 MHz clock output. Since this 40 MHz clock frequency is fed to the PLL N divider, the PLL N divider needs to be programmed = 4. So the total N divide = 16 (as in prior example), but it is distributed between the clock divider and the PLL N divider.

Figure 8 illustrates the waveforms produced in this example. The reference frequency, phase detector frequency, and VCO frequency are as before. However the Clock Output Frequency has been added and shown to have matching phase with the reference frequency. It's worth noting that the PLL N / 4 does produce 4 possible phase of output from the PLL N divider, but no matter which edge occurs, the PLL will phase lock the other possibilities to have the same phase. Refer to Figure 7 which illustrated this in more detail. Finally, if 0-delay was not use, the bottom of Figure 8 illustrates the other 3 possible phase relationships the output clock could have to the input clock making a total of 4 cases. Any number of possible phase relationships greater than one constitutes as non-deterministic.

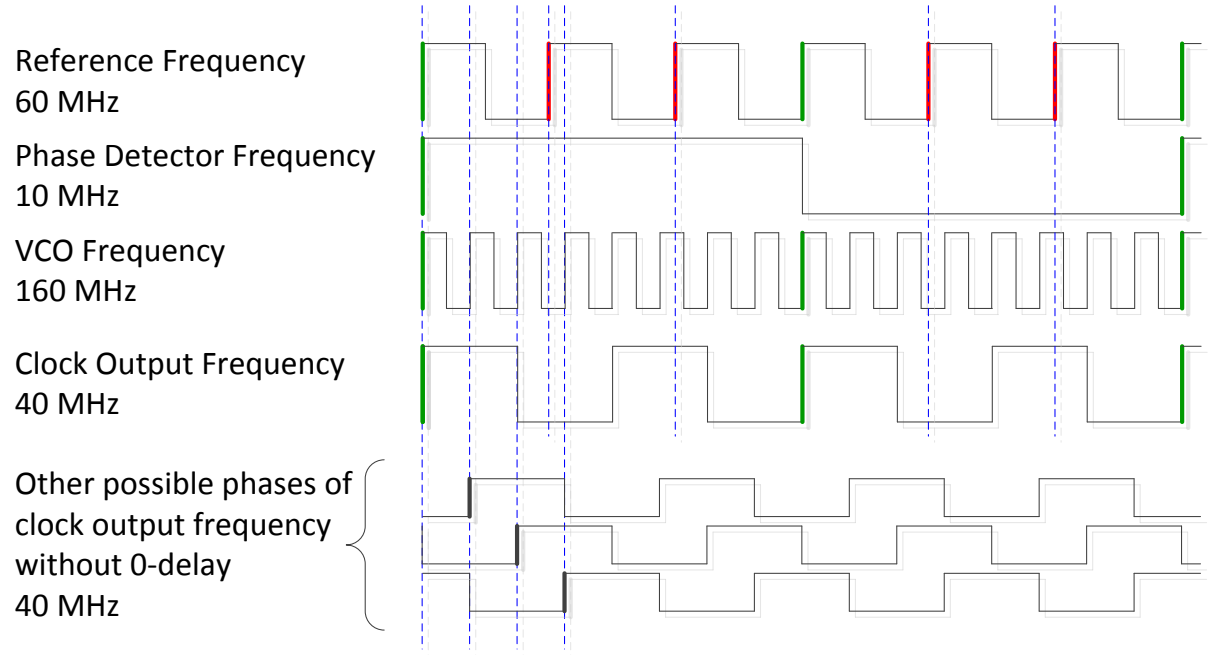

Figure 8 - Output Waveforms for 0-Delay with input frequency not equal to output frequency. Across "clock domains."

Note in the middle of Figure 8 the reference clock, the VCO clock, and the output clock also share common edges, this is because the GCD(60, 160, 40) = 20 MHz, so the clock edges will align at a rate of 20 MHz. A phase detector of as high as 20 MHz could have been used to lock the 60 MHz reference to the 160 MHz VCO. Meaning the reference would need to be lowered to 20 MHz to achieve 0-delay from reference to output.

Now in similar fashion, as the PLL only case, every Nth reference clock edge aligns with the output clock edge.

3.3.2.3 Case 3, 0-delay to align a reference frequency to two clock output frequencies

Conditions

- 10 MHz reference frequency
- 100 MHz and 125 MHz output frequencies
- 500 MHz VCO
- The 100 MHz and 125 MHz clocks should have a deterministic phase relationship to the 10 MHz reference.

When multiple outputs must have deterministic phase with the input, first find the GCD of the output frequencies, in this case GCD(100 MHz, 125 MHz) = 25 MHz. This means that a 25 MHz clock synchronized by divider reset with the 100 MHz and 125 MHz clock and is required to be fed back to the PLL phase detector. Because the greatest common divisor of the reference frequency and the feedback frequency of 25 MHz is 5 MHz, the phase detector must be programmed to 5 MHz to allow integer dividers to program the PLL to lock.

To lock phase with a 5 MHz phase detector frequency using a 10 MHz reference and 500 MHz VCO, R = 2 and Total PLL N = 100. Since a 25 MHz clock is used to drive the PLL2 N divider which requires a clock output divide of 20, we can determine the PLL N should be programmed to 5. Now PLL N of 5 * Clock Divide of 20 = 100, which is the total N value required to lock the PLL. The clock divider for the 100 MHz clock output is /5 and the clock divider for 125 MHz clock output is /4.

Figure 9 illustrates the waveforms produced in this example. As in the prior examples, because of the PLL N divider of 5, there could be 5 different phases of the 5 MHz phase detector as divided from the 25 MHz reference before the PLL phase locks the divided output of PLL N. After lock the diagram looks as shown below. It can also be observed that while the phase of the 100 MHz and 125 MHz align at a rate of 25 MHz, it is only at the rate of 5 MHz that the reference clock edge aligns with both the 100 MHz and 125 MHz clock edges. In cases where an extra frequency is required for alignment, the LMK products require only the clock divider to operate while the output driver to be powered down to conserve current.

In many cases, the feedback clock will be the same frequency as the lowest output clock. For instance if 50 MHz and 100 MHz are generated, the GCD(50 MHz, 100 MHz) = 50 MHz and the 50 MHz clock would have been used as the feedback clock, but could have also been used as an output clock.

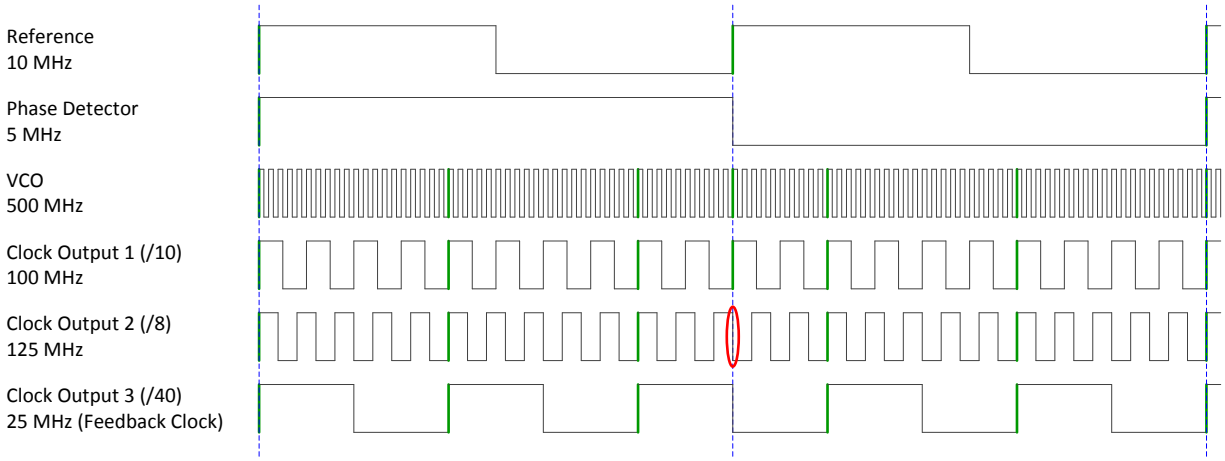

Figure 9 - Output Waveforms for 0-Delay with two different output frequencies

Note that the 100 MHz clock actually has 1:1 synchronization to the reference clock, but the 125 MHz clock has N:1 synchronization to the reference clock, with every other reference clock edge having a corresponding output clock edge.

3.4 Synchronization techniques as applied to multi-device synchronization

When designing multiple devices to be synchronized together, anytime one of the N:1 cases are employed, it is not assured to have synchronization through-out the system. Methods eliminate N:1 uncertainty due to N/R non-reduction are currently being addressed.

TABLE below summarizes the synchronization techniques discussed so far.

Synchronization Case		
Divider reset		
PLL Synchronization, 1:1		
PLL Synchronization, N:1		Divider reset needed to make the N:1 deterministic
0-Delay Synchronization, 1:1		
0-Delay Synchronization, N:1		Divider reset needed to make the N:1 deterministic

4 Practical considerations of synchronization using the LMK0482x devices

4.1 Don't "SYNC" yourself in the foot

When using the JESD204B functionality of the LMK0482x, it is important to realize that *the path to synchronize the dividers is shared with the SYSREF output path*. In fact a **SYSREF signal from the SYSREF divider can reset the SYSREF divider erroneously! If ever a strange waveform is viewed from the SYSREF, then SYSREF is probably re-syncing itself, set SYNC_DISSYSREF = 1.**

Or if 'gated' or otherwise strange looking device clocks, it is probable that the sync disable bits (SYNC_DISX,) bits are clear on the DCLKoutXs and the SYSREF/SYNC path is resetting the output clock dividers. This can easily happen in SYSREF continuous mode, but will occur anytime the SYNC/SYSREF path is asserted.

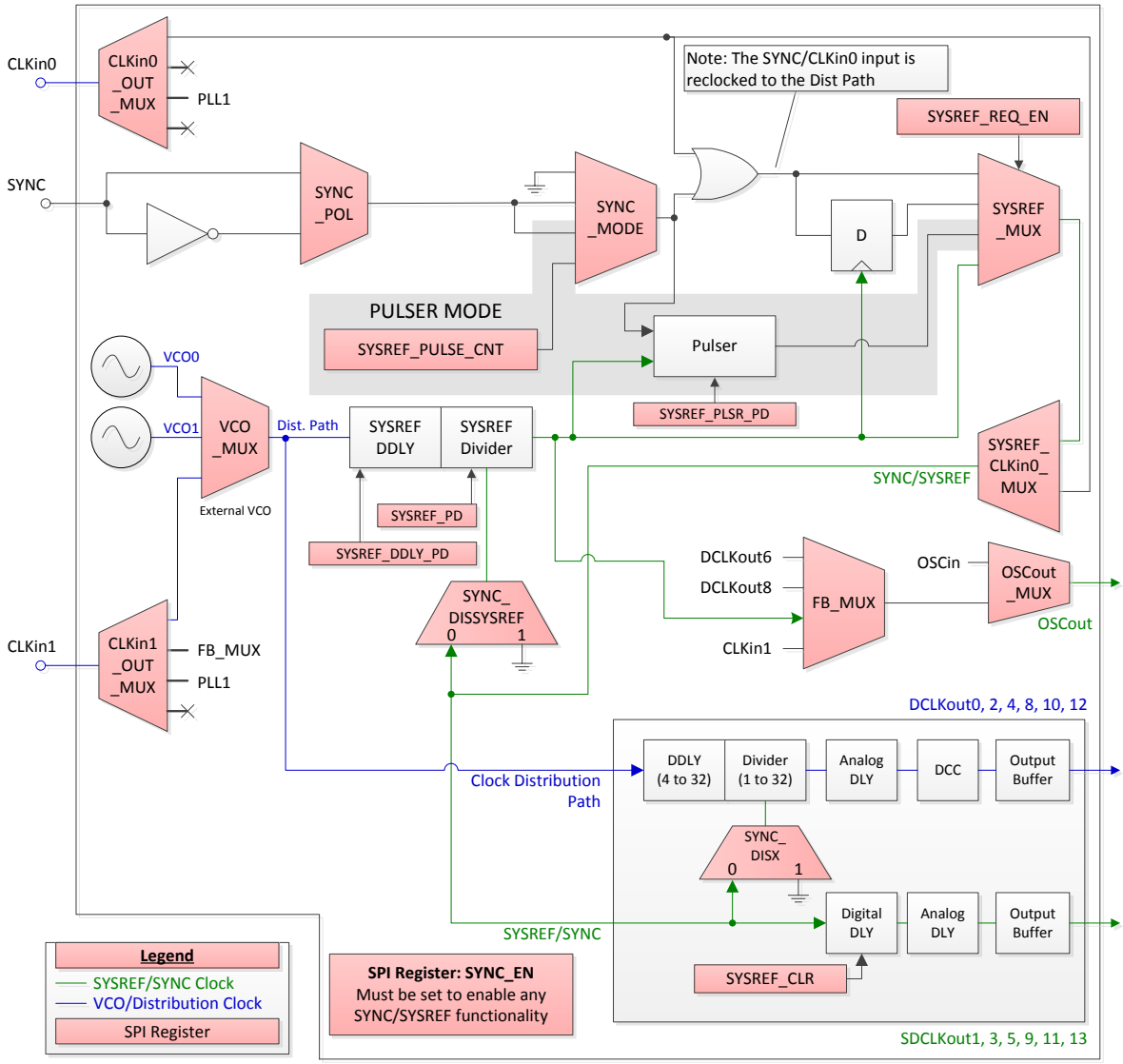

Figure 10 - Detailed View of SYNC/SYSREF

4.2 Synchronization of outputs of a single LMK0482x device

Understanding how the divider reset works on LMK0482x is a fundamental building block. Presented here is a basic technique for synchronizing the dividers of a single LMK0482x.

For dividers with SYNC_DISX/SYNC_DISSYSREF bits clear, the SYNC signal to a divider can be asserted from the SYNC pin via the SYNC_MODE and SYSREF_MUX to each divider. This is illustrated in Figure 11 below. It is possible to issue a software SYNC by SPI programming the SYNC_POL register, refer to Table 1. The SYNC pin may be left disconnected as it has a weak pull-down.

After divider synchronization is complete, for devices generating SYSREF it is then required to set SYNC_DISX and SYNC_DISSYSREF bits before configuring the desired SYSREF generation mode to prevent the SYSREF signal from erroneously resetting dividers.

Table 1 - SYNCing Dividers

SYNC Pin	SYNC_1SHOT_EN [insert link to glossary of terms in front]	Description
Low or NC	0	SYNC_POL = 1 holds dividers in reset.
High	0	SYNC_POL = 0 holds dividers in reset.
Low or NC	1	SYNC_POL 0 → 1 resets dividers
High	1	SYNC_POL 1 → 1 resets dividers

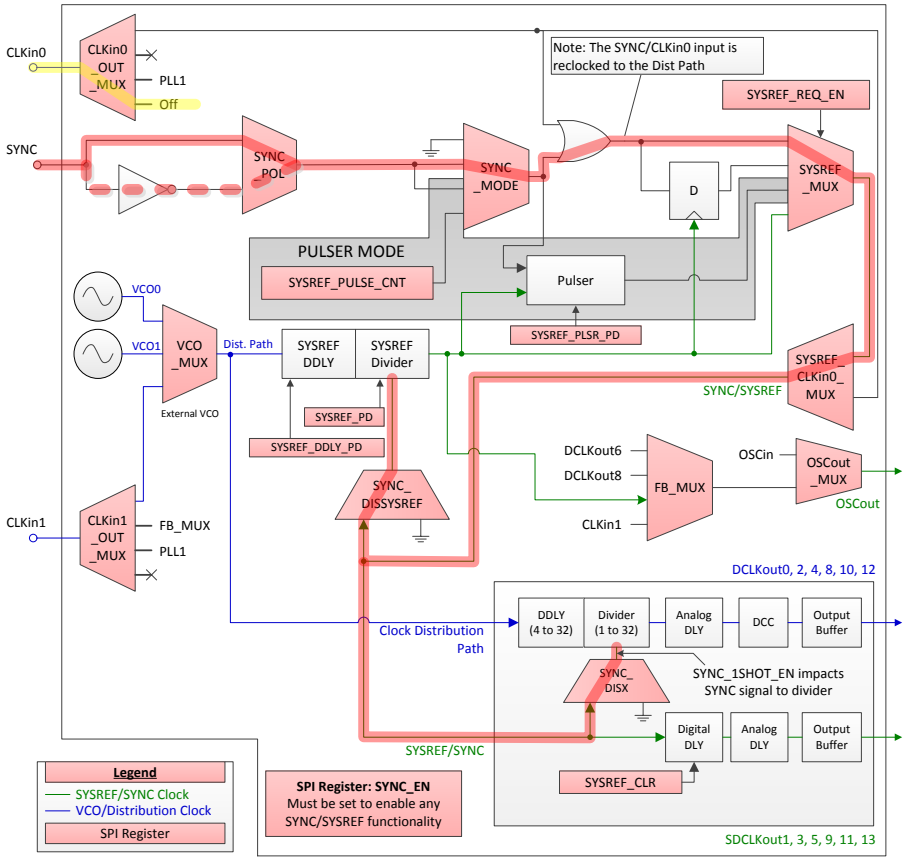

Figure 11 - Basic divider reset

When SYNC is released, all dividers which allowed the SYNC and have digital delay powered up will have a deterministic phase with respect to each other. The actual phase between the device clock and SYSREF clock depends upon the digital and analog delay programmed. Phase between a device clock and SYSREF can be determined from the value of the SYSREF Divider and the mode that the Clock Divider is operating in. Figure 12 shows an example of a how phase of device clock and SYSREF align. There is a separate factor labeled C below used to relate the digital delay values between device clock and SYSREF. Analog delay is added on top.

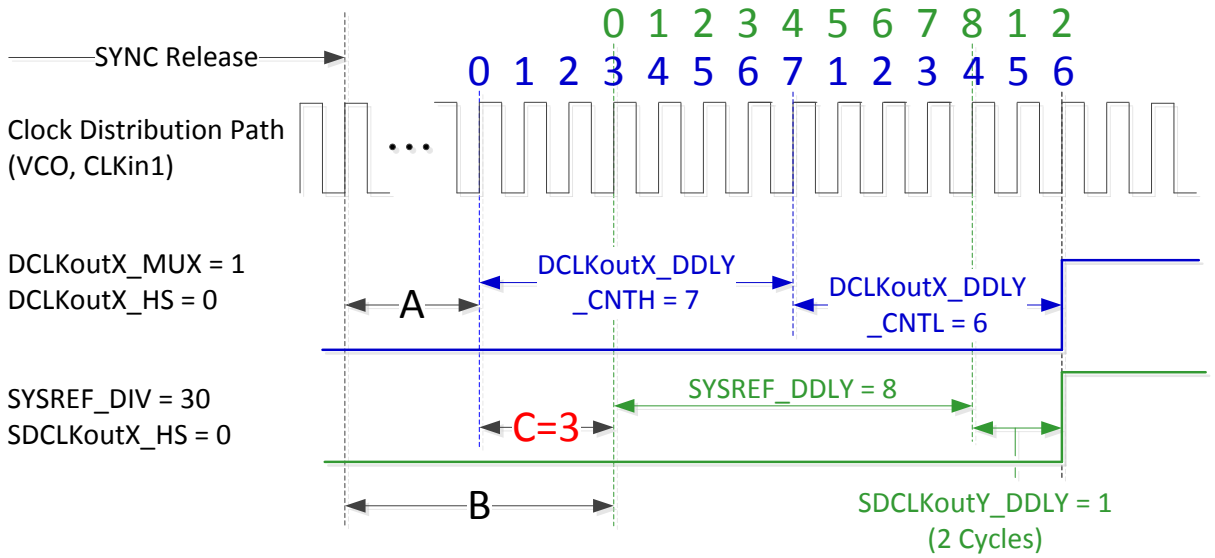

Figure 12 - Relative timing between device clock and SYSREF clock

The actual value of C is defined in part by Table 2 and Table 3, where C = SYSREF_DIV_ADJUST + DCLKout_MUX_ADJUST. So in the Figure 12 case with a SYSREF divider value of 30, where 30 modulus 4 = 2, therefore SYSREF_DIV_ADJUST = 3. And since the DCLKoutX_MUX is set to 1, the DCLKout_MUX_ADJUST = 0. Using these values C = 3. This means that the total device clock and SYSREF are to be aligned by digital delay, the total SYSREF DDLY (global + local) will be programmed to 3 cycles less than the device clock digital delay.

Table 2 - Device clock to SYSREF timing due to SYSREF divider value

SYSREF_DIV % 4	SYSREF_DIV_ADJUST
0	2
1	2
2	3
3	3

Table 3 - Device clock to SYSREF timing due to DCLKoutX_MUX

DCLKoutX_MUX	DCLKout_MUX_ADJUST
0 (Divide)	1
1 (Div + DC + HS)	0

Setting the half step bit will result in the programmed clock to advanced ½ period of the clock distribution path.

In addition to the registers/fields which determine C, when syncing, take into consideration the following fields in Table 4:

Table 4 - Fields of consideration during SYNC

Field	Description
SYNC_DISX/SYNC_DISSYSREF	0 allows SYNC to reset divider
CLKoutX_DDLY_PD/SYSREF_DDLY_PD	0 allows digital delay to provide deterministic phase relationships between dividers

DCLKoutX_DDLY_CNTH DCLKoutX_DDLY_CNTL	These registers summed together define how much VCO clock cycle delay occurs for device clock
SYSREF_DDLY	Defines how much VCO clock cycle delay occurs for SYSREF clock. This is also called global SYSREF delay.

DCLKoutX_HS, SDCLKoutY_HS, and SDCLKoutY_DDLY registers take effect immediately upon programming and do not require a SYNC.

Remember, SYNC and SYSREF share the same path internal to LMK0482x. This can be powerful to allow an external SYSREF to reset dividers. The shared SYNC and SYSREF paths also require management of the sync disable bits, SYNC_DISX and SYNC_DISSYSREF, to get the desired behavior.

4.3 Summary

With the basic understanding of how SYNC and SYSREF operate on an individual LMK0482x, the next sections begin to address multi-device sync.

4.4 Topologies of connecting Multiple LMK0482x Devices together

To demonstrate multi device synchronization, multiple boards can be connected in different topologies discussed next. To illustrate phase determinism between multiple LMK0482x devices, only two devices are required, a master and slave.

In the examples, the slave device is driven from DCLKout0, this allows the user to use DCLKout0_DDLY to change timing. However for best performance, the buffered output of OSCin, OSCout could be used as illustrated in Figure 15 under the daisy chain topology.

While the fundamentals of phase synchronization apply to all topologies, the specific method of connecting multiple LMK0482x devices, and the modes the device operate in have different trade-offs.

4.4.1 Tree

Typically in large systems a tree topology will be used to distribute clocks. The operating mode of the LMK0482x will determine how the noise in the system accumulates.

- In distribution mode, the noise floor will increase at each level of the tree. This is a mode is good for fanning out reference clocks as no PLL noise is added and fanning out high performance external clocks at high frequency.
- In singe PLL mode, the VCO will perform jitter cleaning above the PLL2 loop bandwidth, this typically means that noise floor remains constant, but that the in-band PLL noise will experience some increase at each level of the tree. It is possible to narrow the PLL2 loop bandwidth to achieve jitter cleaning above 10 kHz with good results. Figure 13 illustrates a tree of multiple single loop LMK0482x devices.
- In dual loop mode, the VCXO will perform jitter cleaning above the PLL1 loop filter bandwidth. Dual loop mode results in the best case phase noise throughout the system in terms of no additive jitter except below PLL1 loop bandwidth, which is without consequence as the PLL1 loop bandwidth is chosen to be narrow. The choice of VCXO performance and frequency impact final performance.

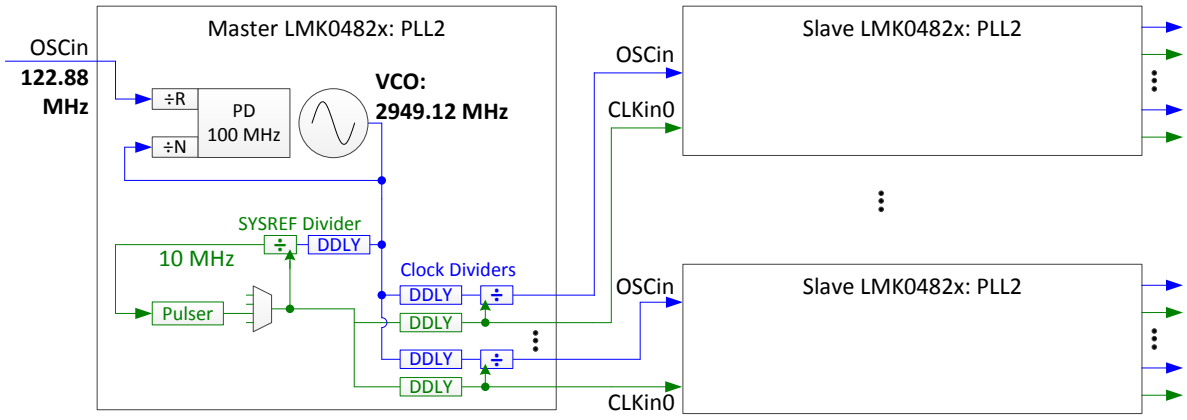

Figure 13 - Tree using multiple LMK0482x

A tree could also be implemented using a fan-out buffer to drive multiple LMK0482x devices. As illustrated in Figure 14, the SYSREF master can still be downstream of the reference fan-out.

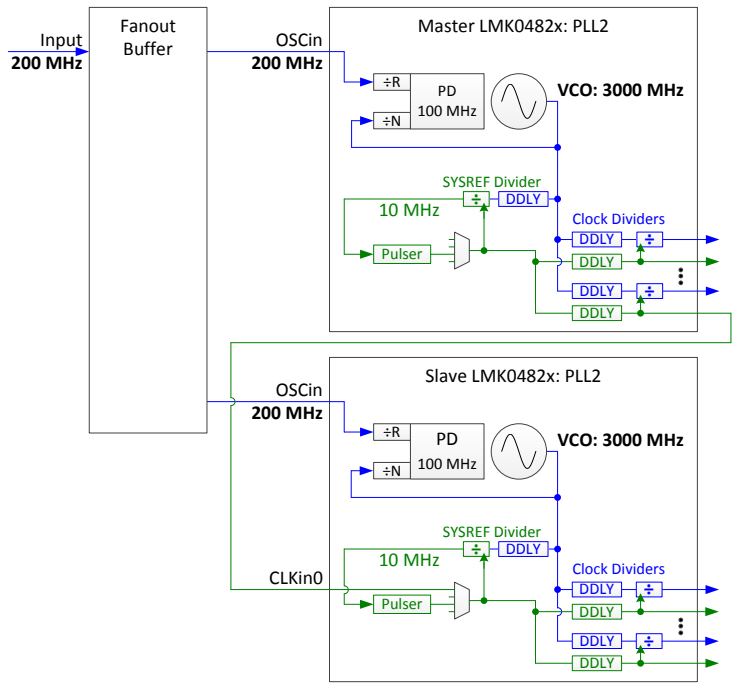

Figure 14 - Tree using multiple LMK0482x showing that the master SYSREF control can be downstream of fan-out

An advantage of the tree is that any propagation delay shifts over temperature will occur to all outputs at the same level in the tree equally with-in typical part to part variation. This helps keep the outputs phase matched.

4.4.2 Daisy Chain

This topology requires the least number of parts to get two or more LMK0482x working together.

A single or dual loop master can buffer the OSCin input to the OSCout output. No extra buffer is required to fan-out a low noise reference. The advantage of distributing the reference is no PLL noise has been added by the LMK0482x. Only the noise floor will increase, but because the slave device is typically operating in single or dual loop mode, this noise floor increase is of little to no impact in the system.

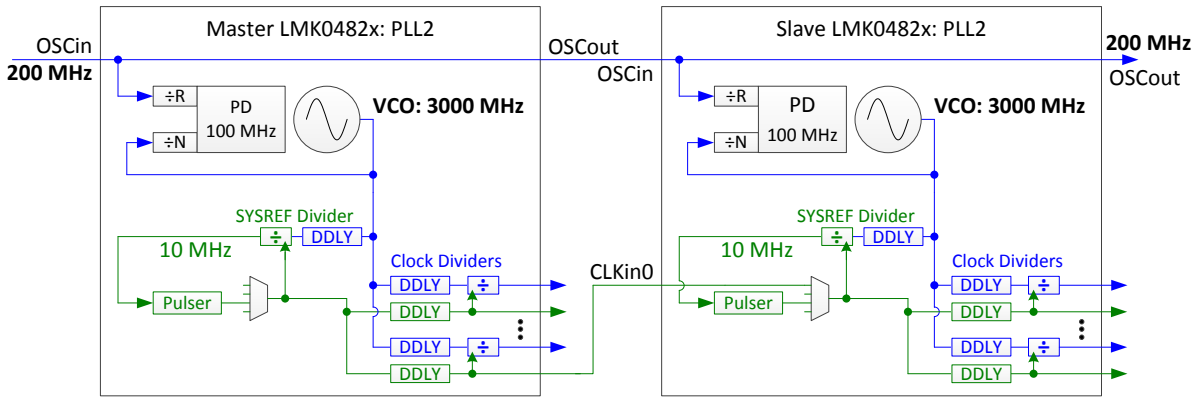

Figure 15 - A very simple, low jitter, multi-LMK0482x solution

It is also possible to use a DCLKout to drive OSCin of the slave PLL, however DCLKout will be driven by PLL2 and will have some addition of noise caused by PLL2.

The phase error between master and slave can be minimized by using the digital delay. The resolution of a half step delay on the device clock outputs allows phase adjust to within ~¼ VCO clock cycle. Because the reference to master and slave are different, subsequent voltage temperature variation could cause additional drift to the slave. If this is not tolerable, a tree topology can be used.

4.4.3 Master Dual Loop with Multiple Single Loop Slaves

If jitter cleaning is required and multiple LMK0482x devices are needed to provide all clocks, it is possible to use PLL1 of the master LMK0482x to perform jitter cleaning using a VCXO, but instead of directly connecting the VCXO into the OSCin of that master device. Fan-out the VCXO to the master device OSCin + multiple other LMK0482x devices OSCin input operating in single loop mode.

The advantage of this architecture is that it can reduce system cost by requiring only 1 VCXO + fan-out buffer instead of one VCXO for each LMK0482x.

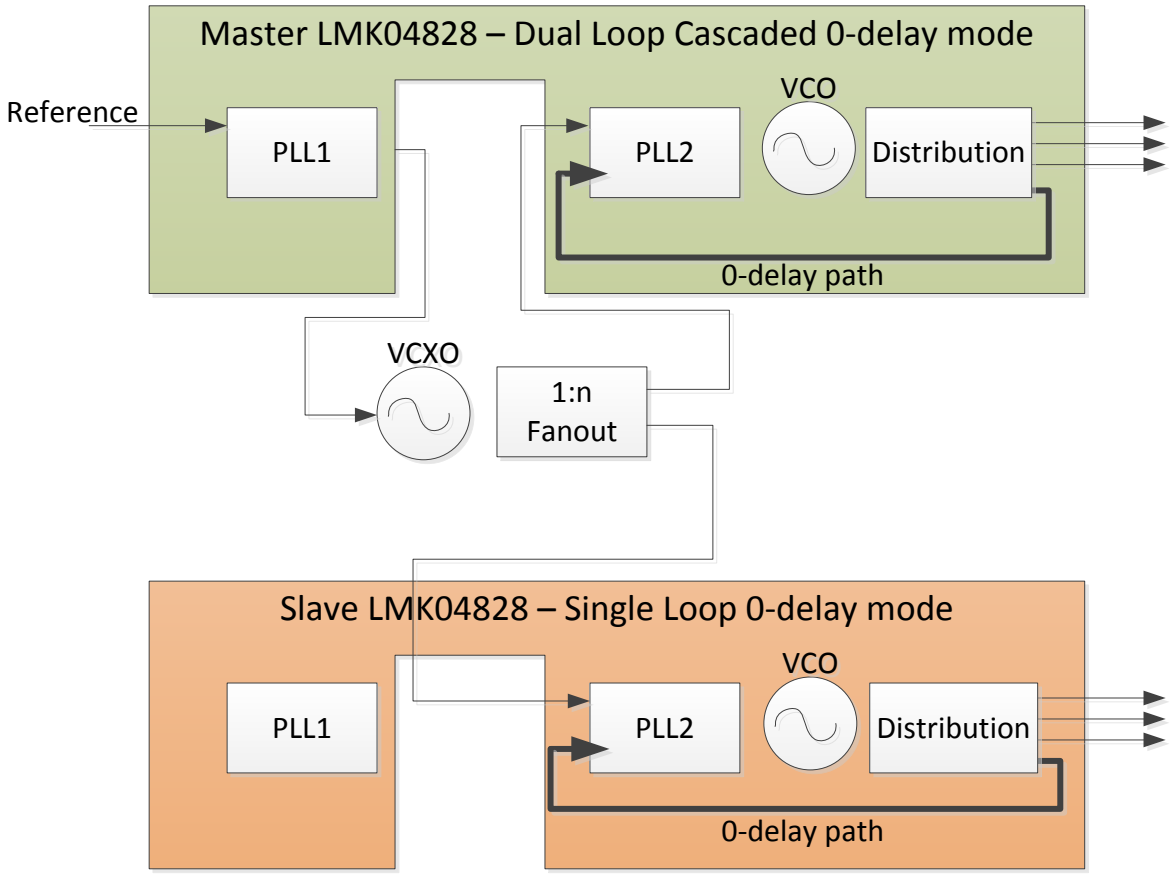

Figure 16 - Common OSCin reference topology, fan-out buffer could be replaced with the master LMK0482x clocking many LMK0482x slaves in large systems.

4.5 Multiple LMK0482x Device Output Synchronization

A primary focus for these synchronization examples will be for the JESD204B clocking case where the low frequency SYSREF becomes the lowest frequency required for determinism between all devices.

The LMK0482x can be configured to route SYNC/SYSREF for SYSREF pulser mode, re-clocked SYNC/SYSREF, continuous SYSREF, direct analog bypass of SYSREF, pin operated SYNC, etc. Refer to LMK0482x datasheet Table 1, "Some Possible SYNC Configurations" to see more details.

For many of the JESD204B cases, there is a two-step process of first SYNCing the devices, then providing SYSREF to downstream devices.

The following sections will help to outline how the LMK0482x can be programmed to achieve deterministic phase between devices depending on the functional mode of the slave devices. Table 5 outlines the slave device modes and use cases for the LMK0482x. The examples build upon themselves. Starting with distribution mode, and then introducing the PLLs.

Table 5 - LMK0482x Configuration Cases for Synchronization

Case	Slave Device Mode	Synchronization Technique	SYSREF
1a	Distribution	Direct divider reset from master	Local
1b	Distribution	Direct divider reset from master	Master by re-clock
1c	Distribution	Direct divider reset from master	Master direct analog
2a	Single Loop 0-Delay	0-Delay with SYSREF as Reference Frequency	Local
2b	Dual Loop Nested 0-Delay	0-Delay with SYSREF as Reference Frequency	Local
3a	Single Loop	Direct divider reset from master	Local
3b	Dual Loop	Direct divider reset from master	Local
4a	Single Loop, 0-Delay	re-clocked SYSREF	Master by re-clock
4b	Single Loop, 0-Delay	re-clocked SYSREF, Slave Dividers reset by master's re-clocked SYSREF	Master by re-clock
5a	Dual Loop, cascaded 0-Delay	re-clocked SYSREF	Master by re-clock
5b	Dual Loop, cascaded 0-Delay	re-clocked SYSREF, Slave Dividers reset by master's re-clocked SYSREF	Master by re-clock

4.5.1 Case 1a/b/c: Synchronization of multiple LMK0482x in Distribution mode

4.5.1.1 Overview

The LMK0482x configured to operate in distribution mode uses the external VCO path (CLKin1) for PLL2 to provide a clock to the dividers and outputs. Follow the yellow path in Figure 17 and Figure 19 to see how the distribution clock is delivered to the output clocks (e.g. DCLKout0) and how the distribution clock optionally re-clocks an incoming SYNC/SYSREF pulse on CLKin0.

By providing a SYNC pulse to the CLKin0 pin which meets a setup and hold time to CLKin1, it is possible to reset dividers of the LMK0482x deterministically.

After synchronization of device clock and SYSREF dividers the device may generate SYSREF locally (case 1a), re-clock the CLKin0 or SYNC input (case 1b), or directly analog bypass the CLKin0 to the outputs (case 1c).

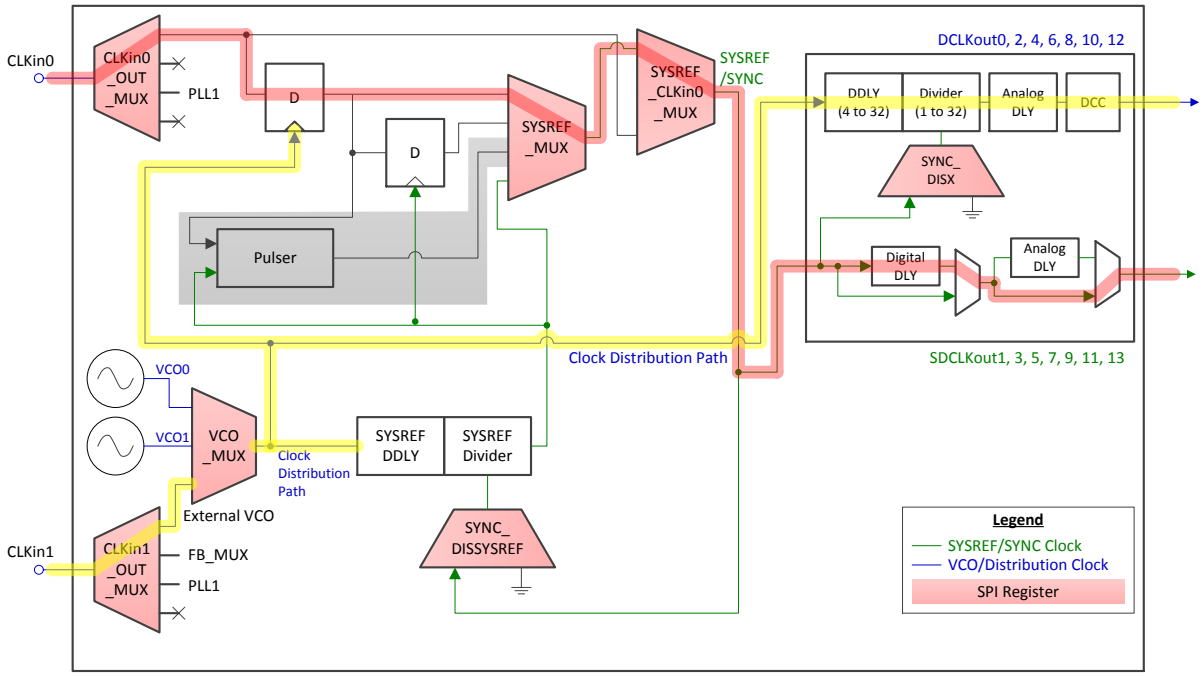

Figure 17 - CLKin0 and CLKin1 clocking paths highlighted for clock distribution mode

4.5.1.2 Procedure to Synchronize

4.5.1.2.1 Prepare to Synchronize LMK0482x dividers (was Basics) (??)

The slave LMK0482x is programmed as illustrated in Figure 17 to allow CLKin0 to reset all dividers. Follow recommended programming sequence from datasheet.

It is possible to synchronize the SYSREF and/or clock output dividers of the slave LMK0482x device in clock distribution mode using the CMOS SYNC pin. However, it is recommended to use the high speed CLKin0 path as illustrated in red highlight in Figure 17 for the SYNC/SYSREF clock. This path minimizes setup and hold times as compared to using the SYNC pin.

To allow the incoming SYSREF/SYNC signal to reset the dividers, the SYNC_DISX/SYNC_DISSYSREF bits must be clear for desired dividers. To reset on the rising edge, set SYNC_1SHOT_EN = 1. Only a single pulse is required reset the DCLKoutX and/or SYSREF dividers.

If the SDCLKoutY is powered up and selecting SYSREF with SYSREF_CLR = 0, then the same SYNC/SYSREF pulses which reset the dividers of the LMK0482x will also propagate to outside the chip. Powering down the output individually or with SYSREF_GBL_PD and appropriate SDCLKoutY_DIS_MODE, or setting SYSREF_CLR = 1 will prevent this from occurring.

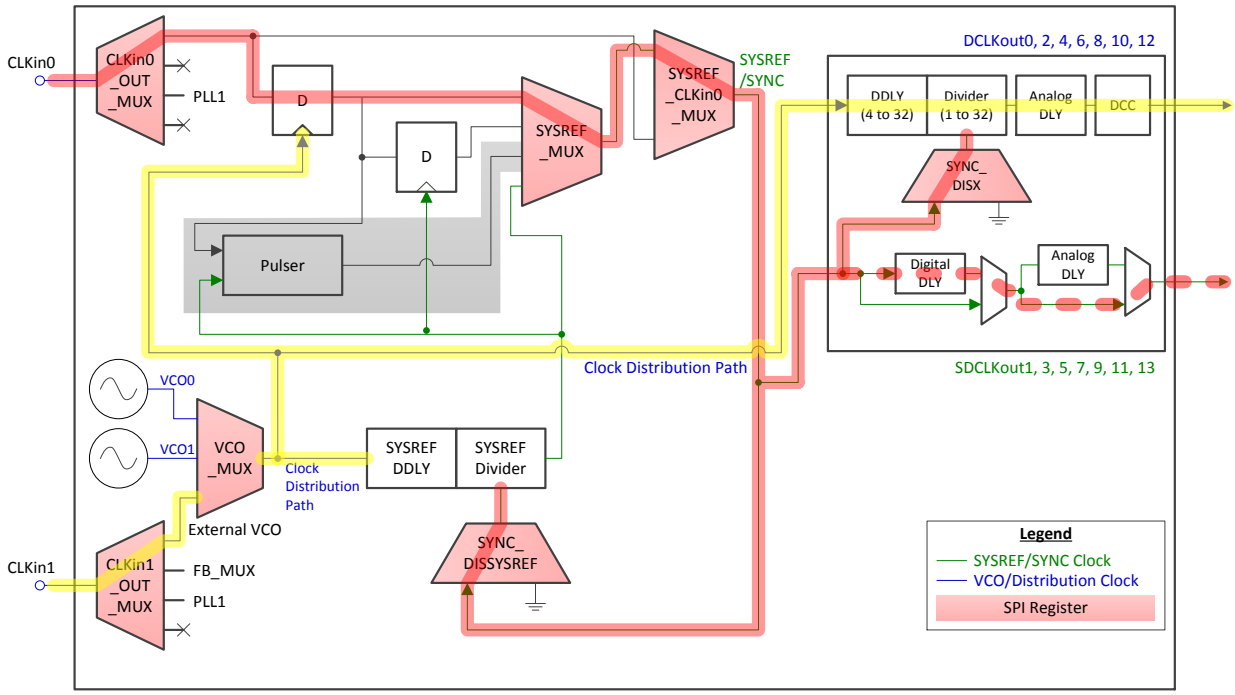

Figure 18 - Resetting dividers in distribution mode

To synchronize dividers, the key registers are:

Table 6 - Fundamental registers to setup slave in distribution mode

Address	Field	Value	Definition
Synchronization and clock routing path specific registers			
0x147[1:0]	CLKin0_OUT_MUX	0	Route CLKin0 to SYSREF_MUX
R313[0:1]	SYSREF_MUX	0	Route CLKin0 to SYSREF_CLKin0_MUX
R313[2]	SYSREF_CLKin0_MUX	0	Route SYSREF_MUX to SYSREF/SYNC Path
R324[0,1,2, 3,4,5,6,7]	SYNC_DISX, SYNC_DISSYSREF	0	Allow SYSREF/SYNC path to reset dividers as desired
R320[1]	SYSREF_DDLY_PD	0	Enable SYSREF DDLY
R316[0:4] & R317[0:7]	SYSREF_DDLY	?	As desired for global SYSREF DDLY
R262[7], … (Multiple)	DCLKoutX_DDLY_PD	0	Enable DCLKoutX_DDLY_PD
R257[0:3],[4:7], … (Multiple)	DCLKoutX_DDLY_CNTL DCLKoutX_DDLY_CNTH	? ?	As desired for device clock DDLY

	SYNC_MODE	0	Disables possibility of CMOS SYNC pin6 from causing a SYNC event. If desired, set to 1 to enable this path.
	SYSREF_PD	0	SYSREF Divider and circuitry powered up.

4.5.1.2.2 Synchronize DCLKoutX and SYSREF Dividers

Once the slave device is programmed to accept SYNC/SYSREF to reset its dividers, the SYNC event occurs. Now reconfigure the slave device as desired.

It is recommended for the external SYNC to arrive on DC coupled CLKin0. However the SYNC pin may also be used lower input frequencies.

4.5.1.2.3 Output of SYSREF

After the dividers are reset using the above configuration, the device may be reconfigured to generate SYSREF signals for downstream devices as illustrated in Figure 19. Here the SYNC_DISX/SYNC_DISSYSREF bits are re-programmed to prevent the SYSREF/SYNC signal from resetting the dividers, and the SYSREF_MUX is now selecting the pulser as the source for SYSREF signals. Note that other options would also be valid such as continuous mode (SYSREF_MUX = 3), re-clocked SYNC from CLKin0/SYNC pin (SYSREF_MUX = 1), or direct analog bypass of CLKin0 to SDCLKoutY (SYSREF_CLKin0_MUX = 1).

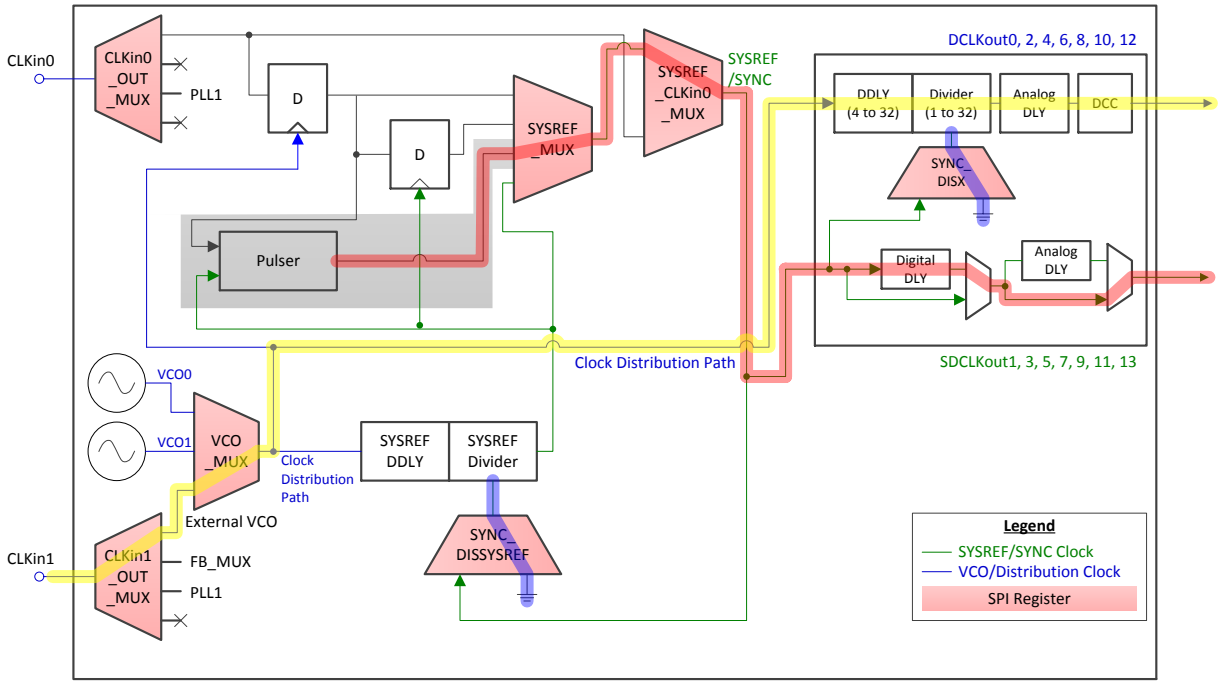

Figure 19 - Distribution with local SYSREF generation (simplified from Figure 10)

For this step, key registers are:

Address	Field	Value	Definition
	SYNC_DISX/ SYNC_DISSYSREF	1	Disable all SYNC

	SYNC_MODE	2 or 3	Select pin or SPI pulser trigger
	SYSREF_MUX	3	Select pulser
	SYSREF_CLR	0	SYSREF CLR must be 0 for operation

4.5.1.3 Example

This example will use two LMK04828 boards as illustrated in Figure 20. The master will be configured in a PLL2 mode with the VCXO of the master being hold at Vcc/2 by forcing holdover and using a manual DAC voltage setting. It is allowable to configure the master as dual loop and lock PLL1 if a signal generator is available.

is configured to generate a 983.04 MHz clock output from both DCLKout0 and DCLKout2. The master output's SDCLKout1 and SDCLKout3 will be configured to generate a single SYSREF pulse used to reset the dividers in the slave device in distribution mode. The phase of the slave's DCLKout0/SDCLKout1 can be compared against the master's DCLKout2 and SDCLKout3 to confirm the determinism. Naturally the clock outputs of the slave device will be deterministic and this can be measured on DCLKout0/2, SDCLKout1/3.

When connecting the boards together, take care to connect same polarity inputs and outputs. Unless an extra SMA is populated on the LMK04828 Slave board, DCLKout0* (inverting) will connect to CLKin1* (inverting).

4.5.1.3.1 Overview

The basic settings for master and slave are outlined in Table 7.

Table 7 – Case 1a/1b Demo Configuration

Setting	**Master**	**Slave**
Default Mode	Multi SYNC Master, Reference Free, 983.04 MHz, pulser	Multi SYNC Slave – Case 4b, 0-Delay SYSREF re-clocking; Sync from Master
OSCin Frequency	122.88 MHz	122.88 MHz
VCO Frequency	2949.12 MHz	2949.12 MHz
DCLKout0	983.04 MHz (/3)	122.88 MHz (/24)
DCLKout2	983.04 MHz (/3)	245.76 MHz (/12)
SYSREF Divider Frequency	12.288 MHz (/240)	122.88 MHz (/24)
SYSREF Mode	Pulser	Re-Clocked
FORCE_HOLDOVER	1	0
MAN_DAC	512 (Vcc/2)	N/A

4.5.1.3.2 Modify EVMs

Because this example uses the pulser for SYNC/SYSREF from master, it is necessary to modify the master for DC coupled SDCLKout1 output and the slave for DC coupled CLKin0 input. Refer to *APPENDIX B – Instructions for Modifying EVMs*, for detailed instructions.

4.5.1.3.3 Connecting EVMs together

When connecting the boards together, take care to connect same polarity inputs and outputs. Unless an extra SMA is populated on the LMK04828 Slave board, DCLKout0* (inverting) will connect to CLKin1* (inverting).

To connect the EVMs together, refer to the diagram in Figure 20. While the SDCLKout1 of the master must be DC coupled to differentially to CLKin0 of the slave for timing reasons, the outputs of the LMK04828 connected to the oscilloscope may be configured to AC or DC coupled as desired. If it is chosen to connect both the non-inverting and inverting output of an SDCLKout to the oscilloscope, it is recommended to use DC coupling so that the signals will not need time to bias to result in a proper, steady state, differential waveform.

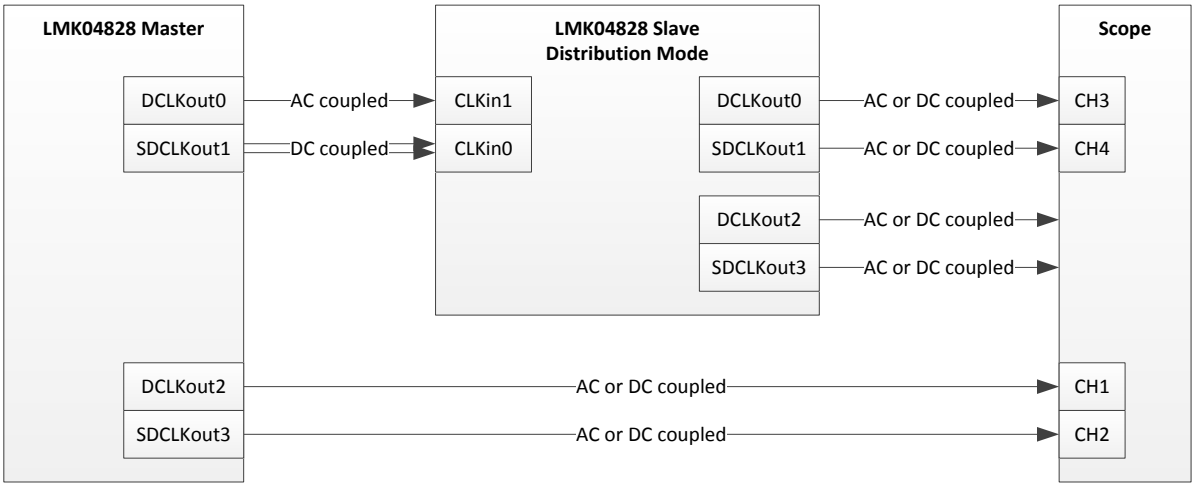

Figure 20 - Synchronization of Distribution LMK04828. PCB and test equipment connection diagram

4.5.1.3.4 Software Setup

Once the EVMs are modified and the connected together, connect the USB2ANYs from the PC to the EVMs. Start two copies of TICS Pro and load the LMK04828B profile for each device. To identify which EVM is being controlled by which TICS Pro instance select “USB communications” on the menu bar, and select “Interface” to open the Communication Setup window. Click the “Identify” button to flash the green LED on the USB2ANY controlled by the specific instance of TICS Pro.

On the TICS Pro controlling the master EVM

- click “Default configurations” on the menu bar, and
- select “Multi-sync demo, master, dual loop, cascaded 0-delay, without reference, 983.04 MHz”
    - This will load the LMK04828B EVM to be in dual loop mode, but will force holdover with a fixed voltage on the 122.88 MHz VCXO so that PLL2 will lock to reliable reference. Frequency may not be exactly 122.88 MHz.
        - When in holdover, output phase noise/jitter at offsets below 12 kHz may be impacted from holdover mode. Different VCXOs will have different sensitivity and offsets at which phase noise may degrade from a locked condition.
    - If it is desired to lock to answer external reference, connect a reference at 122.88 MHz to CLKin1 and uncheck FORCE_HOLDOVER on the User Controls page.

- Click “Write All Registers” button on the toolbar or press “Ctrl-L” to program the master LMK04828.
- Then press the “SYNC Dividers” button to synchronize all the dividers of the master.
- Confirm that the PLL2 DLD LED is lit next to the VCXO.

With the TICS Pro program controlling the slave EVM,

- click “Default configurations” on the menu bar, and
- select “Multi-sync demo, slave, distribution.”
    - This will load the LMK04828B EVM to have both PLLs powered down, route CLKin1 to distribution, and prepare the device to receive a SYNC/SYSREF pulse on CLKin0.
- Click “Write All Registers” button on the toolbar or press “Ctrl-L” to program the master LMK04828.

Now using the TICS Pro for master,

- on the SYSREF Page, click the “Send Pulses” button to launch a SYSREF pulse into the slave’s CLKin0 input. This will synchronize the dividers on the slave.

On the slave device

- on the “Set Modes” tab, click “Disable SYNC on all Dividers” button to prevent the dividers from responding to SYNC/SYSREF now that they’ve been aligned.
- Then select the desired JESD204B mode, “Continuous,” “Pulser,” or “SYSREF Request.”
    - For this example, selection “Continuous” so a continuous stream of SYSREF pulses are output which can be compared with the master.
    - **However in a real application**, “Pulser” would be the normal selection as it is undesirable to send continuous SYSREF pulses because of noise and power consumption.
        - In this real application, pulses would then be sent by programming SYSREF_PULSE_CNT or toggling the SYNC pin.

This concludes then necessary steps to get a system operational.

4.5.1.3.5 Further visualization, testing, and optimization

In a normal application, the system would now be operational, however to assist in visualization, on the master TICS Pro.

- set “Continuous” JESD204B mode to generate continuous SYSREF pulses which may be observed with respect to the slave.

It is also possible to observe the reset of the slave device dividers by observing the impact of reset timing on the device clocks. To do this, with the master in continuous SYSREF mode, on the slave

- On the “Set Modes” page click the “Receive SYNC/SYSREF on CLKin0” button.
    - Now the reset of the device clock maybe observed from slave device.
- On the “Clock Outputs” page uncheck
    - DDLY_PD for CLKout0
    - Change the digital delay value by adjusting the two comboboxes immediately below the DDLY_PD. Half Step may also be checked.

To determine the position in the valid window for the slave to properly receive the SYNC/SYSREF signal with respect to its device clock, on the master refer to APPENDIX C – Adjusting Timing from a Master Device for maximum setup and Hold Time.

4.5.1.4 General Usage of TICS Pro

For any given setup, to get to a device in clock distribution mode to sync, on the Set Modes page, click…

- "Set Distribution" to put the device into distribution mode.
- "Reclocked CLKin0" to set CLKin0 to reset dividers.
- "Enable SYNC for SYSREF" and "Enable SYNC for CLKout Dividers"

Once SYNC occurs, click "Disable SYNC for all Dividers"

Naturally all device clock and SYSREF clock outputs need to be configured as desired.

4.5.2 Case 2a/b: 0-Delay with SYSREF as Input Frequency for Single or Dual Loop

4.5.2.1 Overview

An LMK0482x configured to operate in nested 0-Delay mode with the SYSREF Divider included in the feedback loop allows the PLL1 phase detector to lock the phase of the reference to the feedback divider. Because the reference is the SYSREF frequency and the feedback divider outputs the SYSREF frequency, the PLL will lock with the phases of the reference and SYSREF divider match. Because the same reference is fanned out to multiple LMK0482x devices, the phase of all the SYSREF dividers will be in phase by closed loop 0-Delay mode.

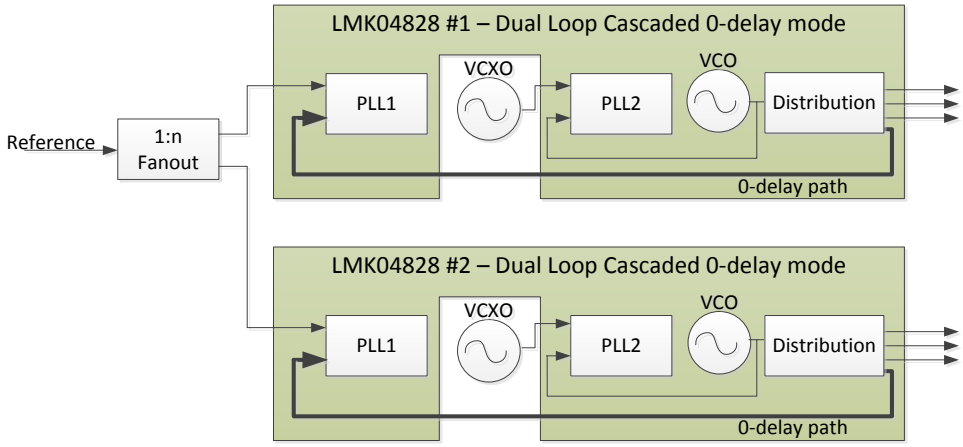

Figure 21 - Using SYSREF frequency as reference to allow 0-delay to synchronize clocking devices

This SYSREF reference frequency technique can be used in both single and dual loop modes, but because SYSREF is typically a low frequency, using SYSREF as a reference or feedback frequency requires the phase detector to be limited to the SYSREF frequency. Small phase detector frequencies can result in narrower loop bandwidths and higher PLL noise so it is best to use the dual loop mode for best jitter performance when phase noise at low offsets is critical to the application. Since PLL1 of the dual loop is typically configured to operate with a narrow loop bandwidth to attenuate reference and PLL noise with the VCXO noise performance, the dual loop mode suits this technique. This does not preclude use in single loop mode, the integrated VCO performance of the LMK0482x is able to provide very good output phase noise and jitter cleaning at offsets above 10 kHz.

4.5.2.2 Procedure to Synchronize

4.5.2.2.1 Synchronize LMK0482x dividers

Synchronize the dividers of the master and all slave devices. Refer to 4.2 Synchronization of outputs of a single LMK0482x device.

4.5.2.2.2 Automatic Phase Alignment by 0-Delay

Once all PLLs are locked, all SYSREF clocks and clocks which have a GCD(SYSREF Frequency, Clock Frequency) equal to SYSREF Frequency, provided SYSREF frequency less than clock frequency, will have deterministic phase with one another.

The 0-delay feature using SYSREF divider as feedback requires all SYSREF divider outputs to be in phase if the PLLs are to be locked.

4.5.2.2.3 Output of SYSREF

SYSREF may now be generated at any time from any device to synchronize converters or logic devices. The SYSREF pulse will always be deterministic with one another if GCD(SYSREF frequency, other clock output frequency also requiring deterministic phase) less than SYSREF frequency. In this case, this lower GCD calculated frequency must be provided to the input.

4.5.3 Case 3a/3b: Single or dual loop operation using divider reset

4.5.3.1 Overview

When operating an LMK0482x device with a PLL, simply providing a SYNC signal to CLKin0 can reset all the divides of slave device. The path marked in red of Figure 22 shows how the external SYNC/SYSREF will reset all the Clock Output and SYSREF Dividers. The SYNC pin could also be used.

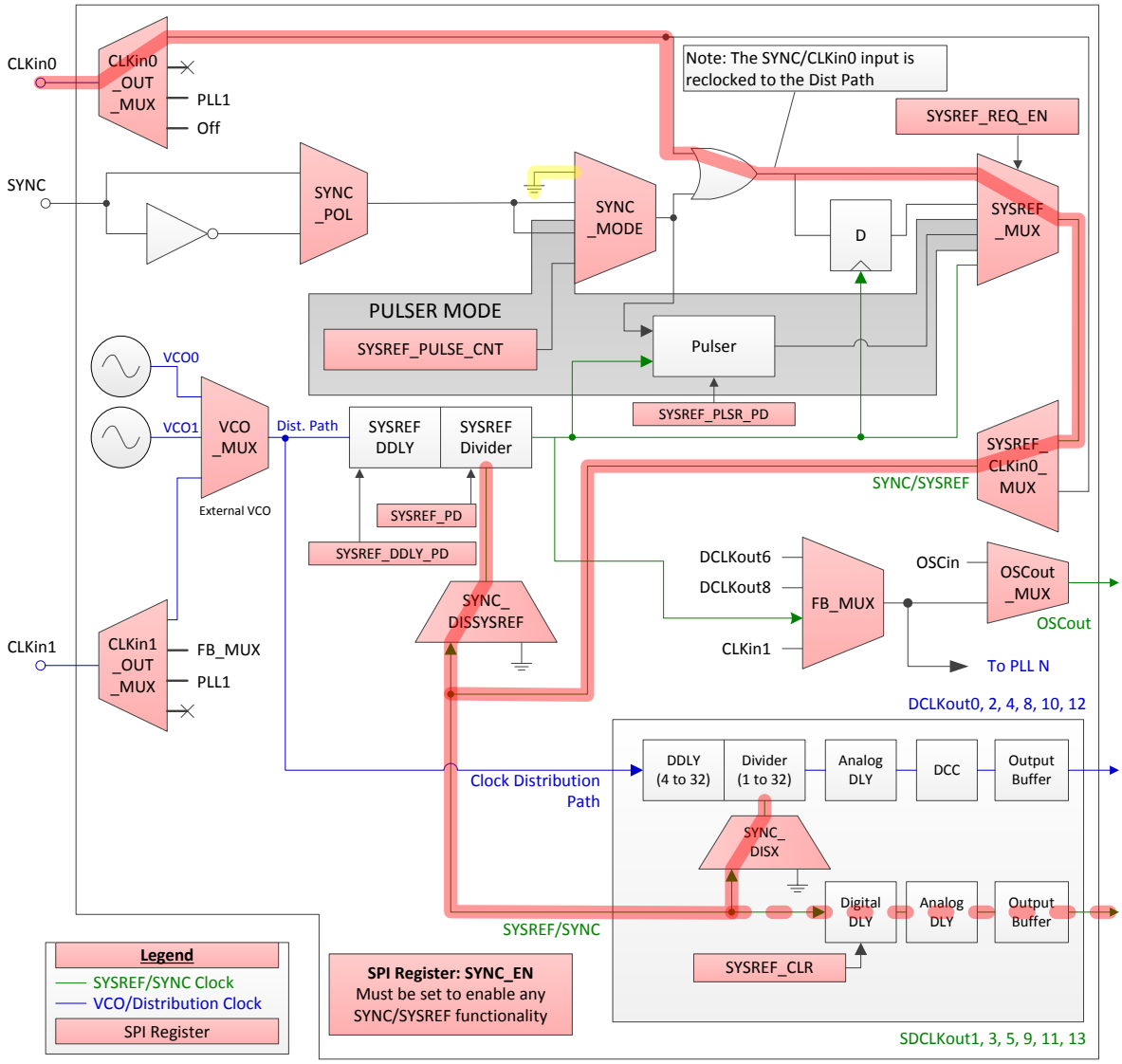

Figure 22 - Direct SYNCing of CLKout and SYSREF Divides

After this synchronization is complete, the slave device can re-program the SYSREF_MUX to provide pulser or continuous SYSREF output.

4.5.3.2 Pros

Because the SYSREF divider can be reset, the SYSREF divider can provide a SYSREF frequency different from the master.

4.5.3.3 Cons

One risk is that some slave devices may be off +/- n distribution clock cycles from each other, especially when the SYNC pin is used instead of CLKin0. Note that +/- n distribution clock cycle cycles may be less than +/- n device clock cycles as the device clock may be operating at a lower frequency that the distribution clock path. The distribution clock path typically operates at the VCO frequency. For example, if the VCO frequency is 3000 MHz and the clock output frequency is 500 MHz, if +/- 1 distribution clock cycle error occurs, this translates to +/- 0.167 device clock error.

Because the SYSREF and clock dividers are driven by the clock distribution path which can operate at high frequencies, on the order of 3 GHz, meeting the setup and hold time to the 3 GHz VCO results in a small valid window.

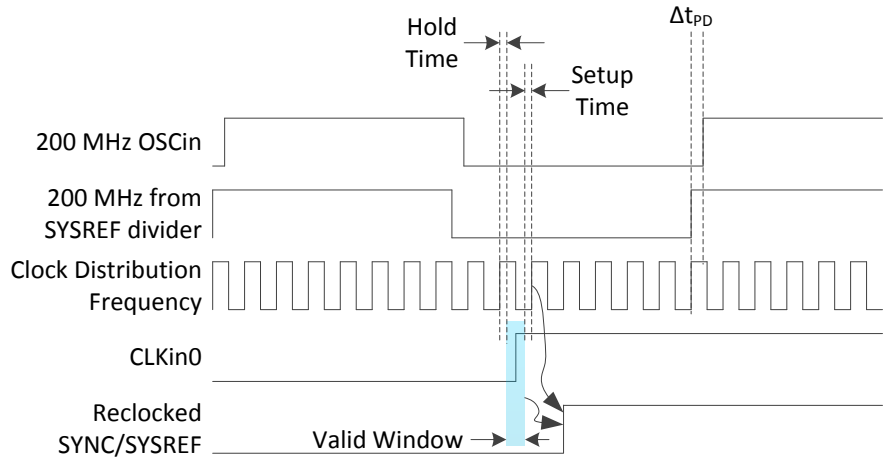

Figure 23 - Setup and hold time to VCO period results in a very small valid window

Meeting the setup and hold time to a 3 GHz clock can be done and is illustrated for distribution mode in section *4.5.1 Case 1a/b/c: Synchronization of* multiple LMK0482x in Distribution mode. **However the challenge in a PLL mode for meeting setup and hold time to VCO clock (clock distribution clock) is that only the phase of the PLL reference is known, not the exact phase of the VCO/Clock Distribution path.** Because the phase between the PLL reference and VCO is fixed it is possible to achieve repeatable results in a lab setting, but analog phase variation over PVT between reference and VCO frequency phase may result in little to no valid window depending on design requirements. Characterization over some variables of PVT may allow the user to use this mode to achieve deterministic SYNC between multiple devices. Refer to **Error! Reference source not found.** to see example data.

To address the difficulty of meeting the setup and hold time to the VCO/Clock Distribution Path when in a single PLL mode, see sections, *4.5.4* Case 4a: Single loop 0-delay operation with SYSREF re-clocking; sync only local dividers and 4.5.5 Case 4b: Single loop 0-delay operation with SYSREF re-clocking; sync slave dividers from master. These address the challenge of difficult to meet setup and hold times to high speed VCO by using 0-delay to relax requirements to meeting setup and hold to the reference frequency. Compare Figure 23 (this case) with **Error! Reference source not found.** (re-clocked case) to ee the difference in the length of the valid window when synchronizing against a VCO period vs. synchronizing against the reference period.

4.5.3.4 Procedure to Synchronize

4.5.3.4.1 Prepare to Synchronize Dividers

The slave LMK0482x is programmed as illustrated in Figure 22 to allow CLKin0 to reset all dividers. Follow recommended programming sequence from datasheet. Program device registers, the device must be programmed to lock.

Table 8 - Basic register programming for case 3a/3b

Address	Field	Value	Definition
If using PLL1			
	CLKin0_OUT_MUX	**0**	**CLKin0 is used to provide SYNC signal to dividers.**
	PLL1_N_MUX*	0	Select OSCin for PLL2. (Not 0-delay)
PLL2			
	PLL2_N_MUX	0	Select PLL2_P for PLL2. (Not 0-delay)
SYNC/SYSREF Signal Path, for steady state operation.			
	SYNC_1SHOT_EN	**1**	**Recommend setting one shot to enable synchronization to the rising edge of SYNC/SYSREF input**
	SYNC_MODE	**0**	**Disable SYNC pin**
	SYSREF_MUX	**0**	**Normal SYNC. CLKin0 directly drives SYNC/SYSREF path.**
	SYSREF_CLKin0_MUX	**0**	**SYSREF_MUX source**
Clock Outputs & SYSREF Divider, as needed			
	SYNC_DISSYSREF	0	Enable SYSREF divider reset
	SYSREF_DDLY_PD	0	Enable SYSREF digital delay
	SYSREF _DDLY	?	As desired for SYSREF DDLY
	SYNC_DISX	0	Enable DCLKoutX divider reset
R262[7], … (Multiple)	DCLKoutX_DDLY_PD	0	Enable DCLKoutX_DDLY_PD
R257[0:3],[4:7], … (Multiple)	DCLKoutX_DDLY_CNTL DCLKoutX_DDLY_CNTH	? ?	As desired for device clock DDLY

* Only needed if dual loop mode is used.

At this time, with a reference signal present on OSCin, PLL2 will lock to reference. If dual loop is being used the reference will be some voltage controlled oscillator, typically a VCXO and PLL1 will also lock to the reference.

The phase between OSCin and the outputs, and even the outputs with one another will not be deterministic.

4.5.3.4.2 Synchronize PLL R Dividers

When PLL# Total N / PLL# R reduces to x/1, then no synchronization of PLL R dividers is required.

4.5.3.4.3 Synchronize Clock and SYSREF Dividers

It is assumed that the master has synchronized its own dividers internally and then reconfigures to provide a SYNC/SYSREF signal to the slave device.

When the master LMK0482x outputs a SYNC/SYSREF pulse to slave, the dividers programmed for divider reset will be synchronized. Synchronization between all dividers on the slave device is deterministic.

Determinism between reference and outputs requires a valid setup and hold time of the SYNC/SYSREF pulse to the clock distribution path. Because the setup and hold time from SYNC/SYSREF to clock distribution path can't be directly measured, some characterization may be required to find the center of the valid window with respect to the reference. There will be a fixed phase relationship between the reference clock and the clock distribution path. Using calibration information for the device for PVT can assist in achieving +/- 0 clock distribution path error. Otherwise +/- n clock distribution path error will be experienced.

In addition to meeting the setup and hold requirements, for the phase between reference and clock distribution path to be deterministic, so no N:1 phase case caused by irreducible R divider as discussed in the theory section is permitted. Methods eliminate N:1 uncertainty due to N/R non-reduction are currently being addressed.

4.5.3.4.4 Output of SYSREF

The slave LMK0482x is now synchronized to +/- n clock distribution path cycles to the master, where n is some integer 0 or higher. Device clocks and SYSREF clocks produced from the single slave device will behave as in a single LMK0482x system.

Set synchronization disable bits to prevent CLKin0 or local SYNC/SYSREF from disrupting the dividers.

Address	Field	Value	Definition
Synchronization and clock routing path specific registers			
R324[0,1,2, 3,4,5,6, 7]	SYNC_DISX, SYNC_DISSYSREF	1	Prevent local divider reset.
	SDCLKoutY_PD	0	Power up sysref output
	SDCLKoutY_MUX	1	Select SYSREF for SDCLKoutY
	SYSREF_GBL_PD	0	If SDCLKoutY_DIS_MODE is set to a conditional setting, setting this bit to 0 allows SYSREF to operate
	SDCLKoutY_DIS_MODE	0, 1, or 2	0 will result in SDCLKoutY always active, but setting 1 or 2 will require SYSREF_GBL_PD = 0 for output from SDCLKoutY.
	SYSREF_CLR	0	SYSREF Clear must be 0 to allow SYSREF to output. SYSREF_CLR is used in part to reset the SDCLKoutY_DDLY from producing random pulses on initial power-up.

SYSREF can now be produced locally using any mode. Pulser mode is commonly used.

4.5.3.5 Example

Figure 24 illustrates one way the master and slave can be configured for operation together. The slave must be first configured to accept the SYNC/SYSREF pulse directly to the dividers for reset, then re-configured for pulser mode at which time either device can be triggered to generate SYSREF pulses using their local SYSREF pulsers.

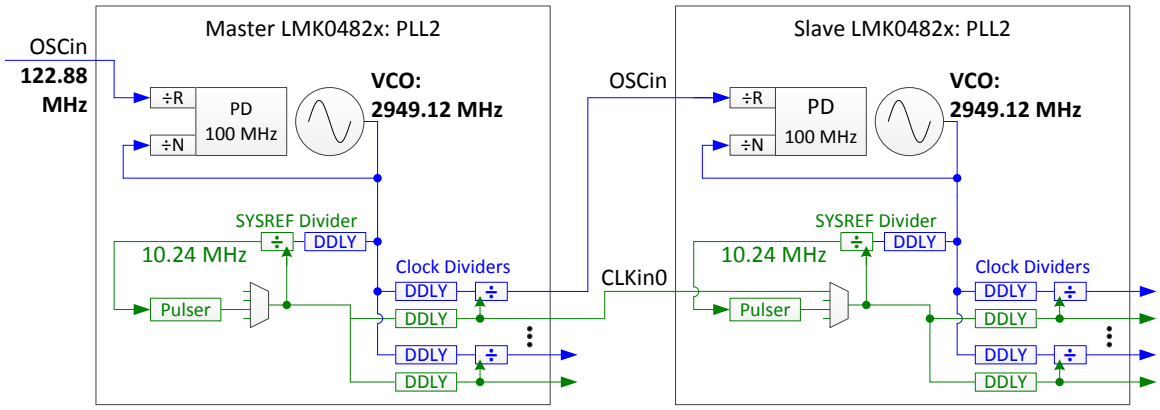

Figure 24 - Master and Slave LMK0482x when SYNCing the slave dividers sourced by VCO

If any PLL R divider cannot reduce to 1 when considering the fraction PLL Total R / PLL Total N, then this technique cannot assure deterministic phase. Refer to section 3.3.2.2, Case 2, 0-delay to align 60 MHz reference with 40 MHz clock output.

4.5.4 Case 4a: Single loop 0-delay operation with SYSREF re-clocking; sync only local dividers

4.5.4.1 Overview

An LMK0482x configured to operate in 0-delay, single loop mode, using the SYSREF divider as 0-delay feedback programmed to the same frequency as the reference input will result in deterministic phase between the input reference, OSCin, and all clock outputs, provided the first and second rule of 0-Delay determinism are met. See section 3.3.1, 0-Delay Rules for Determinism. For rule #2, the SYSREF frequency divider must be the lowest frequency. Provided these rules are met, simply syncing the dividers of each device according to section 4.2, Synchronization of outputs of a single LMK0482x device, will result in deterministic device clocks at all outputs.

To provide a deterministic SYSREF, the slave will re-clock the master's SYSREF onto the clock distribution path using the SYSREF divider. Because the SYSREF divider operates at the reference frequency, there is a deterministic re-clocking edge for every reference edge.

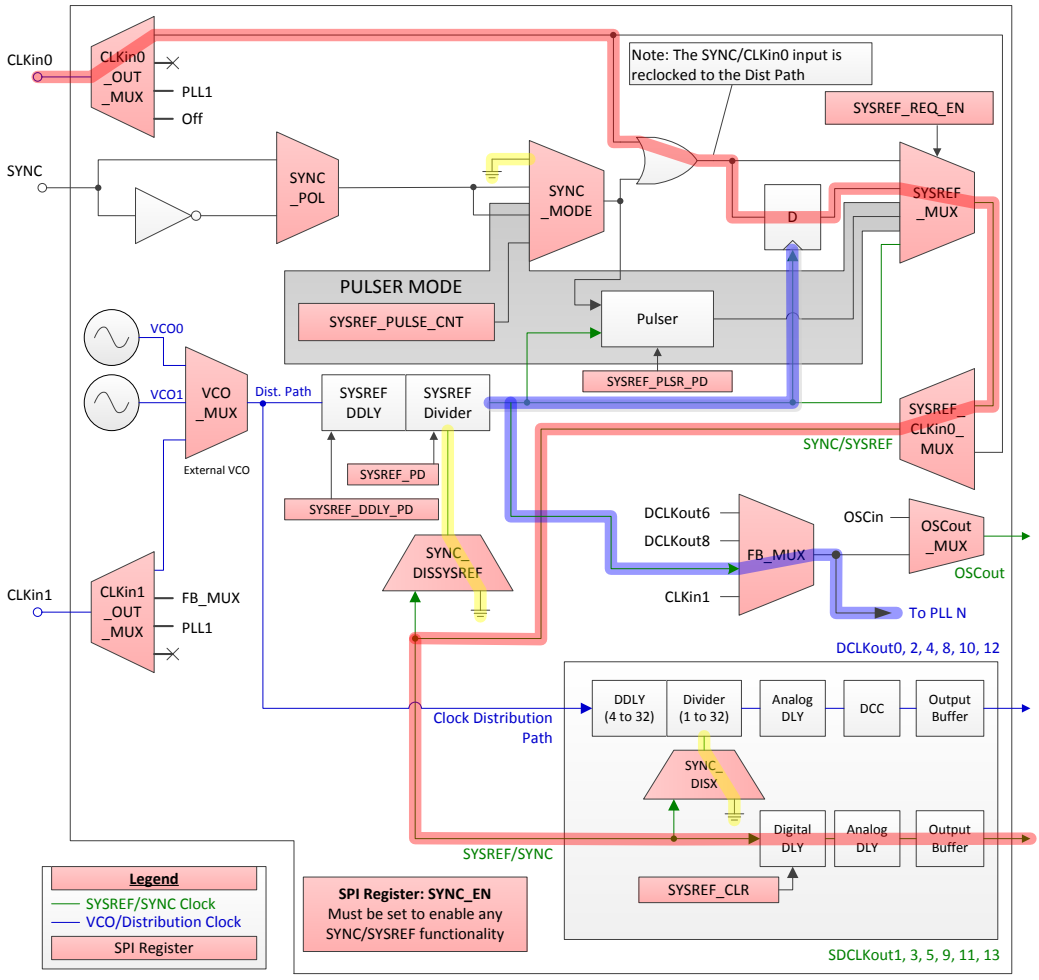

Figure 25 - Re-clocking CLKin0 with SYSREF Divider, SYSREF Divider also feedback to PLL N for 0-Delay

In Figure 25 the blue marked path shows the SYSREF divider being used to re-clock the input SYNC/SYSREF and also be feed back to the PLL to allow 0-delay.

The red path shows the external SYNC/SYSREF passing through the D flip-flop, at which point the external SYNC/SYSREF gets re-clocked to the phase domain of the Clock Distribution Path. The SYNC/SYSREF continues to the output where digital and analog delay can be used to adjust the phase of the SYSREF to the Device Clock.

The yellow marked paths show in steady state operation mode, the SYNCs are disabled from all dividers. At the start, SYNC was allowed to synchronize all the dividers of the slave device.

4.5.4.2 Pros

Because master and slave are synchronized by themselves, then 0-delay takes care of all alignment, this is a simple mode to use for phase determinism.

When sending SYSREF, because the master generates all SYSREF, synchronizing an entire system is as simple as causing one device, the master to send SYSREF pulses.

The re-clocking of the external SYNC/SYSREF input to by the SYSREF divider results in large valid windows for the master which makes establishing deterministic SYSREF between multiple LMK0482x easy. Figure 26 illustrates the very wide valid window for SYNC/SYSREF possible in this mode. The phase variation from the PLL phase detector is small compared with the period of the reference frequency.

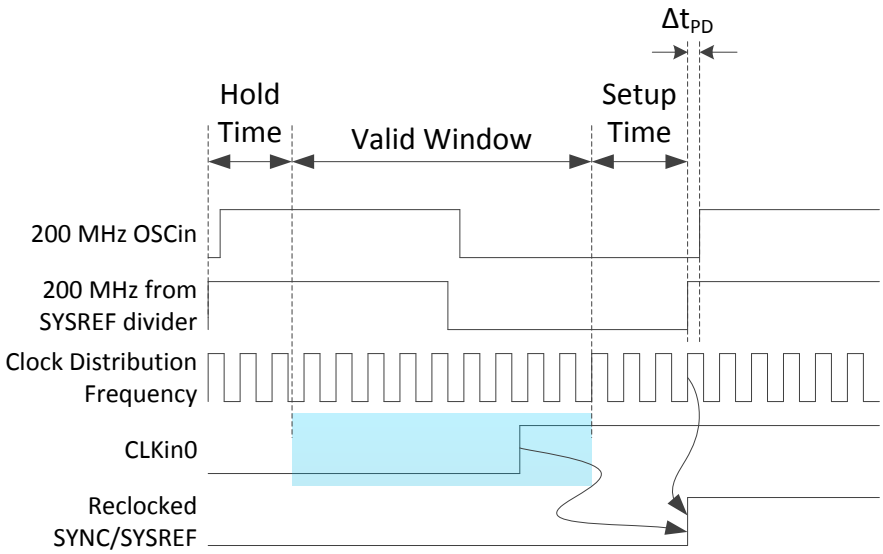

Figure 26 - Valid window illustrated resulting from setup and hold time taken from reference frequency

4.5.4.3 Cons

- In some systems, output frequencies of the slave device may not satisfy the 0-delay rules for determinism. In this case refer to

Case 4b: Single loop 0-delay operation with SYSREF re-clocking; sync slave dividers from master.

The SYSREF frequency is set by the master. It is still possible to control individual delivery of SYSREF by programming the various master and slave devices.

4.5.4.4 Procedure to Synchronize

4.5.4.4.1 Prepare for Synchronization

Follow recommended programming sequence from datasheet. The device must be programmed to lock PLL2 in 0-delay mode using SYSREF divider as feedback.

Table 9 - Key registers for case 4a

Address	Field	Value	Definition
PLL2 to lock with SYSREF divider as feedback			
	PLL2_N_MUX	**1**	**Select Feedback Mux for PLL2**
	FB_MUX_EN	**1**	**Enable Feedback Mux**
	FB_MUX	**2**	**Select SYSREF Divide for Feedback**
SYNC/SYSREF Signal Path, for steady state operation.			
	SYNC_POL	?*	As needed for SYNC pin input. For low SYNC pin, set to 0.
	SYNC_MODE	**0***	**Disable SYNC pin**
	SYSREF_MUX	**1***	**Re-clocked SYSREF**
	SYSREF_CLKin0_MUX	**0**	**SYSREF_MUX source**
Clock Outputs, as needed			
R262[7], … (Multiple)	DCLKoutX_DDLY_PD	0	Enable DCLKoutX_DDLY_PD
R257[0:3],[4:7], … (Multiple)	DCLKoutX_DDLY_CNTL DCLKoutX_DDLY_CNTH	? ?	As desired for device clock DDLY

* Will be momentary set to another value for local synchronization at system start-up.

With a reference signal present on OSCin, PLL2 will lock to reference, however the phase between the outputs will not yet be deterministic.

4.5.4.4.2 Synchronize dividers

Now all the used dividers of slave device are synchronized. Refer to 4.2 Synchronization of outputs of a single LMK0482x device. It is required to synchronize the divides of the master also by the same method.

To synchronize the dividers, it is suggested to ensure a steady state of the SYNC pin and use a software SYNC by toggling the SYNC_POL bit.

4.5.4.4.3 Auto phase alignment

With synchronized dividers and 0-delay mode, the phase of the output clocks will become deterministic with the output clocks of the master and other slave devices. This occurs when the PLLs become locked.

4.5.4.4.4 Output of SYSREF

To ensure the slave device is prepared to output SYSREF, set the SYSREF_CLR bit = 1 for at least 15 clock VCO clock cycles before clearing again.

For the master to output SYSREF through the slave, the following registers are key to allow an input on CLKin0 or SYNC pin to re-clocked onto the Clock Distribution Path domain, be propagated to the outputs. Only the CLKin0 or SYNC pin input path is required to be programmed. CLKin0 is a high performance path and is recommended. A continuously toggling SYNC pin may cause crosstalk to VCO.

SYNC/SYSREF Signal Path, for steady state operation using CLKin0 as input			
	SYNC_MODE	0	Disable SYNC pin
	CLKin0_TYPE	?	Bipolar or MOS as desired
	CLKin0_OUT_MUX	0	Deliver CLKin0 to SYSREF_MUX
SYNC/SYSREF Signal Path, for steady state operation using SYNC pin as input			
	SYNC_POL	?	As required for desired polarity. Typically 0.
	SYNC_MODE	1	Use SYNC pin
	CLKin0_OUT_MUX	3	CLKin0 is not required, turn off.
Common			
	SYSREF_MUX	1	Re-clocked SYSREF
	SYSREF_CLKin0_MUX	0	SYSREF_MUX source

To ensure well behaved SYSREF output, particularly across PVT, the timing of the SYSREF input to CLKin0 or SYNC pin must meet setup and hold time with respect to the OSCin signal.

4.5.4.5 Example

In this example two LMK0482x EVMs will be used. To simplify evaluation equipment requirements, the master will be configured in a PLL2 mode with the VCXO of the master being held at Vcc/2 by forcing holdover and using a manual DAC voltage setting. It is allowable to configure the master as dual loop and lock PLL1 if a signal generator is available.

The master will be configured in SYSREF continuous mode to simplify visualization of the phase determinism. However at the end of the example, an option to use pulser mode will be illustrated. To use pulser mode, the SDCLKout1 of the master and the CLKin0 of the slave EVMs must be modified as described in APPENDIX B – Instructions for Modifying EVMs.

4.5.4.5.1 Overview

The basic settings for master and slave are outlined in Table 10.

Table 10 – Case 4a Demo Configuration

Setting	**Master**	**Slave**
Default Mode	Multi SYNC Master, Reference Free, 122.88 MHz, continuous	Multi SYNC Slave – Case 4a, 0-Delay SYSREF re-clocking; Sync Local
OSCin Frequency	122.88 MHz	122.88 MHz

VCO Frequency	2949.12 MHz	2949.12 MHz
DCLKout0	122.88 MHz (/24)	122.88 MHz (/24)
DCLKout2	122.88 MHz (/24)	245.76 MHz (/12)
SYSREF Divider Frequency	12.288 MHz (/240)	122.88 MHz (/24)
SYSREF Mode	Continuous	Re-Clocked
FORCE_HOLDOVER	1	0
MAN_DAC	512 (Vcc/2)	N/A

Figure 27 illustrates the interfacing of the master and slave devices. Alternate configurations could be used as described in section 4.4, Topologies of connecting Multiple LMK0482x Devices together for improved phase noise performance.

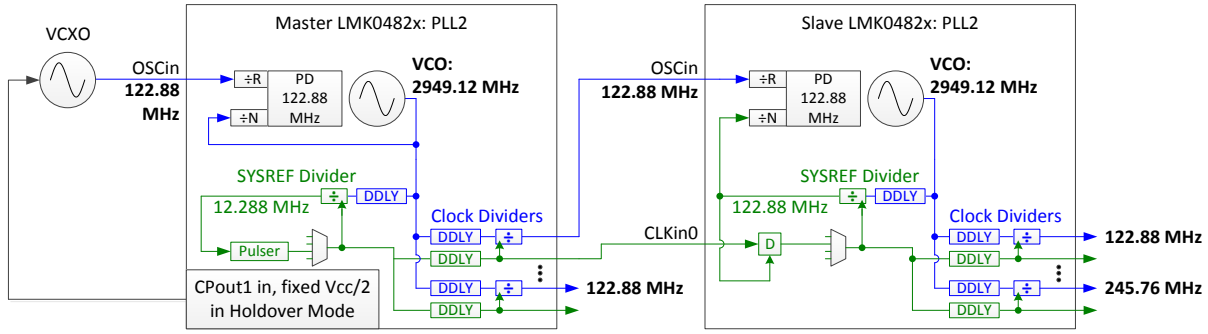

Figure 27 - Master and Slave LMK0482x. Slave case 4a to achieve synchronization with master. Optional: master uses SYSREF continuous mode.

4.5.4.5.2 Connecting EVMs Together

The slave EVM must be modified to accept external reference for PLL2 on OSCin. Refer to section 4.8, Modify EVM for Single Loop Operation for details.

Figure 28 illustrates the connections between the two EVMs from an SMA level. Connect like polarities, for instance, if connecting to slave OSCin*, use DCLKout0* and not DCLKout0.

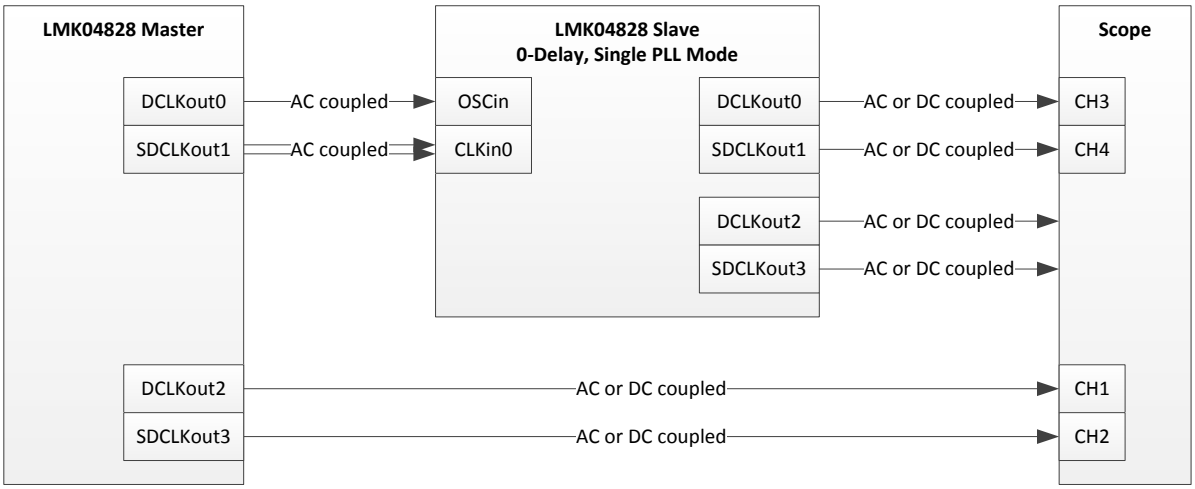

Figure 28 - Using re-clocked SYNC/SYSREF on LMK0482x Slave Device to simply timing for determinism

Because of the cascade nature of the master and slave, the phase of the clock outputs from master from slave could vary slightly. Any delay can be minimized to within ~¼ VCO clock cycle by using the half step

delay on the device clock outputs. However over temperature, the slave device would have additional propagation delay variation from OSCin to OSCout. To eliminate this, simply use a separate splitter or fan-out buffer to provide the reference to each device. One LMK0482x device will still be master, connect the SDCLKout of the master to the slave as in **Error! Reference source not found.**.

4.5.4.5.3 Software Setup

Once the EVMs are modified and the connected together, connect the USB2ANYs from the PC to the EVMs. Start two copies of TICS Pro and load the LMK04828B profile for each device. To identify which EVM is being controlled by which TICS Pro instance select "USB communications" on the menu bar, and select "Interface" to open the Communication Setup window. Click the "Identify" button to flash the green LED on the USB2ANY controlled by the specific instance of TICS Pro.

On the TICS Pro controlling the master EVM

- click "Default configurations" on the menu bar, and
- select "Multi SYNC Master, No Reference, 122.88 MHz"
    - This will load the LMK04828B EVM to be in dual loop mode, but will force holdover of PLL1 with a fixed voltage on the 122.88 MHz VCXO so that PLL2 will lock to reliable reference. Frequency may not be exactly 122.88 MHz.
        - When in holdover, output phase noise/jitter at offsets below 12 kHz may be impacted from holdover mode. Different VCXOs will have different sensitivity and offsets at which phase noise may degrade from a locked condition.
    - If it is desired to lock to answer external reference
        - Connect a reference at 122.88 MHz to CLKin1
        - Uncheck FORCE_HOLDOVER on the User Controls page
        - Change PLL1_LD_MUX = "PLL1 DLD" on the Status page so that Status_LD1 pin and LED reflect PLL1 DLD instead of holdover mode active.
- Click "Write All Registers" button on the toolbar or press "Ctrl-L" to program the master LMK04828.
- **Then press the "SYNC Dividers" button to synchronize all the dividers of the master.**
- Confirm that the PLL2 DLD LED is lit next to the VCXO.

With the TICS Pro program controlling the slave EVM,

- click "Default configurations" on the menu bar, and
- select "Multi SYNC Slave – Case 4a, 0-Delay SYSREF re-clocking; Sync Local."
    - This will load the LMK04828B EVM to have PLL2 powered up and configured for locking using 0-Delay of SYSREF Divider. It will also route CLKin0 to SYSREF in Re-Clocking Mode with all divider SYNC functions disabled.
- Click "Write All Registers" button on the toolbar or press "Ctrl-L" to program the master LMK04828.
- **To get deterministic phase from master to slave, click the "Sync Dividers" button to synchronize all the dividers of the slave device.**
    - The SYNC Dividers button automatically.
        - Temporarily disables CLKin0 input, so no stray SYNCs are received from master.

- Sets up the SYNC/SYSREF path for “Normal SYNC” using the SYNC pin.
- Expects the input pin state of SYNC pin to be constant.
- Allows SYNC to all dividers by setting SYNC_DISSYSREF = 0 and SYNC_DISX = 0 for all clock dividers which drive outputs that are powered up.
- Then toggles the SYNC_POL according to the set pin state of the SYNC pin in the GUI.
- Prevents SYNC to all dividers by setting SYNC_DISSYSREF = 1 and SYNC_DISX = 1.
- Then reverts the SYNC/SYSREF path to previous state. (Re-clocked SYSREF) and CLKin0 to drive SYSREF_MUX.

This concludes then necessary steps to get the LMK0482x devices synchronized.

4.5.4.5.4 Control of specific SDCLKoutY / Powerdown SYSREF after use

To control which devices/device outputs are outputting SYSREF, it is possible to power down the output to disable. It is also possible to use the SDCLKoutY_DIS_MODE and SYSREF_GBL_PD to control the state of the SDCLKoutY of a single LMK0482x. By setting SDCLKoutY_DIS_MODE = 2, Conditional Vcm; when SYSREF_GBL_PD = 1; then all these outputs will be held is a reduced power state. It is also possible to further power down the entire SYSREF output buffer.

4.5.4.5.5 Using SYSREF Pulser Mode

If desired, to use SYSREF pulser instead of continuous SYSREF, to ensure valid signals at CLKin0, it is recommended to perform the DC SDCLKout1 modification to the master board and the DC CLKin0 modification to the slave board. These are outlined in section 4.6 Modify Master EVM for DC coupled SDCLKout1 operation and 4.7 Modify Slave EVM for DC coupled CLKin0 operation.

Once the hardware is updated, on the TICS Pro SYSREF page of the master LMK0482x:

- Click SYSREF_CLR on.
- Uncheck SYSREF_PLSR_PD
- Click SYSREF_CLR off.
- Change SYSREF_MUX to Pulser.
- Change SYNC_MODE to SYNC SPI (Pulser)
- To send pulses, click “Send Pulses” button. Changing the SYSREF_PULSE_CNT will also send
- pulses out. With SYNC SPI (Pulser) set, the act of programming the SYSREF_PULSE_CNT register initiates the pulser.

4.5.5 Case 4b: Single loop 0-delay operation with SYSREF re-clocking; sync slave dividers from master

4.5.5.1 Overview

An LMK0482x configured to operate in 0-delay, single loop mode, using the SYSREF divider as 0-delay feedback programmed to the same frequency as the reference input will result in deterministic phase between the input reference, OSCin, and the SYSREF Divider.

To provide determinism of a slave clock output phase to the master, the master will provide a SYNC/SYSREF signal to CLKin0 which is deterministically re-clocked by the SYSREF divider. All clock output dividers which allow SYNC will now have a deterministic relationship to that SYNC/SYSREF signal. In this use case, during this synchronization the SYSREF divider must never be reset.

After the SYNC of the slave's clock output dividers, the slave will re-program sync disable registers to prevent the CLKout dividers from being reset again. The slave will then re-clock any pulses from the master's SYSREF output onto the clock distribution path using the SYSREF divider.

In both the initial synchronization and then later SYSREF operation, because the SYSREF divider of the slave operates at the reference frequency, there is a deterministic re-clocking edge for every reference edge. Figure 29 illustrates the signal flow during the initial divider SYNC of the slave.

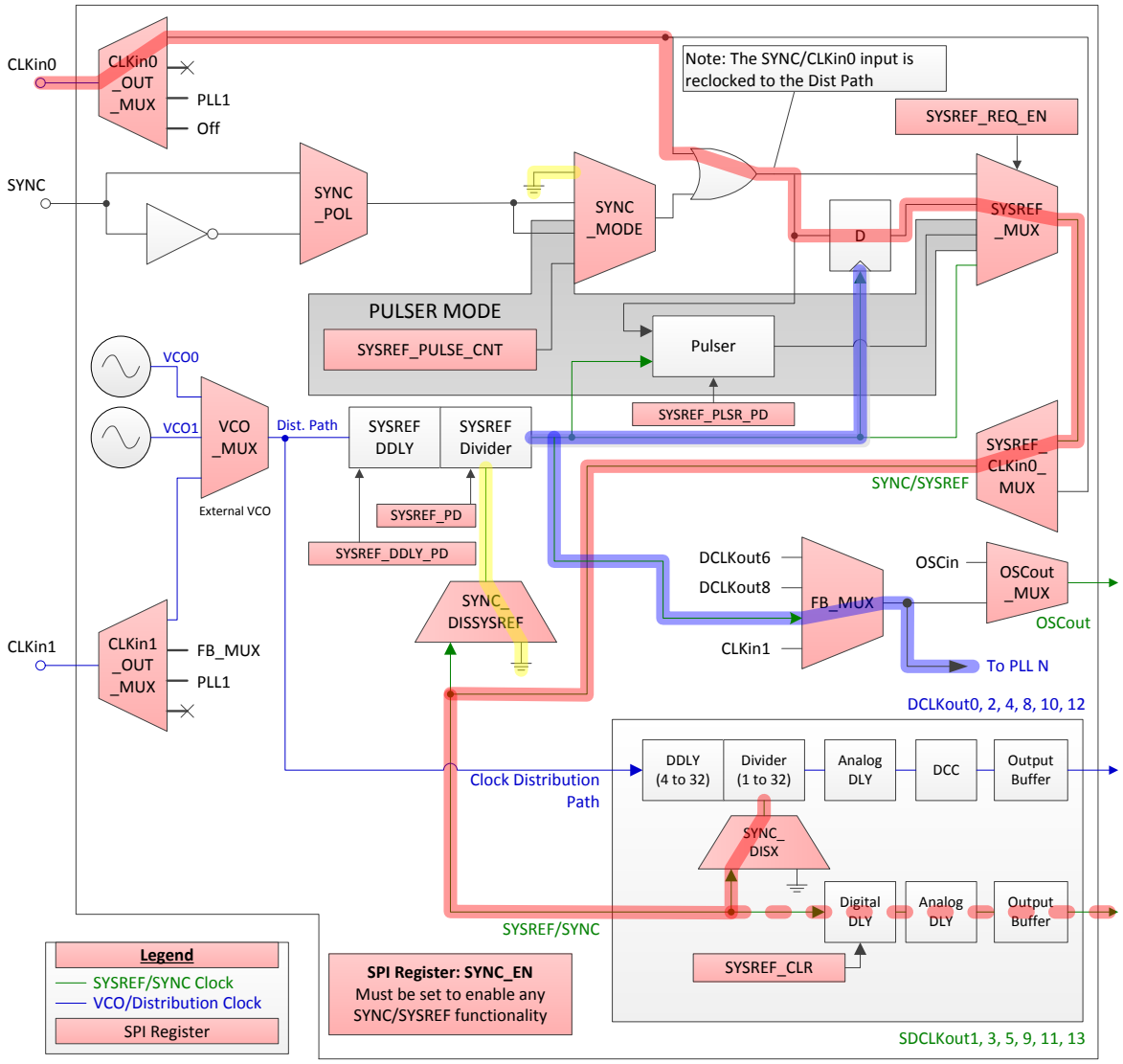

Figure 29 - Using Re-Clocked SYNC/SYSREF to reset clock output dividers, but not SYSREF Divider.

In Figure 29 the blue marked path shows the SYSREF divider being used to re-clock the input SYNC/SYSREF and also be feed back to the PLL to allow 0-delay. Because the SYSREF divider is clocked by the Clock Distribution Path, the re-clocked SYNC has a tight phase relationship to the Clock Distribution Path.

The red path shows the external SYNC/SYSREF passing through the D flip-flop, at which point the external SYNC/SYSREF gets re-clocked to the phase domain of the Clock Distribution Path. The SYNC/SYSREF continues to the output where digital and analog delay can be used to adjust the phase of the SYSREF to the Device Clock.

The yellow marked paths show in operation mode, the SYNCs are disabled from all dividers.

4.5.5.2 Pros

Because the dividers of the slave device are synchronized by the SYNC/SYSREF from the master device, the phase determinism will now exist for outputs which satisfy the equation, SYSREF Frequency = GCD(SYSREF Frequency, Output Frequency). This is an improvement over section 4.5.4, Case 4a: Single loop 0-delay operation with SYSREF re-clocking; sync only local dividers. If the SYNC/SYSREF pulse can be considered a one shot, determinism applies to all clock outputs.

The re-clocking of the external SYNC/SYSREF input by the SYSREF divider results in large valid windows for the master which makes establishing deterministic SYSREF between multiple LMK0482x easy. Figure 30 illustrates the wide valid window for SYNC/SYSREF possible in this mode. The phase variation, Δt_{PD}, from the PLL phase detector is small compared with the period of the reference frequency.

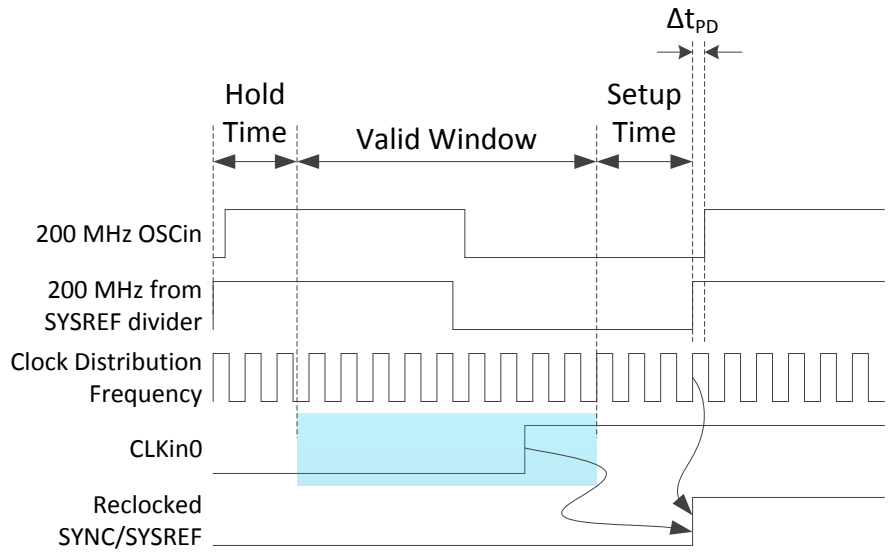

Figure 30 - Valid window illustrated resulting from setup and hold time taken from reference frequency

4.5.5.3 Cons

The procedure to synchronize both master and slave together is more complicated than in section 4.5.4, Case 4a: Single loop 0-delay operation with SYSREF re-clocking; sync only local dividers.

4.5.5.4 Procedure to Synchronize

4.5.5.4.1 Prepare for Synchronization

Follow the recommended programming sequence from the datasheet. Program all device registers in the order specified by datasheet. The slave device programmed to lock in PLL2 0-delay mode using SYSREF divider as feedback.

Table 11 - Key settings for case 4b

Address	Field	Value	Definition
PLL2 to lock with SYSREF divider as feedback			
	PLL2_N_MUX	**1**	**Select Feedback Mux for PLL2**
	FB_MUX_EN	**1**	**Enable Feedback Mux**

	FB_MUX	**2**	**Select SYSREF Divide for Feedback**
SYNC/SYSREF Signal Path, for steady state operation.			
	SYNC_MODE	**0**	**Disable SYNC pin**
	SYSREF_MUX	**1**	**Re-clocked SYSREF**
	SYSREF_CLKin0_MUX	**0**	**SYSREF_MUX source**
	SYNC_1SHOT_EN	**1**	**Reset divides on rising edge of SYNC**
	SYNC_DISSYSREF	**1**	**SYSREF Divider is never reset**
	SYNC_DISX	**0**	**Allow SYNC for DCLKout dividers as needed**
Clock Outputs, as needed			
R262[7], … (Multiple)	DCLKoutX_DDLY_PD	0	Enable DCLKoutX_DDLY_PD
R257[0:3],[4:7], … (Multiple)	DCLKoutX_DDLY_CNTL DCLKoutX_DDLY_CNTH	? ?	As desired for device clock DDLY

4.5.5.4.2 Synchronize dividers

It is assumed that the master has synchronized its own dividers internally and then reconfigured to provide a SYNC/SYSREF signal to the slave device. Typically this is done using the pulser mode, but continuous SYSREF could also work and is particularly useful when optimizing setup and hold times. Figure 31 illustrates the SYNC/SYSREF path from the master using pulser mode. Refer to 4.2 - Synchronization of outputs of a single LMK0482x device for more detail.

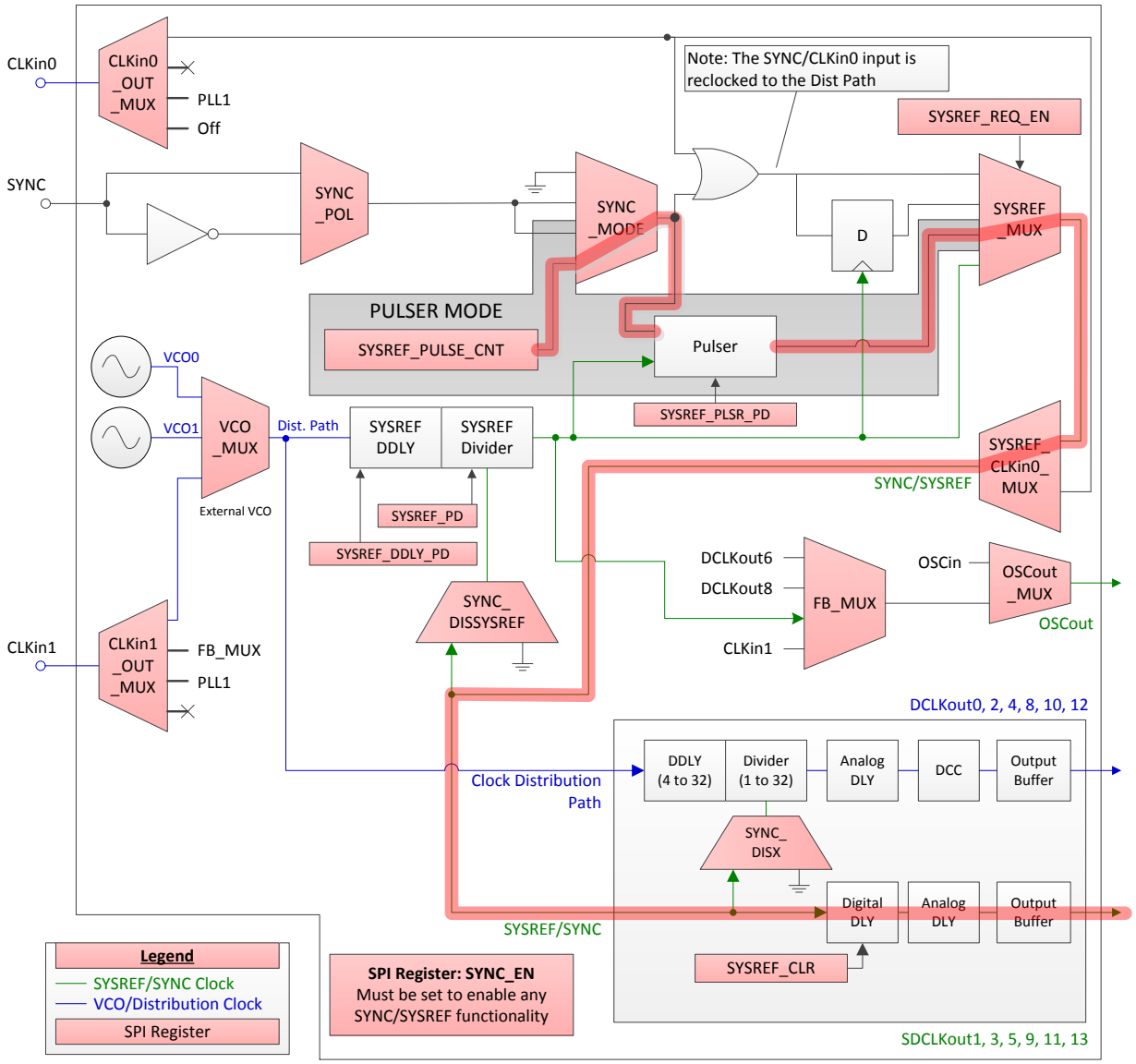

Figure 31 - Master configured to generate a SYSREF pulse

To synchronize the divides of the slave LMK0482x, the master will send one or more SYNC/SYSREF pulses, these pulse will be re-clocked by the D flip-flop clocked by the SYSREF divider. The timing of the reset of the other dividers is now deterministic with respect to the SYSREF divider edge which re-clocked the SYNC/SYSREF input on CLKin0. The phase of the DCLKoutX's with respect to the SYNC/SYSREF pulse can be adjusted as desired using the DDLY as if the SYNC occurred locally.

Only one SYNC/SYSREF pulse is required to reset all dividers on the LMK0482x. Because SYNC_1SHOT_EN is set, the dividers will SYNC with respect to the rising edge of the input. Otherwise the dividers would be held in reset while the input is high, the removal of the SYNC would then release the divides to operate. Figure 29 shows the path the external SYNC/SYSREF signal will take to reset the slave clock output dividers.

If the SDCLKouts are powered up or otherwise active, the SYNC pulses from the master which reset the slave dividers will also exit the slave device and be delivered to downstream devices. This is illustrated by the dotted red line in Figure 29.

4.5.5.4.3 Output of SYSREF

Now that the slave's dividers have been synchronized, the device is re-configured to ignore the SYNC/SYSREF path on its dividers, and just deliver the SYSREF pulses to downstream JESD204B targets.

Address	Field	Value	Definition
Synchronization and clock routing path specific registers			
R324[0,1,2, 3,4,5,6]	SYNC_DISX	1	Prevent local divider reset.
	SDCLKoutY_PD	0	Power up sysref output
	SDCLKoutY_MUX	1	Select SYSREF for SDCLKoutY
	SYSREF_GBL_PD	0	If SDCLKoutY_DIS_MODE is set to a conditional setting, setting this bit to 0 allows SYSREF to operate
	SDCLKoutY_DIS_MODE	0, 1, or 2	0 will result in SDCLKoutY always active, but setting 1 or 2 will require SYSREF_GBL_PD = 0 for output from SDCLKoutY.
	SYSREF_CLR	0	SYSREF Clear must be 0 to allow SYSREF to output. SYSREF_CLR is used in part to reset the SDCLKoutY_DDLY from producing random pulses on initial power-up.

4.5.5.5 Example

In this example two LMK0482x EVMs will be used. To simplify evaluation equipment requirements, the master will be configured in a PLL2 mode with the VCXO of the master being held at Vcc/2 by forcing holdover and using a manual DAC voltage setting. It is allowable to configure the master as dual loop and lock PLL1 if a signal generator is available.

Pulser mode will used by the master to generate the SYNC pulses to reset the slave dividers and to generate the SYSREF pulses need by the downstream JESD204B subclass 1 devices. At the end of the example, it will be illustrated how to configure continuous mode which may simplify optimizing a system for setup and hold time and also allow the user to change the slave DCLKoutX DDLY registers while immediately seeing the results (since SYNC is continuously being applied).

To use the pulser mode, the SDCLKout1 of the master and the CLKin0 of the slave EVMs must be modified as described in section 4.6 - Modify Master EVM for DC coupled SDCLKout1 operation and section 4.7 - Modify Slave EVM for DC coupled CLKin0 operation respectively.

4.5.5.5.1 Overview

The basic settings for master and slave are outlined in Table 12.

Table 12 – Case 4b Demo Configuration

Setting	Master	Slave

Default Mode	Multi SYNC Master, Reference Free, 122.88 MHz, pulser	Multi SYNC Slave – Case 4b, 0-Delay SYSREF re-clocking; Sync from Master
OSCin Frequency	122.88 MHz	122.88 MHz
VCO Frequency	2949.12 MHz	2949.12 MHz
DCLKout0	122.88 MHz (/24)	122.88 MHz (/24)
DCLKout2	122.88 MHz (/24)	245.76 MHz (/12)
SYSREF Divider Frequency	12.288 MHz (/240)	122.88 MHz (/24)
SYSREF Mode	Pulser	Re-Clocked
FORCE_HOLDOVER	1	0
MAN_DAC	512 (Vcc/2)	N/A

Figure 32 illustrates the interfacing of the master and slave devices for this example. Alternate configurations could be used as described in section 4.4 Topologies of connecting Multiple LMK0482x Devices together for improved performance.

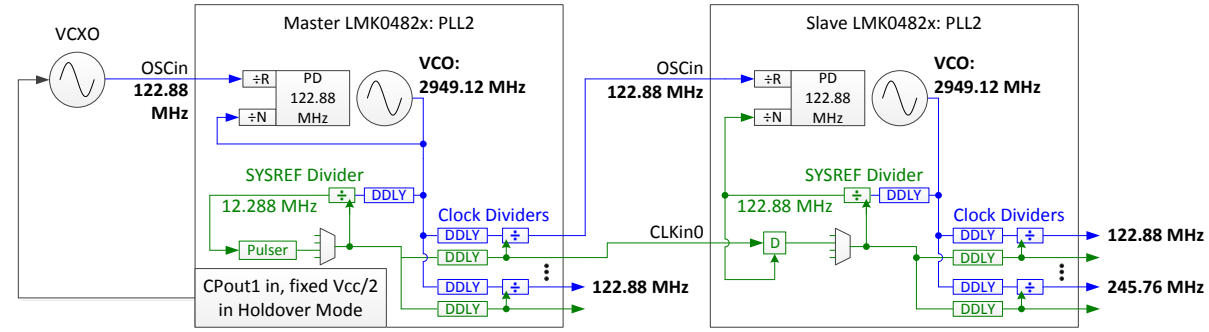

Figure 32 - Master and Slave LMK0482x. Slave case 4a to achieve synchronization with master. Optional: master uses SYSREF continuous mode

4.5.5.5.2 Modify EVMs

The master and slave EVM must be modified for DC coupled SYNC/SYSREF on SDCLKout1 and CLKin0. The slave EVM must be modified to accept external reference for PLL2 on OSCin. Refer to section APPENDIX B – Instructions for Modifying EVMs for more information on the detailed updates.

4.5.5.5.3 Connecting EVMs Together

When connecting the boards together, take care to connect same polarity inputs and outputs. Unless an extra SMA is populated on the LMK04828 Slave board, DCLKout0* (inverting) will connect to CLKin1* (inverting).

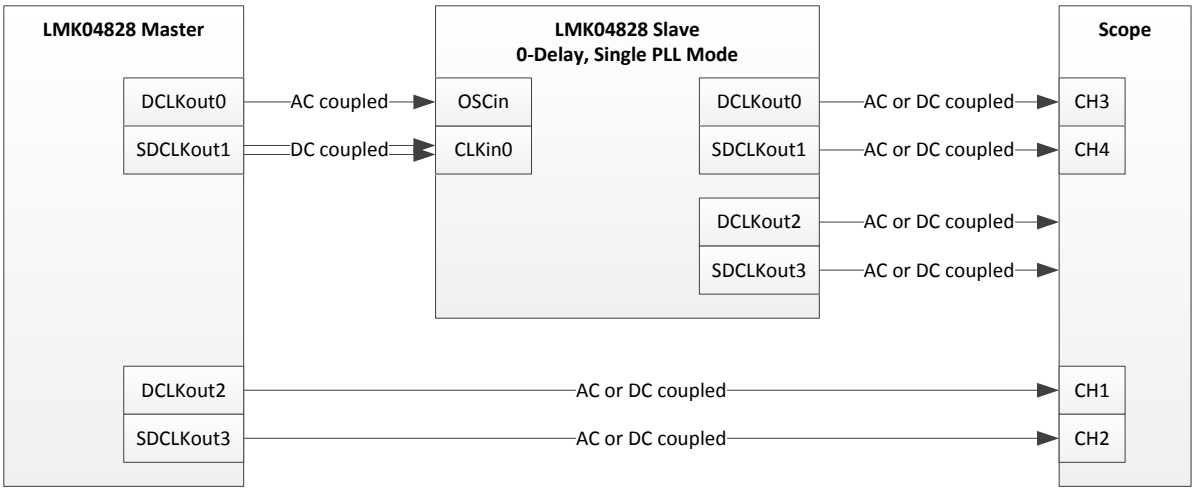

Figure 33 - Synchronization of Single PLL using 0-Delay to simplify timing

4.5.5.5.4 Software Setup

Once the EVMs are modified and the connected together, connect the USB2ANYs from the PC to the EVMs. Start two copies of TICS Pro and load the LMK04828B profile for each device. To identify which EVM is being controlled by which TICS Pro instance select "USB communications" on the menu bar, and select "Interface" to open the Communication Setup window. Click the "Identify" button to flash the green LED on the USB2ANY controlled by the specific instance of TICS Pro.

On the TICS Pro controlling the **master EVM, load and lock the PLL.**

- click "Default configurations" on the menu bar, and
- select "Multi SYNC Master, Reference Free, 122.88 MHz, pulser"
    - This will load the LMK04828B EVM to be in dual loop mode, but will force holdover with a fixed voltage on the 122.88 MHz VCXO so that PLL2 will lock to reliable reference. Frequency may not be exactly 122.88 MHz.
    - If it is desired to lock to answer external reference
        - Connect a reference at 122.88 MHz to CLKin1
        - Uncheck FORCE_HOLDOVER on the User Controls page
        - Change PLL1_LD_MUX = "PLL1 DLD" on the Status page so that Status_LD1 pin and LED reflect PLL1 DLD instead of holdover mode active.
- Click "Write All Registers" button on the toolbar or press "Ctrl-L" to program the master LMK04828.
- Then press the "SYNC Dividers" button to synchronize all the dividers of the master.
- LED Status
    - PLL1 DLD will be lit to indicate the board is in holdover mode, unless changed for PLL1 DLD as described above, if so confirmed PLL1 is locked.
    - Confirm that the PLL2 DLD LED is lit next to the VCXO.

Using TICS Pro program controlling the **slave EVM, load and lock the PLL and ready dividers for SYNC.**

- click "Default configurations" on the menu bar, and
- select "Multi SYNC Slave – Case 4b, 0-Delay SYSREF re-clocking; Sync from Master"

    - `This will load the LMK04828B EVM to have
- Click “Write All Registers” button on the toolbar or press “Ctrl-L” to program the master LMK04828.

Now using TICS Pro controlling the **master EVM, send the SYNC/SYSREF pulses.**

- On the SYSREF Page, click the “Send Pulses” button to launch a SYNC/SYSREF pulse into the slave’s CLKin0 input. This will synchronize the dividers on the slave.

Now using the TICS Pro controlling the **slave EVM, prevent SYNC/SYSREF pulses from resetting dividers.**

- On the “Set Modes” tab, click “Disable SYNC on all Dividers” button to prevent the dividers from responding to SYNC/SYSREF now that they’ve been aligned.
- Then select the desired JESD204B mode, “Continuous,” “Pulser,” or “SYSREF Request.”
    - For this example, selection “Continuous” so a continuous stream of SYSREF pulses are output which can be compared with the master.
    - However in a real application, “Pulser” would be the normal selection as it is undesirable to send continuous SYSREF pulses because of noise and power consumption.
        - In this real application, pulses would then be sent by programming SYSREF_PULSE_CNT or toggling the SYNC pin. However the device is programmed.

This concludes then necessary steps to get a system operational.

4.5.5.5.5 Further visualization, testing, and optimization

In a normal application, the system would now be operational, however to assist in visualization, on the master TICS Pro.

- set “Continuous” JESD204B mode to generate continuous SYSREF pulses which may be observed with respect to the slave.

It is also possible to observe the reset of the slave device dividers by observing the impact of reset timing on the device clocks. To do this, with the master in continuous SYSREF mode, on the slave

- On the “Set Modes” page click the “Receive SYNC/SYSREF on CLKin0” button.
    - Now the reset of the device clock maybe observed from slave device.
- On the “Clock Outputs” page uncheck
    - DDLY_PD for CLKout0
    - Change the digital delay value by adjusting the two comboboxes immediately below the DDLY_PD. Half Step may also be checked.

To determine the position in the valid window for the slave to properly receive the SYNC/SYSREF signal with respect to its device clock, on the master refer to APPENDIX C – Adjusting Timing from a Master Device for maximum setup and Hold Time.

APPENDIX A - Synchronization requirements for JESD204B

Deterministic latency is required for JESD204B subclass 1 operation. However depending upon application, the deterministic latency uncertainty may be greater than 0. Achieving deterministic latency with +/- 0 device clock error requires the SYSREF to always meet the setup and hold time of the target device with respect to the device clock. However in some applications, it may be allowable to tolerate +/- 1, or +/- n device clock cycles of deterministic latency uncertainty. This is more likely to occur for system with high device clock frequencies like 3 GHz. Some applications can even detect and correct for this small, +/- n device clock cycle uncertainty.

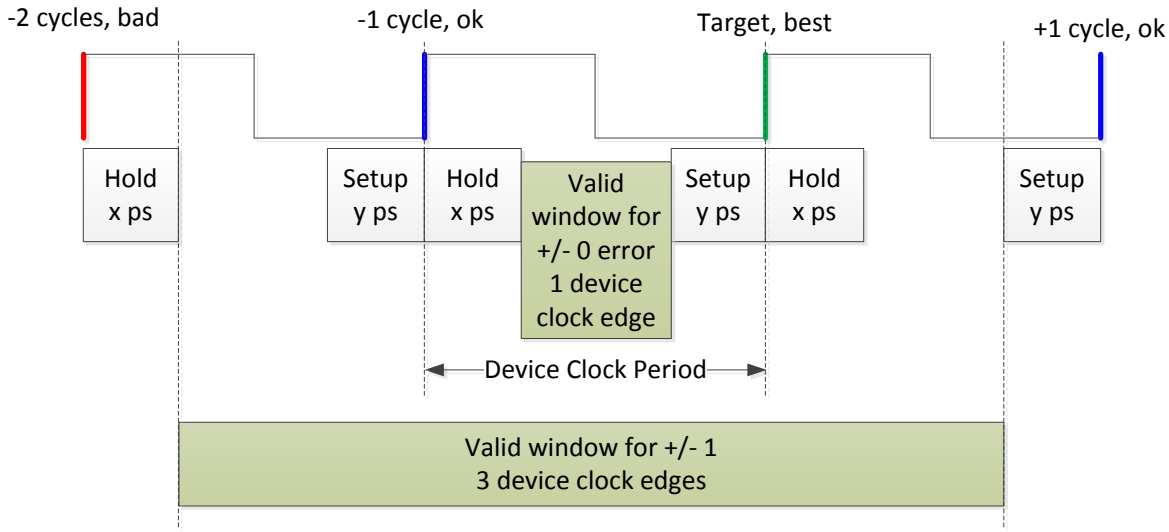

Figure 34 - Comparison of valid window for application which demands +/- 0 device clock cycle alignment vs. one which can tolerate +/- 1 device clock cycle. > 300% increase in valid window.

APPENDIX B – Instructions for Modifying EVMs

In the examples given above, the master and slave EVMs must be modified to allow SYSREF to operate as a DC signal. When single loop operation is called for, modifications to the EVM are required to connect OSCin to an external signal. The sections below outline possible modification of boards.

4.6 Modify Master EVM for DC coupled SDCLKout1 operation

By default the LMK0482x evaluation board outputs are AC coupled to protect test equipment from DC voltages, but to demonstrate the ability of a single pulse to reset dividers in the distribution device, the master LMK0482x board should be setup for HSDS 8 mA DC coupled operation. HSDS 8 mA output should have the emitter resistors R104 and R112 removed. Replace 0.1 uF capacitors C48 and C52 with 0603 0 ohm resistors. These components are circled below in Figure 35.

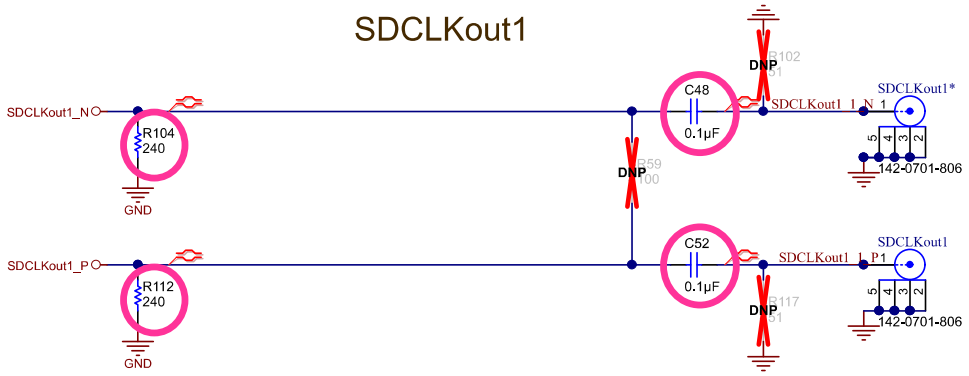

Figure 35 - Preparing LMK0482x for use with DC coupled SYNC/SYSREF output as HSDS 8 mA

The same adjustment for output format/AC or DC coupling may be made to any of the DCLKoutX/SDCLKoutY outputs as desired. **But do not connect signals with > 0 V DC to sensitive RF test equipment!**

4.7 Modify Slave EVM for DC coupled CLKin0 operation

To prepare the evaluation boards for use with this example, the LMK0482x slave must have the CLKin0 path set for DC coupled input to demonstrate the ability of a single pulse to reset dividers. For a DC coupled CLKin0, replace 0.1 uF capacitors C2 and C6 circled below in Figure 36 with 0603 0 ohm resistors. The CLKinX inputs of LMK04828 are able to be driven differentially by DC coupled HSDS 8 mA.

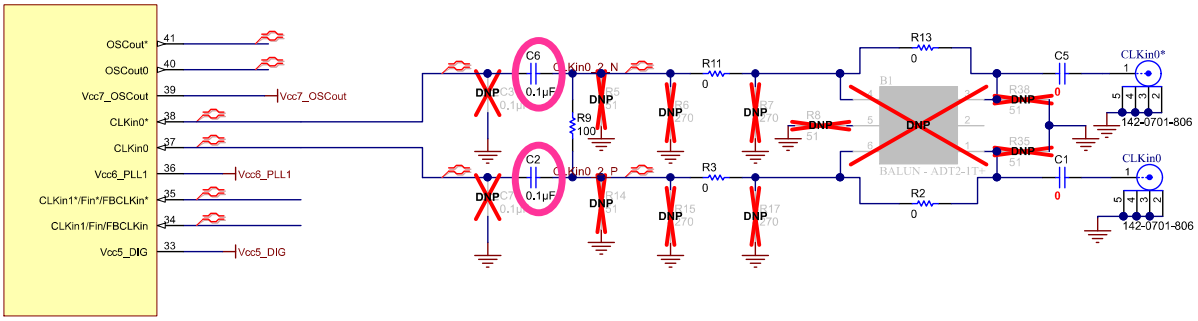

Figure 36 - Preparing LMK0482x for use with DC coupled SYNC/SYSREF input to CLKin0

4.8 Modify EVM for Single Loop Operation

For single loop operation, connect OSCin SMAs for external signal, set termination as needed, and remove power from VCXO.

Use OSCin or OSCin* as desired. OSCin* is used with single ended VCXO to allow footprint compatibility with differential VCXOs. Since this is the inverting input, when connecting single ended to a master device, use it's inverting output.

Optionally, the extra updates to use OSCin path instead of OSCin* could be performed. Or to use OSCin differentially.

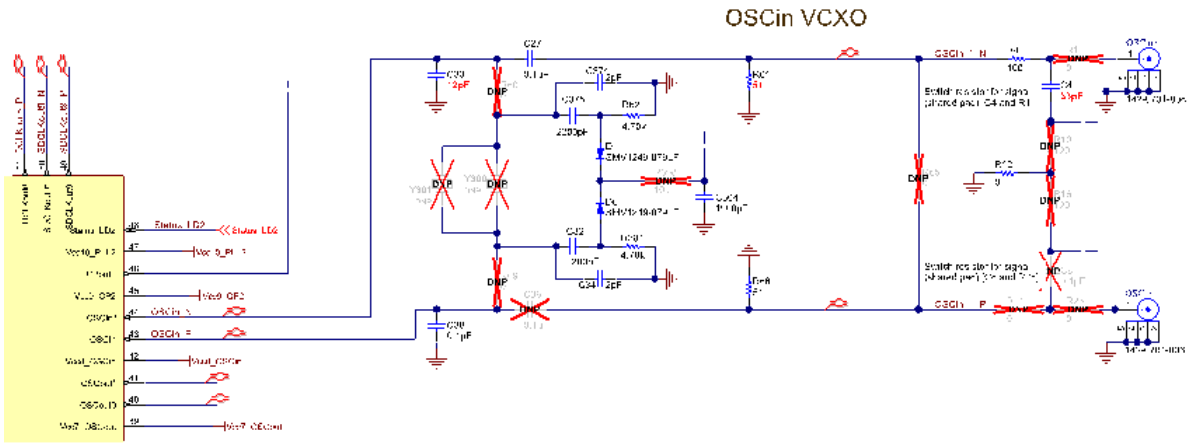

Figure 37 - OSCin input schematic

Table 13 - Modifications for single ended input on OSCin*

Designator	EVM Default	Single Loop Operation
C33	12 pF (filter for 122.88 MHz)	Optional
R61	51 ohm (termination and voltage division for single ended input)	51 ohms
R4	100 ohm (for voltage division from 3.3 V source)	As desired for voltage division with 51 ohms. Single ended 2.4 Vpp maximum spec on OSCin*
C4 (shared pad with R1)	33 pF (filter for 122.88 MHz, AC coupling to input voltage divider, no DC low impedance path to ground)	Removed
R1 (shared pad with C4)	Open	Place with 0 ohm or cap to connect OSCin to input. Using a capacitor prevents a DC low impedance path to ground.
R19	0 ohms (provide power to VCXO)	Open (remove power from VCXO)

APPENDIX C – Adjusting Timing from a Master Device for maximum setup and Hold Time

Change the digital delay for SDCLKout1 by adjusting the combobox in the digital delay column in-line with the SDCLKout1 output. Changing this digital delay will move the position of SYSREF with respect to the device clock, the half step bit may also be used. The number of digital delay settings for which the phase of the device clock divider remains the same illustrates the actual valid window for the device. If a jump in phase is observed moving from a to b, and from c to d. Then the optimal setting will be half-way between setting b and c.