DP8570A Timer Clock Peripheral Test Mode and Test Considerations

National Semiconductor
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Primarily the test mode is used by National Semiconductor to ease the testing of device at manufacture. However, some users may wish to implement testing of devices prior to being used in designs. The purpose of this application note is to give the user insight into what is involved when testing the DP8570A Timer Clock Peripheral (TCP). The complete range of test mode features is presented here along with notes on how to use them. General testing guidelines are also given which should help the user to avoid some of the pitfalls at the design-in stage.

INTRODUCTION

The real-time clock section of the DP8570A is a series of cascaded registers. To test the correct roll-over of each register in this configuration would take a very long time. For example, if clocked in real-time (100 Hz), testing would take 100 years to complete, obviously this is unacceptable.

Similar problems exist when testing the timers. Each timer is 16 bits wide. If it were to be tested in normal operation, 65536 (2^{16}) pulses are required to produce a cycle in the 16th bit in the chain. This will result in an intolerable increase of testing time.

There are further test considerations with the timer prescaler section of the device. These sections contain frequency divider circuits. The easiest way to test these dividers is to measure the frequency of the output and relate it to the frequency of the input. However, with some standard production machines it is difficult to measure frequency. Therefore it will be difficult to check the various outputs of the timer prescaler.

The actual method of testing these prescalers is to apply a set number of pulses to the input of the divider and monitor the output for a change of state. For example, to test the divide by 32000 counter, that number of pulses would have to be applied to produce an output pulse. If the normal timer prescaler configuration is used it will take one full second waiting for the divide by 32000 counter to cycle.

TEST MODE FEATURES

To overcome testing difficulties of the types discussed a test configuration has been designed into the device, which can be implemented via software. Due to the complex nature of the TCP a complete register is required to control the various test functions. This register is situated at RAM location 1F (hex) on page 0 (see datasheet for details of addressing).

The byte associated with this address is normally a general purpose RAM location. When in test mode, the register can be programmed to implement various test configurations. To enable these functions the test mode enable bit (D7) in the Periodic Flag Register (PFR) must be programmed high. For normal operation this bit must be programmed low. The Test Mode Register configuration is shown in *Figure 1*.

D7	D6	D5	D4	D3	D2	D1	D0
OSF DISABLE	CRB1	CRB0	SRB1	SRB0	EMC	CTR TEST	DIR CLOCK

FIGURE 1. Test Mode Register

The functions of the various bits in the test mode register are outlined below. Bits D0,D1 are for the real time and associated sections, while bits D2 to D6 are dedicated for timer use. D7 is for general use.

DIR CLOCK: This is the Direct Clock bit. When programmed high, the oscillator dividers (32 kHz and 1 kHz) and the pulse subtractor in the clock prescaler are bypassed. Thus the counters in the real-time section may be clocked directly from a signal presented to the OSC IN pin. To implement the by-pass correctly, the frequency select bits D6,D7 in the Real-Time Mode Register, must be programmed such that the 4 MHz and 5 MHz divider chains are also disabled (see *Figure 2*). The correct programming for this is D6,D7 = 0 or D6,D7 = 1.

The 4 MHz and 5 MHz dividers can be tested in isolation using the following:

DIR CLOCK = 1 and D6 = 1 for 4 MHz,
DIR CLOCK = 1 and D7 = 1 for 5 MHz.

The output of these dividers will then be connected directly to the 1/100 second counter.

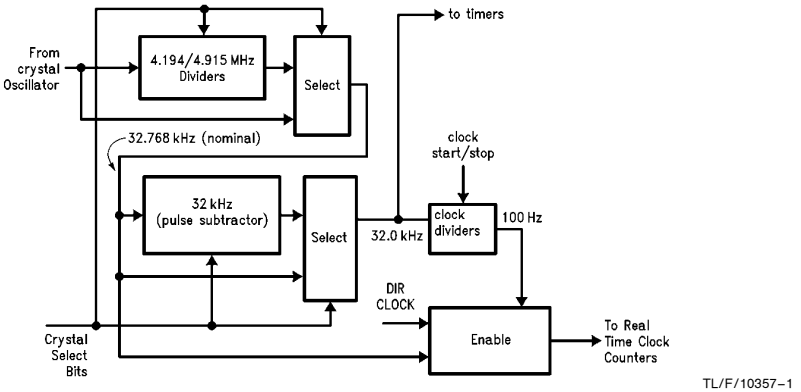

FIGURE 2. Clock Prescaler (with Test Bit)

CTR TEST: This is the Counter Test bit. When programmed high this bit re-configures the real-time counters into the test mode configuration (see *Figure 3*). These counters can then be clocked in parallel thus reducing the test time.

Note that the normal maximum operating frequency of these counters is 100 Hz and the low frequency oscillator is designed to work at approximately 32 kHz. Therefore if fast clocking via the OSC IN pin is attempted serious signal degradation will occur, making testing impossible. For these reasons it is recommended that for a $V_{BB} = 3V$, a maximum clock rate of 200 kHz (2.5 μs pulse width) is used on all tests where the OSC IN pin provides the clock source. When testing the device using clock bursting, the clock must be a return-to-one signal. It is not recommended that the OSC OUT pin be used as a clock source, and must not be connected.

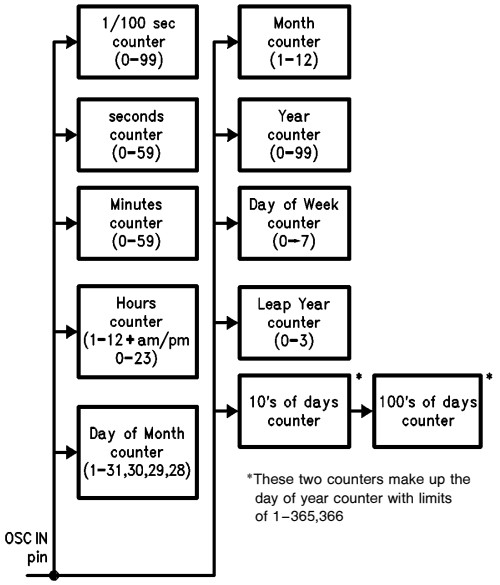

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FIGURE 3. Real Time Counters, Test Mode Configuration

EMC: This is the Enable MSB Clock bit. When programmed high it enables the most significant bytes (MSBs) of both 16-bit counters to be clocked directly. Note that the LSB's of the counters must contain 00(hex) for this to be accomplished correctly. This allows the timers to be tested in two halves, which will give a total of $2 \times (2^8)$ possible states instead of 2^{16} significantly reducing the test time.

SRB0: This is the Signal Route Bit for timer 0 prescaler. When programmed high this bit routes the selected clock to the timer 0 output.

SRB1: This is the Signal Route Bit for timer 1 prescaler. When programmed high this bit routes the selected clock to the timer 1 output.

The inclusion of the ''SRB'' bits means that a more modular approach to timer testing is achieved because the timer prescalers can be tested in isolation.

The clock select bits in the Timer Control Register are used to route the required clock to the multiplexer output ''selected clock'', of the prescaler, see *Figure 4*. Note that timer 0 output is accessed using the Multifunction Output (MFO) pin, see datasheet for details. However, timer 1 output can be accessed directly using the Timer 1 Output (T1) pin.

CRB0: This is the Crystal Route Bit for timer 0 prescaler. When programmed high this bit routes the external crystal frequency to the dividing counters in timer 0 prescaler which are normally driven by the internal 32.0 kHz signal. See *Figure 2*.

CRB1: This is the Crystal Route Bit for timer 1 prescaler. When programmed high, this bit routes the external crystal frequency to the dividing counters in timer 1 prescaler which are normally driven by the internal 32.0 kHz signal.

The ''CRB'' bits allow all the timer prescaler dividers to be clocked directly from the OSC IN pin. This allows fast clocking of these circuits plus allowing a known number of pulses to be input. Note that the frequency select bits in the Real Time Mode register need to be programmed correctly for this section as well (D6,D7 = 0).

OSF DISABLE: This is the OSC Fail Disable bit. When programmed high this bit causes the OSC FAIL detect circuitry in the clock prescaler to be disabled.

One of the features of the DP8570A is its ability to detect when an oscillator fail has occurred. Oscillator failure is indicated by reading bit D6 in the Periodic Flag Register. When an oscillator fail is detected four functions are performed.

1. The OSC fail flag is set.
2. The clock start/stop bit (CSS) in the Real Time Mode register is reset, preserving the time that the oscillator stopped.
3. Overrides the lockout circuitry ensuring that the processor interface is not locked out when an oscillator fail has occurred.
4. Presets battery bit (D6) in PFR (selects the single power supply mode).

Under test conditions a crystal cannot be used because there is no control over its output. A pulse generator must be used to clock the device in a controlled manner. Obviously, under these single-step conditions the oscillator fail circuitry will detect a lack of oscillation and perform the functions mentioned. Therefore for certain tests it will be necessary to disable the effect of OSC fail (where CSS must remain active for example), this is accomplished using the OSC Fail Disable bit.

To get access to the OSF Disable bit, the test mode enable bit (D7 in the PFR) must be written high first. The order is important. The OSF Disable bit must also be programmed back to zero when testing is complete. This is to avoid drawing excess current in standby mode. When initial power is applied, this bit has been designed to power-up in the inactive state, ensuring that the TCP will not enter a state of permanent lockout when power is applied.

The implications of function 4 are also important when considering the fact that a pulse generator is used to provide the clock source. The amplitude of the output signal should be equal to the power supply of the oscillator (V_{OSC}).

In battery backed mode	$V_{OSC} = V_{BB}$
In single power supply mode	$V_{OSC} = V_{CC}$

When testing the device in battery backed mode, and using single pulses, the following steps are necessary to ensure that the device is in the correct mode.

MSR	00	RS = 0
PFR	80	Test Mode Enable
TST	80	OSC Fail Disable Bit
PFR	80	Battery Bit and Test Mode

The reason the PFR has to be written twice is that the OSC FAIL signal will preset the single supply bit (D6) and has to be disabled before D6 can be written to.

Read/Write Considerations

In the DP8570 the bits in the address space consist not only of normal read/write bits but also flags, read-reset flags, write-1 reset flags and a dual function bit. The user should be aware of these when attempting to read/write to the device.

Read/Write Bits

MSR	D6,D7 Only
TCR0, TCR1	D0–D7
PFR	D7 Only
IRR	D0–D5, D7
RTMR	D0–D7

(Bit D3 will remain at 0 unless in test mode or the oscillator is running)

OMR	D0–D7
ICR0, ICR1	D0–D7
1/100 sec	D0–D7
SECONDS	D0–D6 (D7 Always 0)
MINUTES	D0–D6 (D7 Always 0)
HOURS 24 hr	D0–D5 (D6,D7 Always 0)
HOURS 12 hr	D0–D4

(D5,D6 Always 0, D7 = am/pm Bit)

DAY of MONTH	D0–D5 (D6, D7 Always 0)
MONTH	D0–D4 (D5–D7 Always 0)
YEAR	D0–D7
DAY of YEAR	D0–D7
100's DOY	D0, D1 (D2–D7 Always 0)
DAY of WEEK	D0–D2 (D3–D7 Always 0)

The rest of the address locations are all read/write but certain precautions need to be observed to get a correct response. It is recommended that the control section is reset to all zeros before attempting to write to the rest of page 0 locations.

Flags

The flags are read only and are set and reset by events inside the device. They are situated at the following locations.

Batt Low Flag	D6 of IRR
Power Fail Flag	D1 of MSR
Interrupt Status Flag	D0 of MSR
Dual Function	D6 of PFR

When READ, D6 of the PFR will give the contents of the OSC FAIL flag. When WRITTEN, D6 sets up the power supply mode of the DP8570A. Writing a ''1'' selects single power supply mode, writing a ''0'' selects the battery backed mode.

The implications of this are quite important because there is no direct way the user can tell which power supply mode is selected. The only way of determining the mode is by monitoring the OSC OUT pin. The amplitude of this signal will be approximately equal to the value of V_{OSC}.

In battery backed mode the amplitude will be V_{BB}, in single supply mode the amplitude will be V_{CC}. Most of the time, the OSC OUT pin may be measured using a 10 MΩ, 10 pF probe. However, when the high frequency oscillator, the oscillator may stop. For this case a higher impedance, lower capacitance probe may be needed.

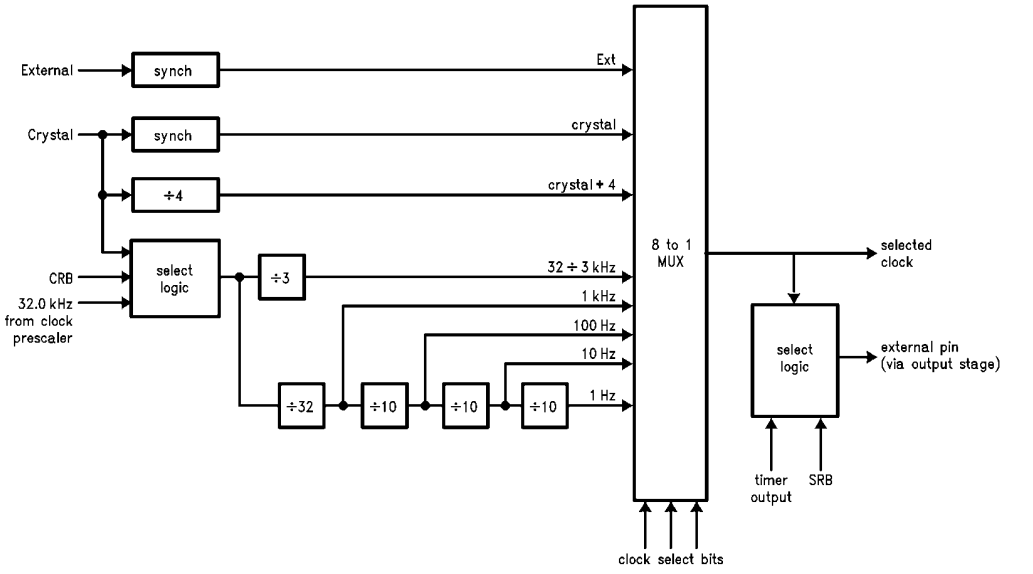

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FIGURE 4. Timer Prescaler (with test bits)

The only way of determining the mode is by monitoring the OSC OUT pin. The amplitude of this signal will be approximately equal to the value of V_{OSC}.

In battery backed mode the amplitude will be V_{BB}, in single supply mode it will be V_{CC}. This technique is helpful when using either a pulse generator or crystal as the clock source. However, care should be taken if probing OSC OUT when a crystal is used, as the probe capacitance could stop the oscillation. As a minimum, a 10 Meg, 10 pF probe is recommended.

The read-reset flags are situated at D0–D5 of the PFR and are read only. Internal events inside the device set the flags and they are reset when read.

The write-1 reset flags are situated at D2–D5 of the MSR. They can be read as a 1 or 0, and are set by internal events inside the device. Writing a 0 to these bits will have no effect. Writing a 1 will reset these flags.

CONCLUSION

The purpose of this note is to provide some insight into the complexities of testing the DP8570A. It shows how various tests can be carried out efficiently by designing testability into a device. The actual testing implemented by the user can be simple or comprehensive and only those features required need be utilized.

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