Texas Instruments Incorporated
Military Products Department
Military High Reliability Integrated Circuits
Processing Conformance Report

Device Type: **5962-1620701VXC**
SMD: **5962-1620701VXC**
Processing Type: **CLASS V**

PCR Lot Number: **4000308MTT**
Device Description: **QMLV CDCLVP111 DEVCIE SETUP**

Assembly Location: **MMT** Assembly Date Code Year: **2023** Week: **29** Lot Window: **A**
Wafer Lot #: **6026947**
Wafer #: **01** Wafer Lot Date Code Year: **2016** Qtr: **2Q** Die Rev: **A** W/F Code: **R**

Integrated Circuits referenced above have received the following processing per recorded lot history.

SCREEN	METHOD	(MIL-STD-883)	
✓ INTERNAL VISUAL PRECAP	2010	CONDITION A (100X)	
✓ INTERNAL VISUAL PRECAP	2010	CONDITION A (40X)	
✓ INTERNAL VISUAL PRECAP	2010	CONDITION A (L/A)	
Wafer Number(s) used in Production:	**01**		
✓ TEMPERATURE CYCLING	1010	CONDITION C	
✓ CENTRIFUGE	2001	CONDITION E,Y1 PLANE	
✓ PIND TEST	2020	CONDITION A	
✓ RADIOGRAPHY	2012	☐ MONITOR OR ✓ 100%	
✓ INTERIM ELECTRICAL TEST		25c DC / FUNCTIONAL	
✓ BURN IN	1015	TEMP (°C): **125c** PDA 1: **0.00%**	TIME (Hrs): **240** PDA 2: **N/A**

FINAL ELECTRICAL TEST TEMP	✓ 25c ✓ 125c ✓ -55c ☐ **N/A**	☐ **N/A**	
TEST PROGRAM #(s)	**I30521/04**	**I30521/04**	**I30521/04**

✓ HERMETICITY	1014	
FINE LEAK		CONDITION A OR B
GROSS LEAK		CONDITION C
✓ EXTERNAL VISUAL	2009	(100%)
✓ EXTERNAL VISUAL	2009	(L/A)

QUALITY CONFORMANCE ATTRIBUTE DATA GROUP "A " SUMMARY

SUBGROUP	TEST & TEMP	SAMPLE SIZE
✓ A-1/4/7	DC ELECTRICAL - AMBIENT	116 OR 100%
✓ A-2/5/8	DC ELECTRICAL - MAXIMUM	116 OR 100%
✓ A-3/6/8	DC ELECTRICAL - MINIMUM	116 OR 100%
✓ A-9	AC ELECTRICAL - AMBIENT	116 OR 100%
✓ A-10	AC ELECTRICAL - MAXIMUM	116 OR 100%
✓ A-11	AC ELECTRICAL - MINIMUM	116 OR 100%

Device Lead-Finish complies with MIL-PRF-38535 A.3.5.6.3 Microcircuit finishes: "Finishes of all external leads or terminals and all external package elements shall conform to either A.3.5.6.3.2 or A.3.5.6.3.3 as applicable. The use of pure tin, as an underplate or final finish, is prohibited both internally and externally. The tin content of solder shall not exceed 97 percent. Tin shall be alloyed with a minimum of 3 percent lead by weight.

SOLDER PROCESSING DATE (IF APPLICABLE): **N/A**
NOTE: The following documents MUST be pulled and sent with each lot.
(A copy to be placed in each box)
1) PROCESS CONFORMANCE REPORT
2) GENERIC GROUP B QCI SUMMARY REPORT
3) GENERIC GROUP D QCI SUMMARY REPORT
4) WAFER LOT ACCEPTANCE REPORT FOR THE WAFER LOT USED IN THIS ASSEMBLY LOT.

Prepared By: **Nattapapat Laokham** Date: **02/12/2024**

QCI Group B - Lot #: **4000308**	Date Code: **2329A**	Pkg Type: **36HFG**	Lead Finish: **A**
QCI Group C - Lot #: **6118898**	Date Code: **1627A**	MCG: **140**	Wafer Lot Date Code: **6B**
QCI Group D - Lot #: **2014254**	Date Code: **2250B**	Pkg Type: **36HFG**	Lead Finish: **A**
QCI Group D6 - Lot #: **3011447**	Date Code: **2326A**	Pkg Type: **36HFG**	Lead Finish: **A**
QCI Group E - Lot #:	Wafer Lot #:	Parent Wafer Lot #:	
QCI Group P - Lot #:	Date Code:	Pkg Type:	Lead Finish:
Wafer Lot Accept - Lot #: **6118898**	Wafer Lot #: **6026947**		

Group B Summary Report

Lot Number: 4000308
Device Name: 5962-1620701VXC
Date Code: 2023-29-A
Assembly Site: MMT
Test Start: 02/13/2024
Test Complete: 02/13/2024
Lead Finish: A
Pin: 36
Package: HFG
Package Family: GROUP 9J

Sub-Group	Test	Method	Sample Size	Rejects / Data	Notes
B1	Resistance To Solvents	TM2015	3	0	1
B2	Bond Strength	TM2011	22	0	2
B2	Die Attach Strength	TM2019 OR TM2027	3	0	
B3	Solderability	TM2003	22	0	3
B4	Ball Shear Test For Bga	JESD22-B117	45	NA	4
B4	Solder Column Pull Test Cga Pa	TM2038	45	NA	5

Notes: 1. Resistance to solvents testing required only on devices using inks or paints as a marking medium.
2. 22 wires / 4 units minimum.
3. 22 leads / 3 packages minimum. Not required for solder columns. Solder temperature +245C +/- 5C.
4. 45 balls from 2 devices minimum. Not required for qualification or quality conformance inspections where group D inspection is being performed on samples from the same inspection lot. For devices with solder terminations, Physical dimension test shall be performed with balls/columns.
5. 45 columns from 2 devices minimum.

Comments:

Prepared By: Nattapapat Laokham
Prepared By Email: x1112274@ti.com
Prepare Date: 02/12/2024

Group C Summary Report

Lot Number:	6118898	Device Name:	CDCLVP111-SP	Assembly Site:	MMT
Lot Date Code:	2016-27-A	Wafer Lot Date Code:	2016-2Q-A-R	Wafer Lot Number:	6026947
Parent Die:	RCDCLVP111A0VE	Die Attach:	QMI	Window:	2Q 2016 to 1Q 2017
Pin:	36	Package:	HFG	MCG:	140
Test Start:	08/08/2016	Test Complete:	09/21/2016		

Sub-Group	Test	Method	Sample Size	Rejects / Data	Notes
C1	Steady-state life test	1005		0	1
C1	Endpoint Electrical Test		45	0	2

Notes: 1. 1,000 hours/125C or equivalent. (If greater than 1,000 hours/125C enter actual conditions into comments below)
2. Endpoint electrical testing in accordance with device test specification.

Comments:
50/0 TESTED

Prepared By:	Jie Xia	Prepared By Email:	jxia@ti.com	Prepare Date:	11/07/2016

Group D Summary Report

Lot Number: 2014254
Device Name: 5962R1022101VSC
Date Code: 2022-50-B
Assembly Site: MMT
Test Start: 02/10/2023
Test Complete: 02/24/2023
Lead Finish: A
Pin: 20
Package: HKH
Package Family: GROUP 9Q9
Window: 50 2022 to 23 2023

Sub-Group	Test	Method	Sample Size	Rejects / Data	Notes
D1	Physical Dimensions	2016	15	0	
D2	Lead / Terminal Integrity Test	2004	45	0	Condition B2
D2	Seal (Fine and Gross leak)	1014	45	0	
D3	Thermal Shock	1011	15	0	Condition B, 15 cycles
D3	Temperature Cycling	1010	15	0	Condition C, 100 cycles
D3	Moisture Resistance	1004	15	0	
D3	Visual Examination	1001 or 1010	15	0	
D3	Seal (Fine and Gross leak)	1014	15	0	
D3	End-point electrical parameters	Data sheet / SMD / JAN Slash-sheet	15	0	
D4	Mechanical Shock	2002	15	0	Condition B
D4	Vibration, Variable Frequency	2007	15	0	Condition A
D4	Constant Acceleration	2001	15	0	Condition E, Y1 orientation only
D4	Seal (Fine and Gross leak)	1014	15	0	
D4	Visual Examination	2007	15	0	
D4	End point electrical test	Data sheet / SMD / JAN Slash-sheet	15	0	
D5	Salt Atmosphere	1009	15	0	Condition A
D5	Visual Examination	1009	15	0	
D5	Seal (Fine and Gross leak)	1014	15	0	
D7	Adhesion of Lead Finish	2025	15	0	
D8	Lid Torque	2024	5	0	
D9	Soldering Heat	2036			Stress during assembly
D9	Seal (Fine and Gross leak)	1014			Stress during assembly
D9	External Visual Inspection	2009			Stress during assembly
D9	End-point electrical test	Data sheet / SMD / JAN Slash-sheet			Stress during assembly

Notes:

Comments:

Prepared By: Sungvorn Muang-len
Prepared By Email: x1126167@ti.com
Prepare Date: 04/09/2025

Group D6 Summary Report

Lot Number:	3011447	Device Name:	5962-1620701VXC		
Date Code:	2023-26-A	Assembly Site:	MMT		
Test Start:	12/15/2023	Test Complete:	01/12/2024	Lead Finish:	A
Pin:	36	Package:	HFG	Package Family:	GROUP 9J
Window:	26 2023 to 09 2024				

Comments:

Prepared By:	Watchara Thongnawakoon	Prepared By Email:	x0245876@ti.com	Prepare Date:	12/21/2023

WLA Summary Report

Lot Number: 6118898 Device Name: CDCLVP111-SP
Wafer Lot Date Code: 2016-2Q-A-R Wafer Lot Number: 6026947
Parent Die: RCDCLVP1110VE Lead Finish: C MCG: 140
Test Start: 09/21/2016 Test Complete: 09/21/2016

Sub-Group	Test	Method	Sample Size	Rejects / Data	Notes
WLA-1	Wafer Thickness	5007	2 wafers/lot	0	1
WLA-2	Metallization Thickness	5007	1 wafer/lot	0	2
WLA-3	Thermal Stablility	5007	1 wafer/lot	0	2,3
WLA-4	SEM Inspection Lot Acceptance	2018	2 wafers/lot	0	2
WLA-4	Lab Performing Analysis:			TI	
WLA-5	Glassivation Thickness	5007	1 wafer/lot	0	2
WLA-6	Gold Backing Thickness	5007	1 wafer/lot	0	2,4
WLA-7	Steady-state life test	1005		0	5
WLA-7	Endpoint Electrical Test	1005	45	0	6

Notes: 1. This test is not required when the finished wafer design thickness is greater than 10 mils before backgrind.
2. In-line monitor data for this wafer lot may be used.
3. Applicable to all linear, all MOS, all bipolar digital operating at 10V or more. (VFB/VT/C-V)
4. Gold backed wafers only.
5. 1,000 hours/125C or equivalent
6. Endpoint electrical testing in accordance with device test specification

Comments:

Prepared By: Vut Kangkamanee Prepared By Email: x0194988@ti.com Prepare Date: 12/23/2016