

Select Device Filter Designer Phase Noise Spurs Lock Time Bode Plot

LMX2581 Design Tips

Filter Architecture
Filter Order: 4th Order Filter Type: Passive

Filter Parameters
Recommend Fpd and Kpd Calculate Loop Filter

Design Target Actual
Loop Bandwidth: 17.41978 kHz 24.829315 kHz
Phase Margin: 45 deg 51.4258 deg

Gamma: 1.255943 3.5844
T3/T1 Ratio: 1.451945 % 0.1644 %
T4/T3 Ratio: 6.207647 % 7.6785 %
Min. High Order Cap: 3300 pF 2200 pF
Capacitor Value Step: 10% Resistor Value Step: 10%
Simulation Shown: Phase Noise Gain Margin: 58.1 dB

Forced Component Values
C1: nF C2: nF R2: kΩ
C3: nF R3: kΩ
C4: nF R4: kΩ

Performance Summary
Setup Conditions on Phase Noise, Spur, and Lock Time Tabs
Optimize: Phase Noise at MKR1 (dBc/Hz)

Parameter	Achieved
Phase Noise at MKR1 (dBc/Hz)	-92
Phase Noise at MKR2 (dBc/Hz)	-95.8
Phase Noise at MKR3 (dBc/Hz)	-87.8
Phase Noise at MKR4 (dBc/Hz)	0
Phase Noise at MKR5 (dBc/Hz)	0

Recommend Fpd, Kpd, and Auto Checkbox Setup
Strategy: C2max Balance for Spurs FpdMin: 20 MHz

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LMX2581 Phase Noise Tips

Graph Settings
Points: 101 Autoscale Axes
X Axis: 0.0001 100 MHz
Y Axis: -200 -70 dBc/Hz
Load Comparison Trace

Total Phase Noise at Offsets

Offset (kHz)	Noise (dBc/Hz)
MKR1: 0.1	-71.6
MKR2: 1	-96.1
MKR3: 10	-94.3
MKR4: 100	-114.4
MKR5: 1000	-140.4
MKR6: 10000	-151

Crossover Metrics
InBand to VCO: 136.972 kHz
PLL 1/f to Floor: 79.283 kHz
VCO 1/f^3 to 1/f^2: 363.078 kHz
VCO 1/f^2 to Floor: 7.762 MHz

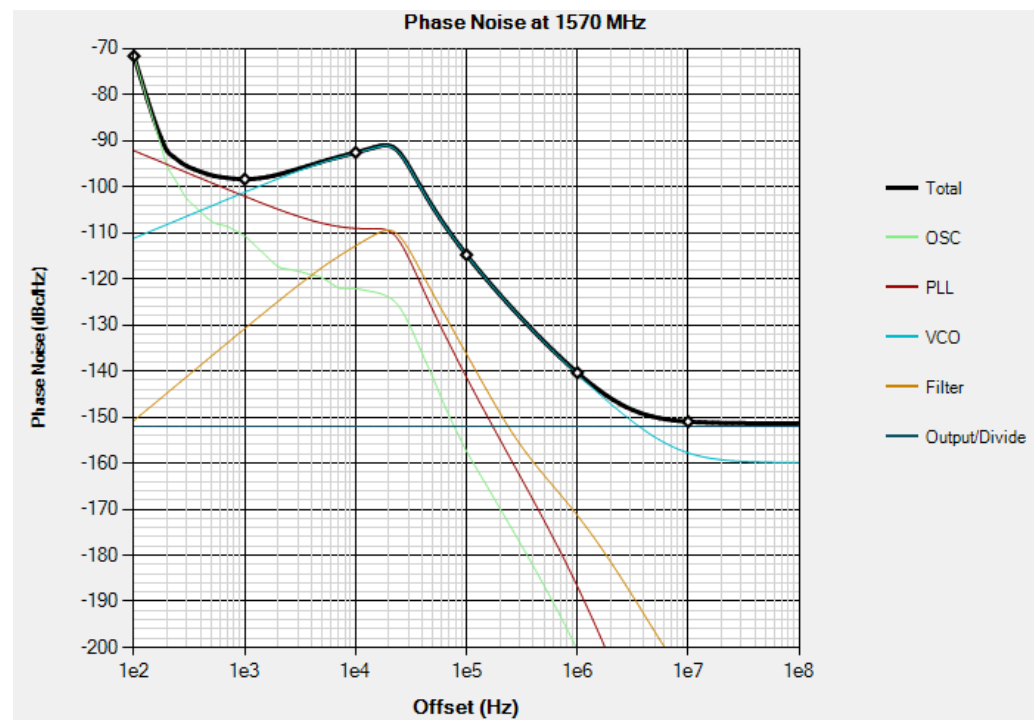
Integrated Noise
Lower Limit: 1 kHz
Upper Limit: 2 MHz
RMS Jitter: 505 fs
Other Integrated Noise Metrics: Add Spurs to Integrated Noise
RMS Phase Error: 0.285 deg
EVM: .497 %
Integrated Noise: 2.482e-5
SNR: -46.1 dBc/Hz
Avg Noise Floor: -112.1 dBc/Hz

Other Noise Sources
Enable Loop Filter Noise
Enable Output/Divider Noise: -152 dBc/Hz

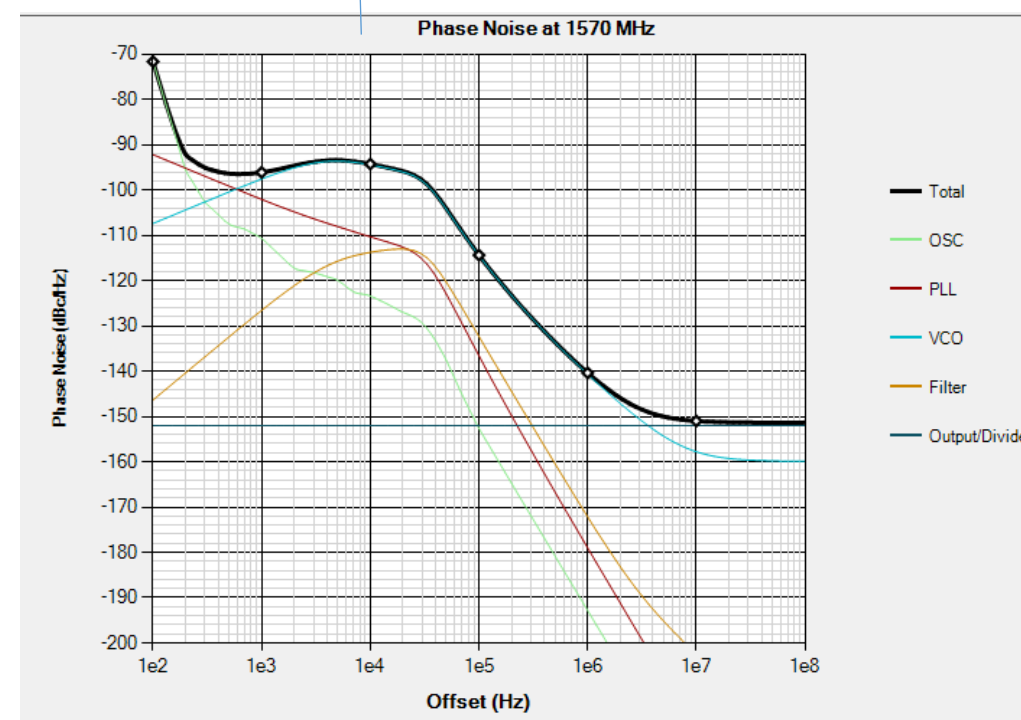
OSC, PLL, and VCO Noise
Input Source (OSC) Noise: Disable
VCO Noise: Use Metrics
PLL Noise: Use Metrics

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Not the same value?



Automatic adjustment



Manual adjustment