

POWER TERMINALS

DUAL 1-A LDO REG (LDO1, LDO2) for DUT VDD & VDDO rails

LDO1 OUT: 3.3 V

LDO2 OUT: 1.8, 2.5, or 3.3 V

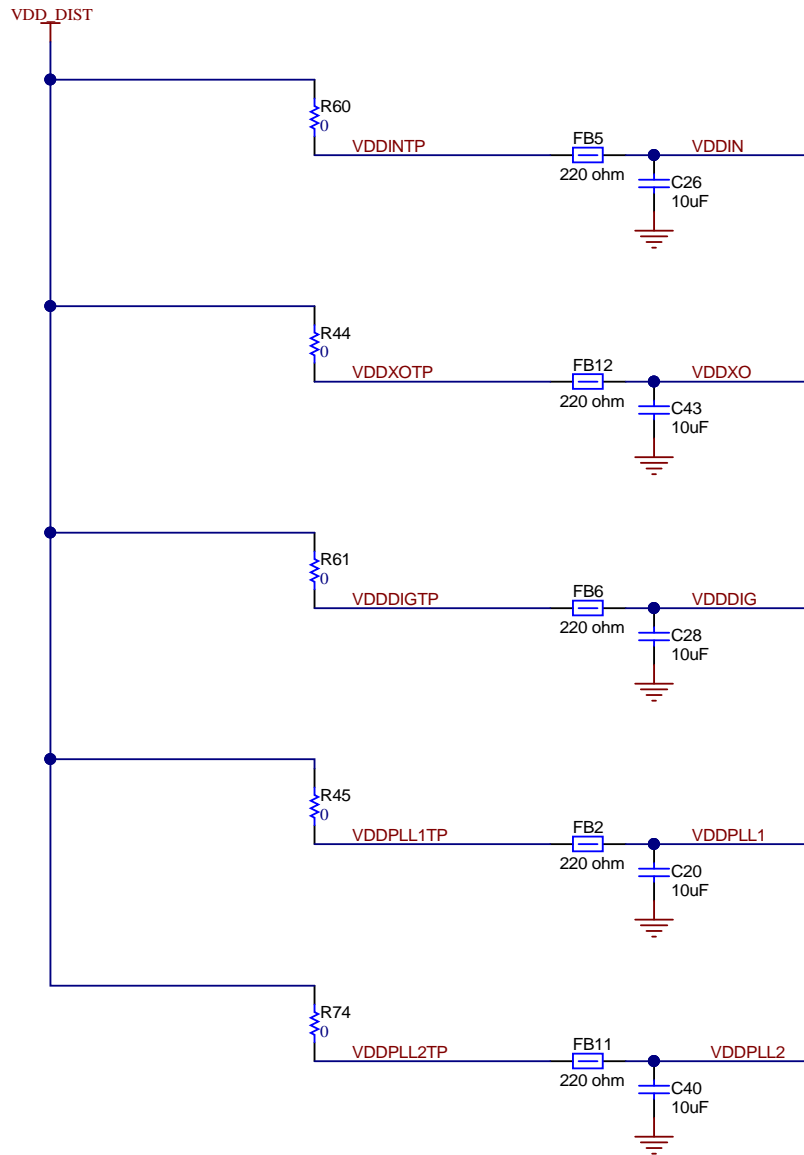
DUT VDD CORE POWER (3.3V)

DUT VDDO OUTPUT POWER (1.8-3.3V)

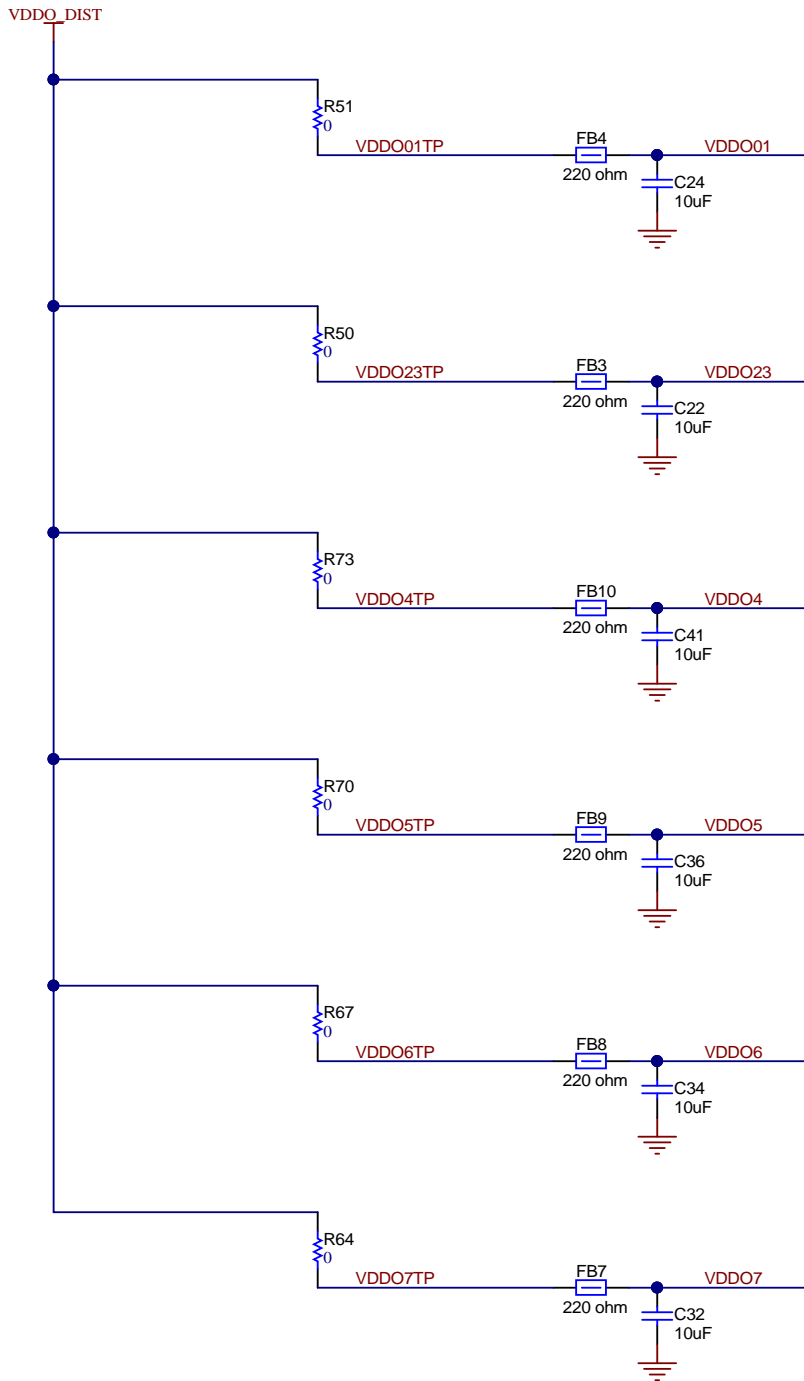
Orderable: LMK05318BEVM		Designed for: Public Release	Mod. Date: 3/26/2020
TID #: N/A		Project Title: LMK05318BEVM	
Number: HSDC086	Rev: A	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: 001	Sheet: 1 of 9
Drawn By:		File: HSDC086A_Power.SchDoc	Size: B
Engineer: Hao Zheng		Contact: http://www.ti.com/support	

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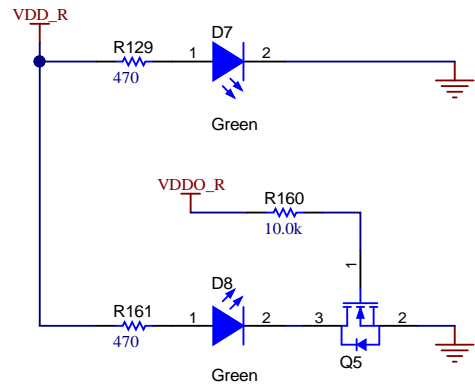
VDD CORE SUPPLY DIST & FILTERING



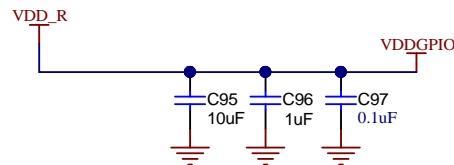
VDDO OUTPUT SUPPLY DIST & FILTERING



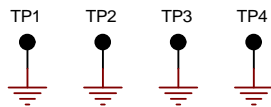
POWER LED INDICATORS



VDDGPIO



GND TEST POINTS



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A

B

C

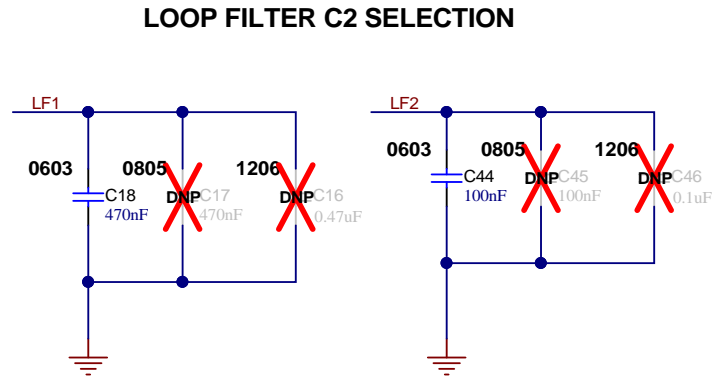
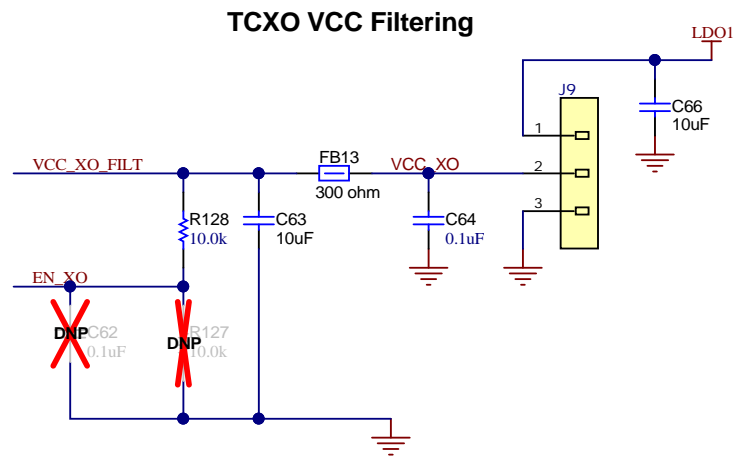
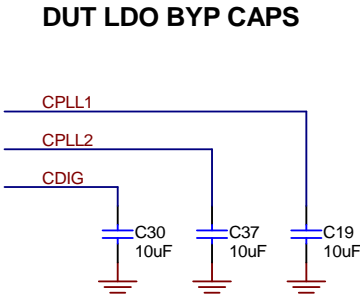
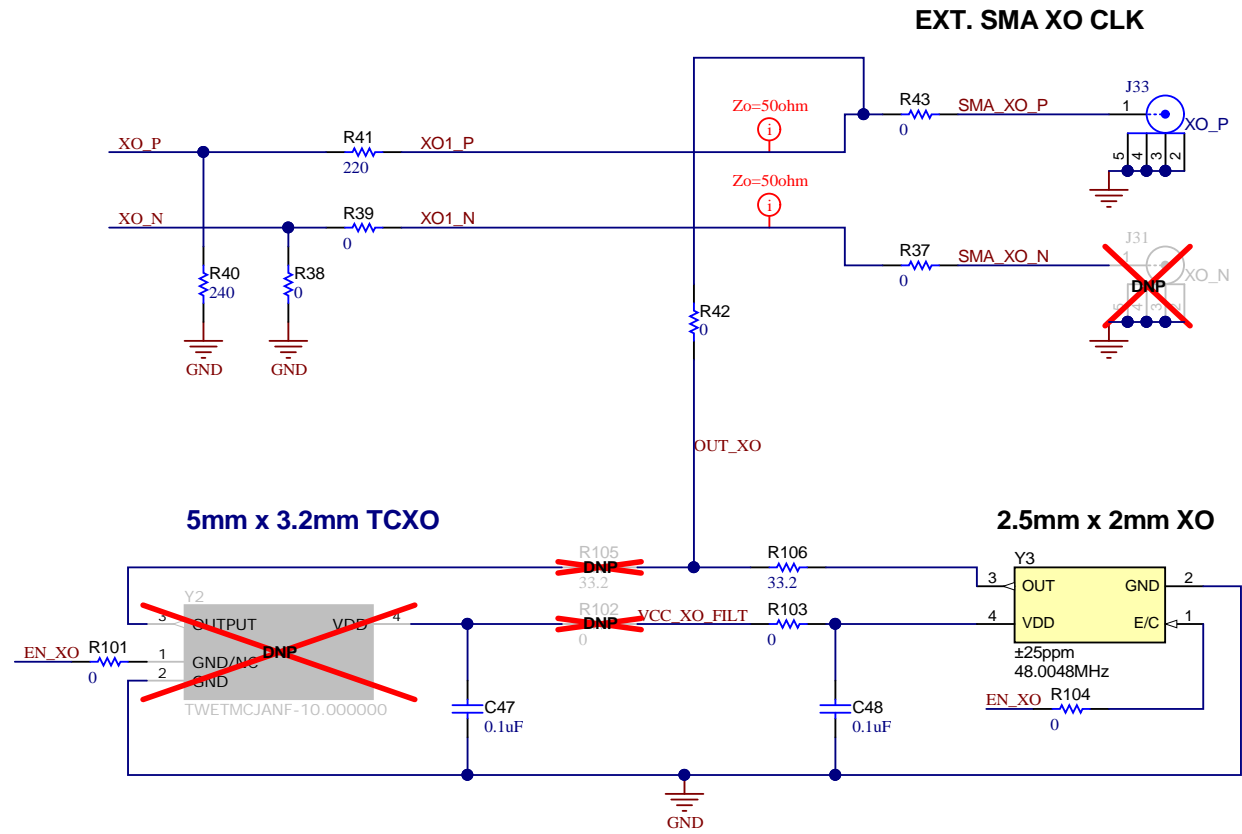
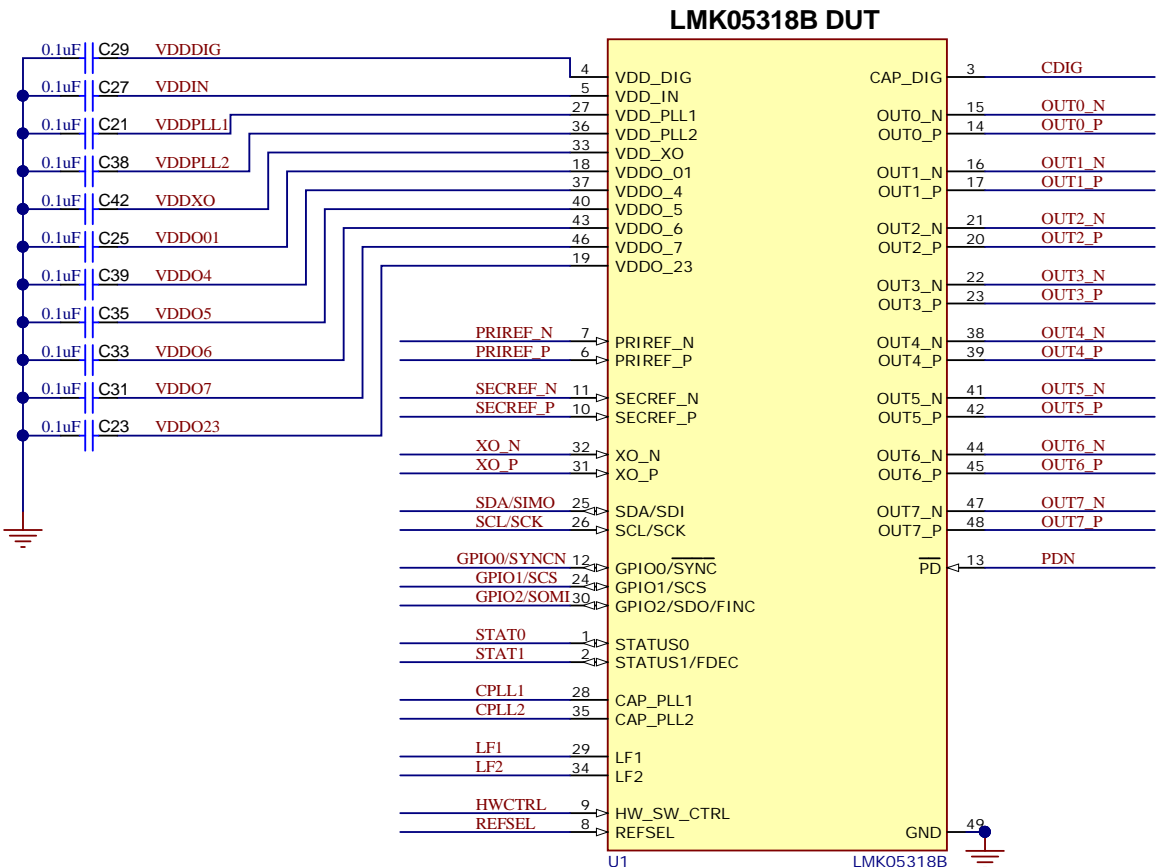
D

A

B

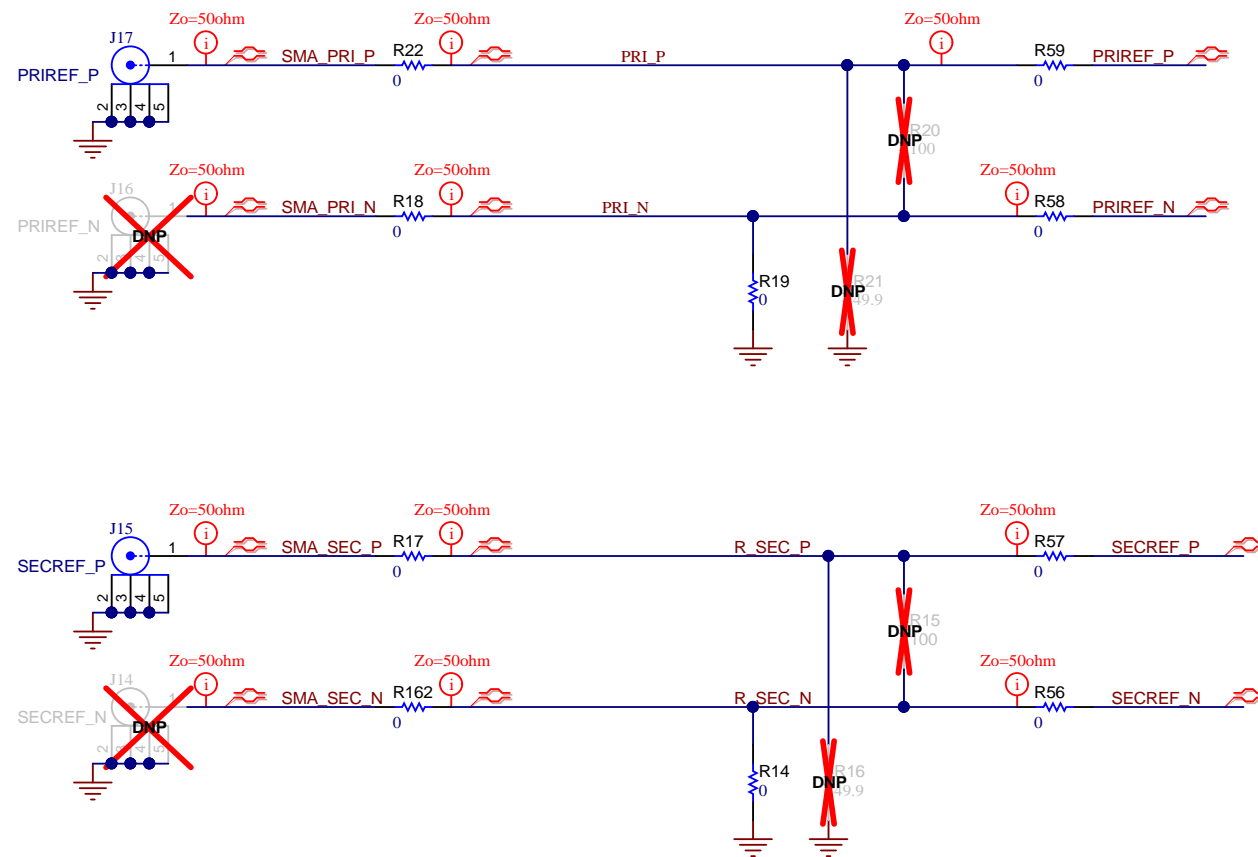
C

D



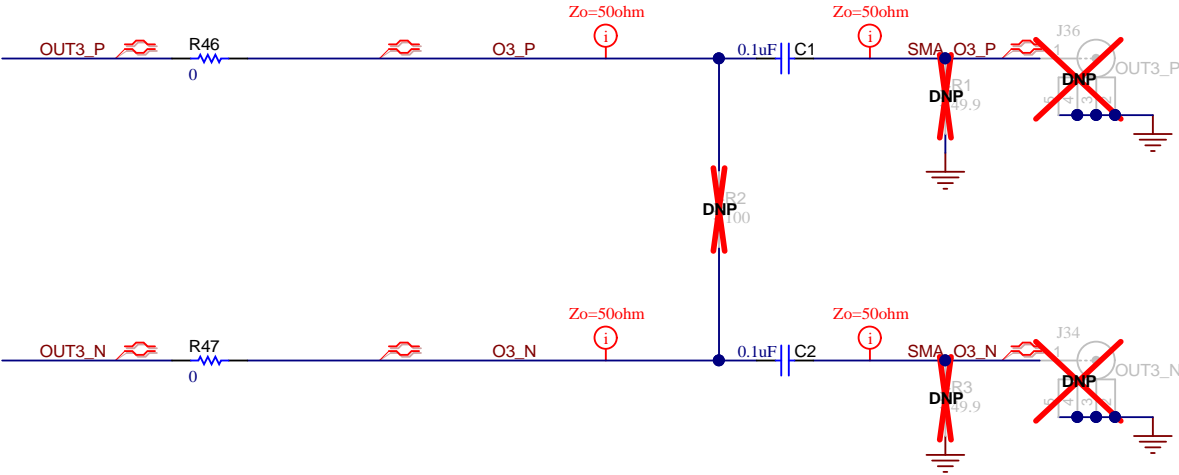
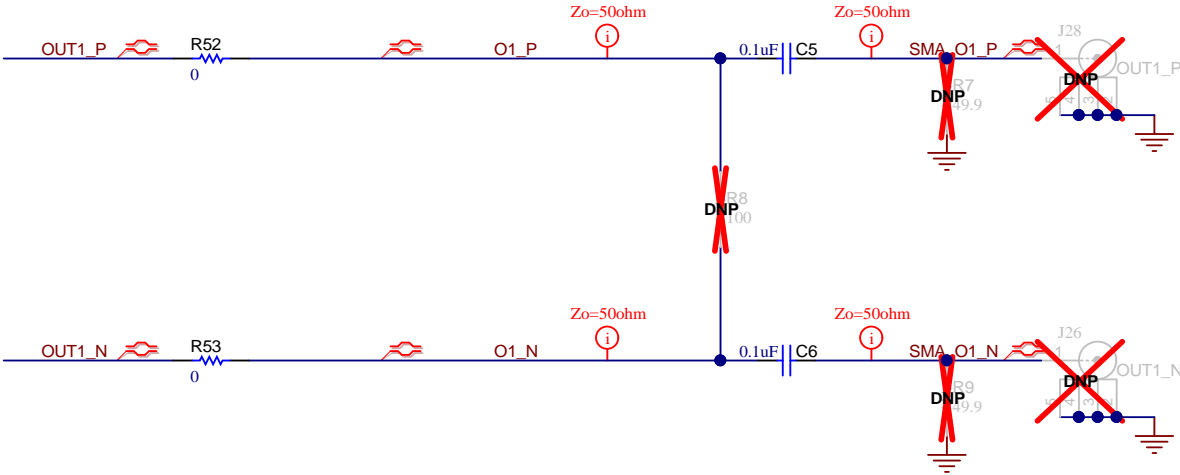
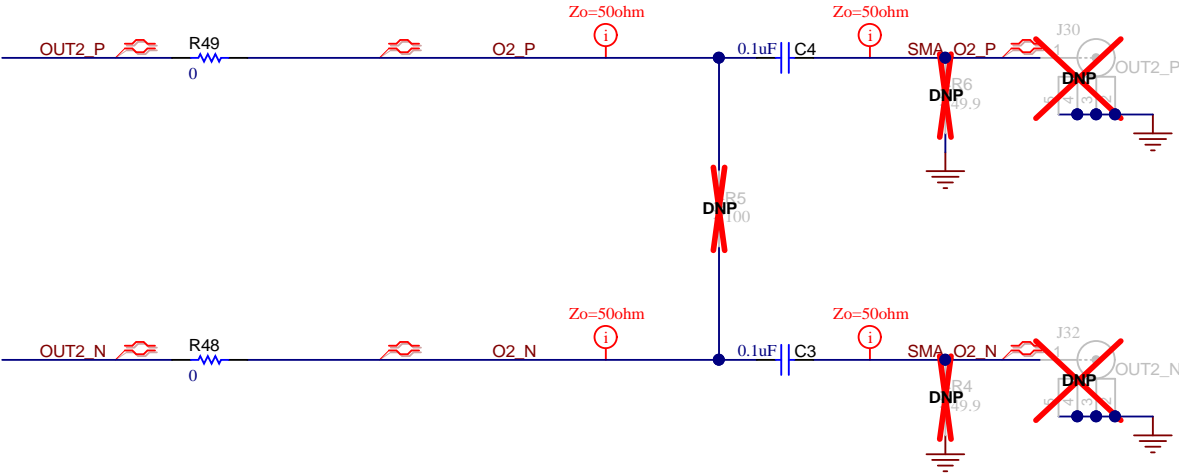
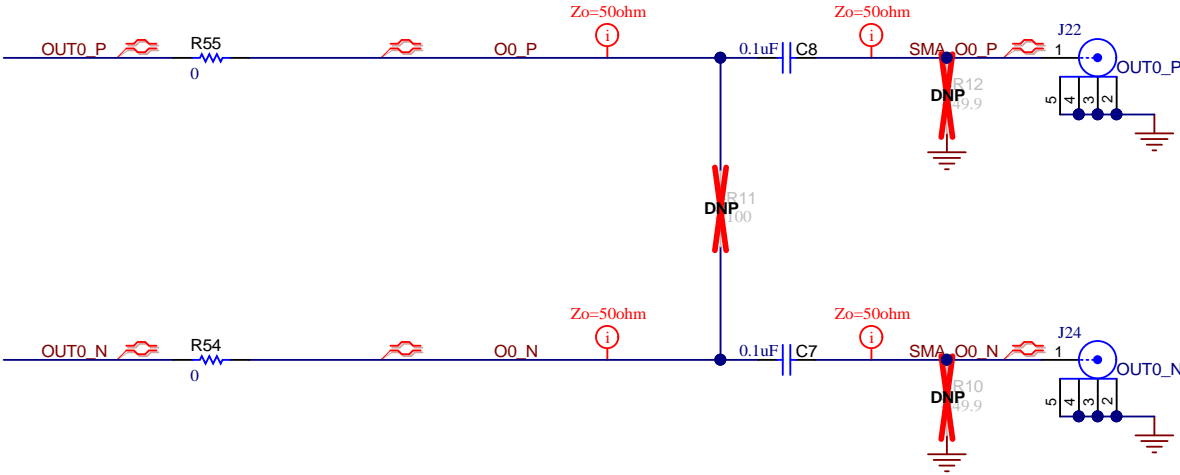
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PRIMARY AND SECONDARY CLOCK INPUTS



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Drawn By:	File: HSDC086A_ReferenceInput_SchDoc	Size: B	
Engineer: Hao Zheng	Contact: http://www.ti.com/support		

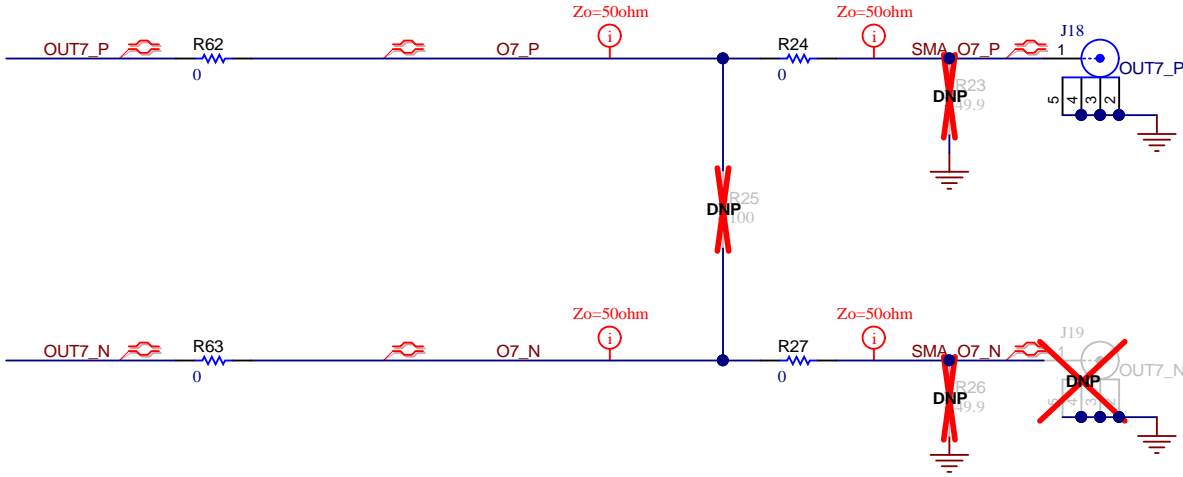
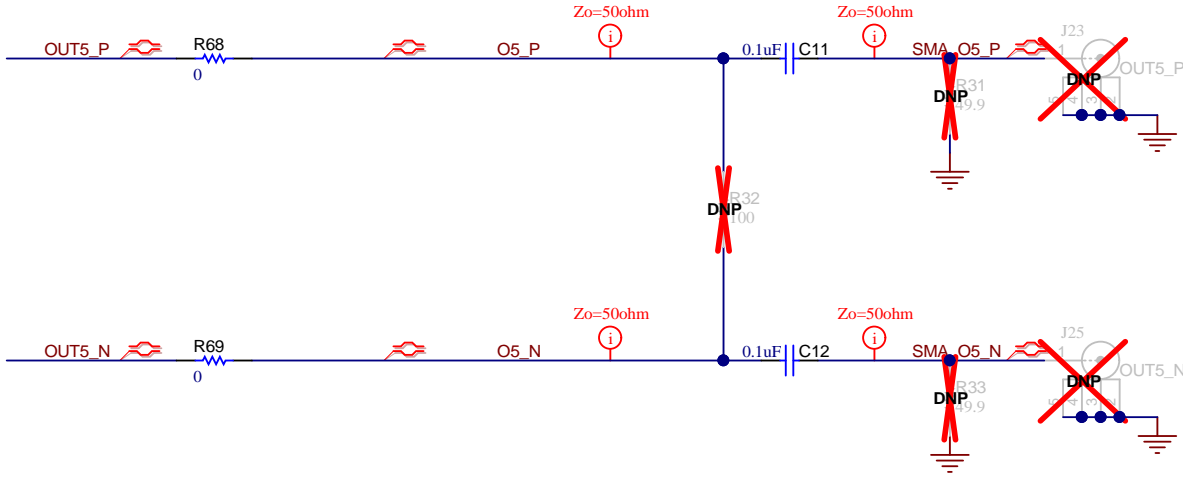
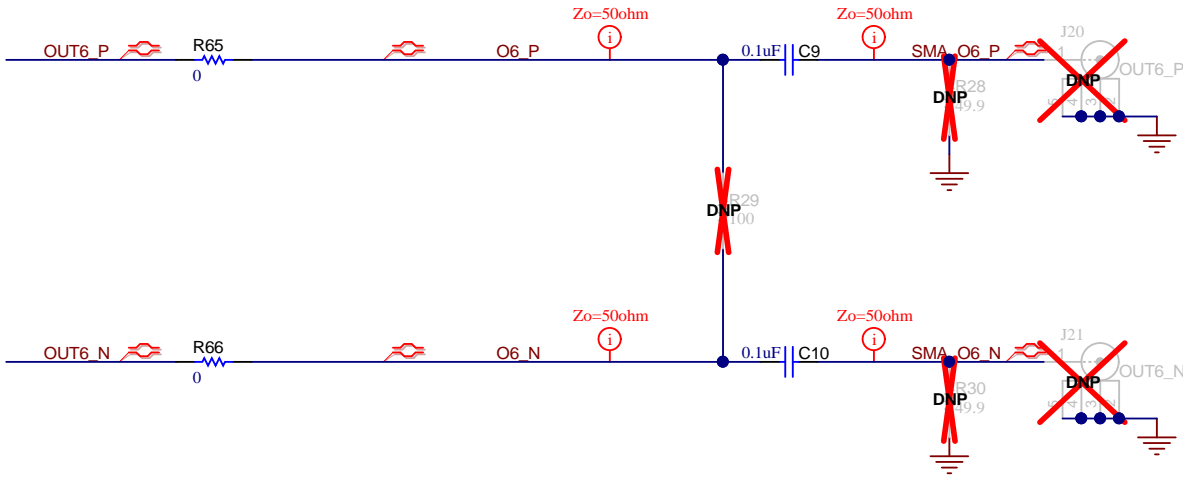
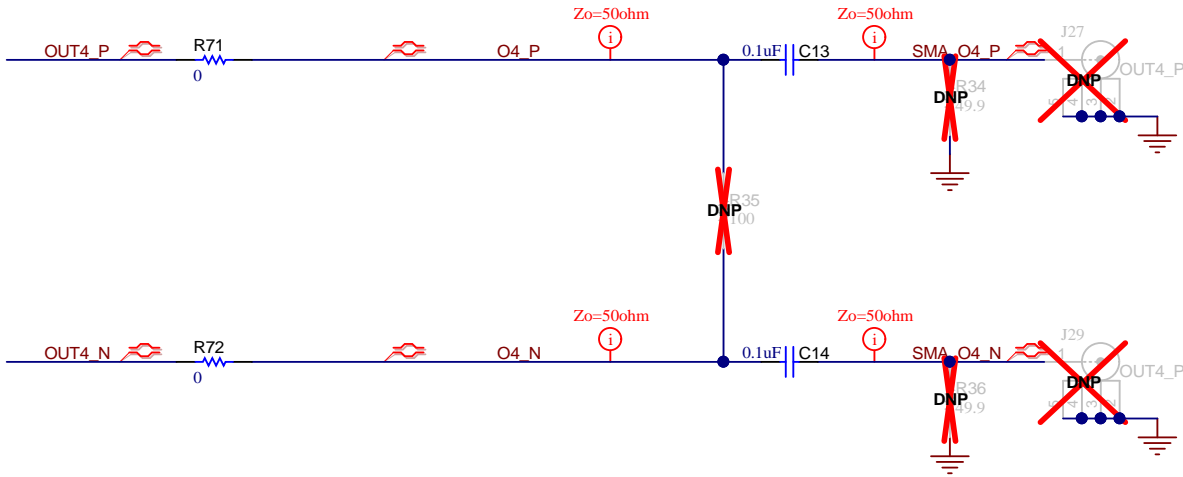
OUT0-OUT3 CLOCK OUTPUTS



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SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 5 of 9
Drawn By:	File: HSDC086A_OUT0-3.SchDoc	Size: B
Engineer: Hao Zheng	Contact: http://www.ti.com/support	

OUT4-OUT7 CLOCK OUTPUTS



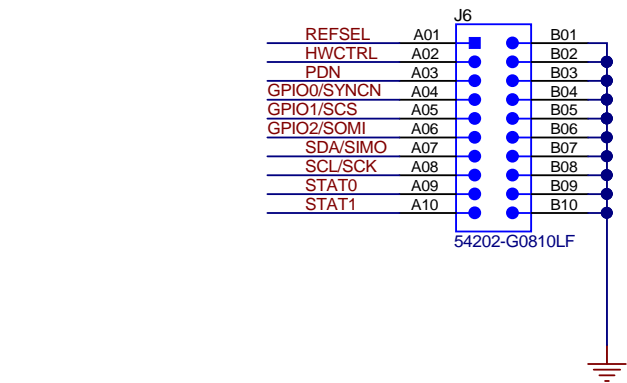
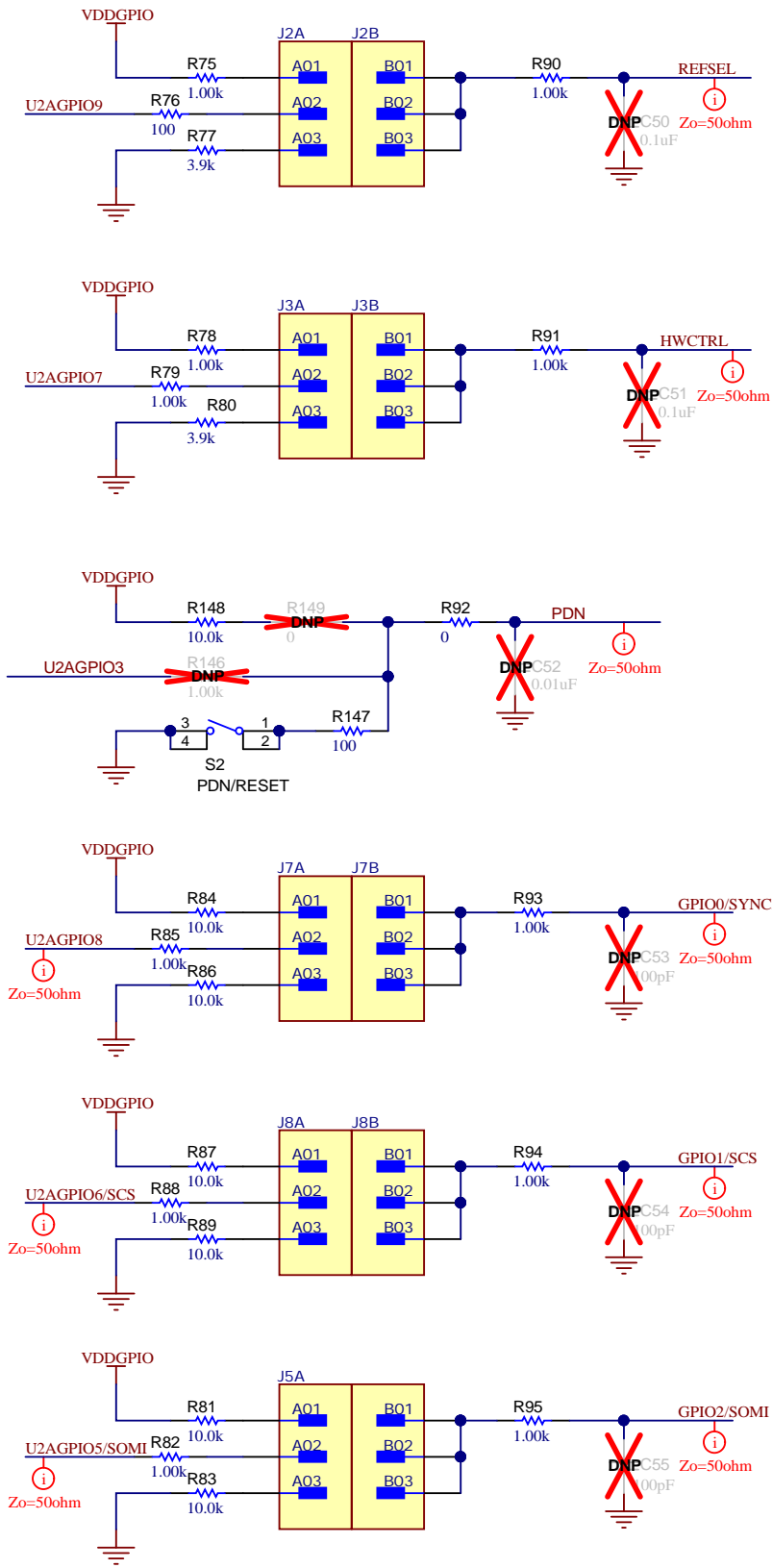
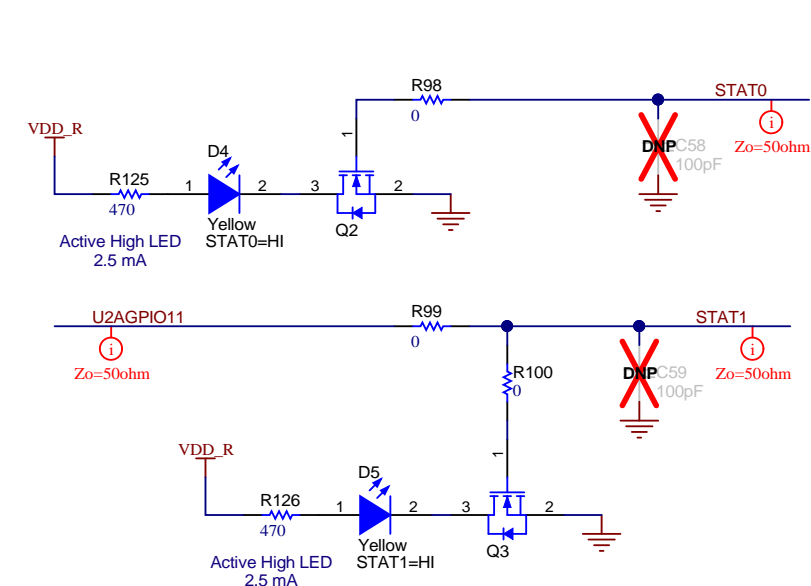
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SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 6 of 9
Drawn By:	File: HSDC086A_OUT4-7.SchDoc	Size: B
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LOGIC I/O INTERFACE

STATUS[0:1] LEDs

LOGIC I/O TEST POINTS



I2C/SPI INTERFACE

