I have three questions about the LMX1204.

Q1: Each time a "write to read" is performed in registers R9 and R16, a countdown occurs with a specific bit by 2 as follows.

- R9 bit9-0 LOGICLK\_DIV

When 0xB020 is written to read, 0xB01E is returned

Write to read 0xB01E, 0xB01C is returned

Write to read 0xB01C, 0xB01A is returned

....

- R16 bit11-0 SYSREF\_DIV

Writing to read 0x1027 returns 0x1025

Write to read 0x1025 returns 0x1023

Write to read 0x1023 returns 0x1021

....

When I try to read the result of writing in this way, I get a -2 down value. Is this expected result? And does the similar thing happen with the LMX1906-SP R9 and R16 too?

Q2: The reset value of register R29 bit7-0 VCO\_CAPCTRL differs between datasheet (0xFF) and evaluation board result (0x00). Is this a datasheet error? Also, the reset value of the similar part LMX1906-SP R29 bit7-0 is (0xFF) in the datasheet. Is this also correct?

Q3: The value of register R76 bit9-5 reserved differs between datasheet clause 7 (0x00) and evaluation board result (0x19). Is this a datasheet error? Also, the equivalent LMX1906-SP R76 bit9-5 is (0x00) in the datasheet. Is this correct at LMX1906-SP or it also should be (0x19) by right?

The above event has been confirmed on both the evaluation board (controlled by TICS Pro) and the in-house board (controlled by FPGA).