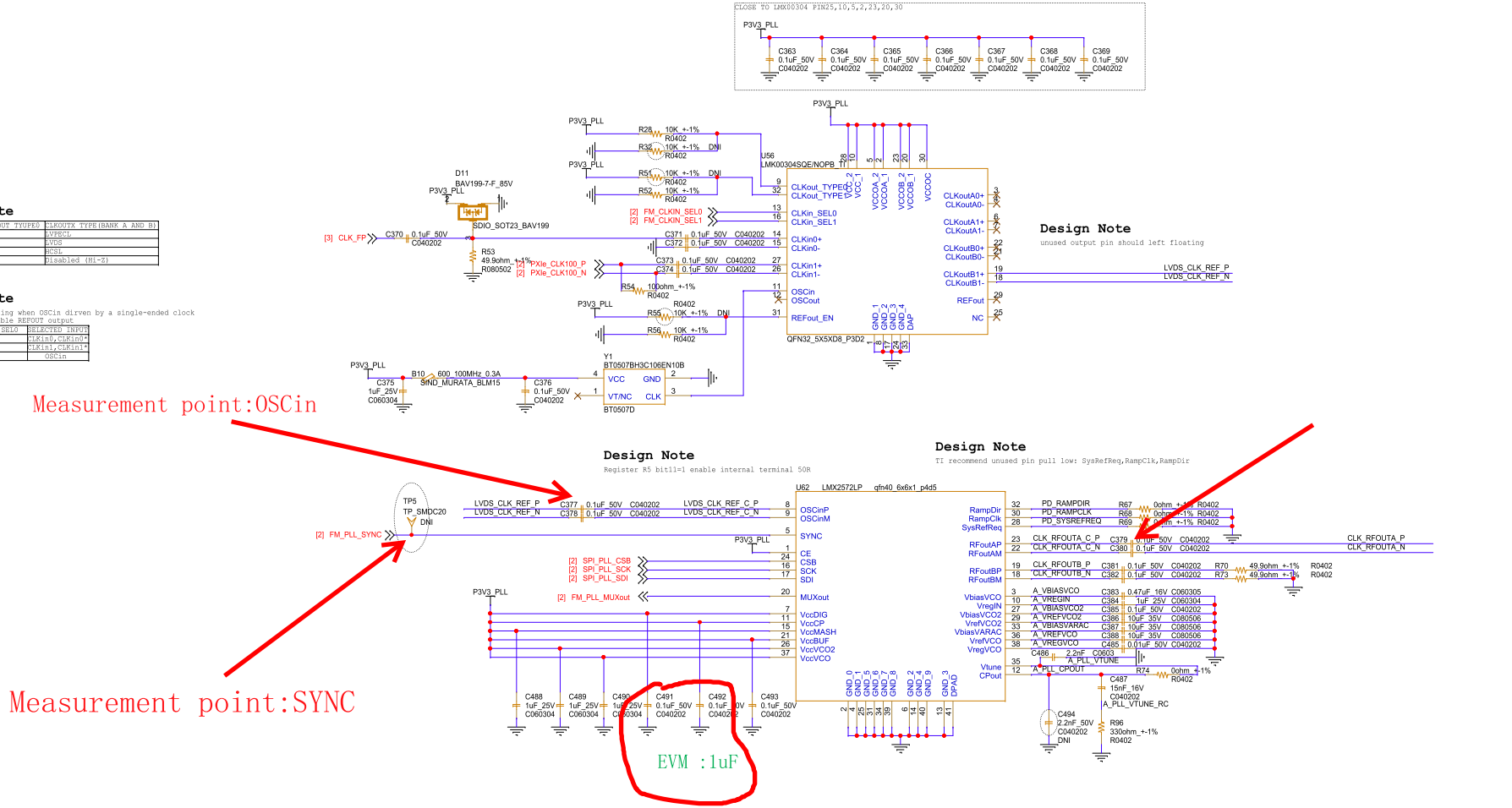
Design Note
CLKOUT TYUPE1 CLKOUT TYUPE0 CLKOUTX TYPE(BANK A AND B)
0 0 LVPECL
0 1 LVDS
1 0 HCSL
1 1 Disabled (Hi-Z)
Design Note
OSCout leave floating when OSCin dirven by a single-ended clock
REFout EN = 0 disable REFOUT output
CLKin SEL1 CLKin SEL0 SELECTED INPUT
0 0 CLKin0,CLKin0*
0 1 CLKin1,CLKin1*
1 X OSCin
Measurement point:OSCin
Design Note
unused output pin should left floating
Design Note
Register R5 bit11=1 enable internal terminal 50R
Design Note
TI recommend unused pin pull low: SysRefReq,RampClk,RampDir
Measurement point:SYNC
EVM :1uF
U56 LMK00304SQE/NOPB_T1
QFN32_5X5XD8_P3D2
U62 LMX2572LP qfn40_6x6x1_p4d5
BT0507D
LVDS_CLK_REF_P
LVDS_CLK_REF_N
CLK_RFOUTA_P
CLK_RFOUTA_N
CLOSE TO LMX00304 PIN25,10,5,2,23,20,30
CLOSE TO LMX00304 PIN25,10,5,2,23,20,31
Design Note
CLKOUT TYUPE1 CLKOUT TYUPE0 CLKOUTX TYPE(BANK A AND B)
0 0 LVPECL
0 1 LVDS
1 0 HCSL
1 1 Disabled (Hi-Z)
Design Note
OSCout leave floating when OSCin dirven by a single-ended clock
REFout EN = 0 disable REFOUT output
CLKin SEL1 CLKin SEL0 SELECTED INPUT
0 0 CLKin0,CLKin0*
0 1 CLKin1,CLKin1*
1 X OSCin
Design Note
unused output pin should left floating
U63 LMK00304SQE/NOPB_T1
U73 DS90LV028ATM
SOP8_1D27X6X1D75_D_1
CLK_LVDS_ADC_P
CLK_LVDS_ADC_N
CLK_LVDS_FPGA_P
CLK_LVDS_FPGA_N
CLK_LVDS_DAC_P
CLK_LVDS_DAC_N
CLK_DAC0_SCK
CLK_DAC1_SCK
Company
简仪科技 JYTEK
Designer
<Designer>
Title
DB-9511
Checker
<Checker>
Document Number
<Doc>
Rev
A2
Date: Friday, March 29, 2024
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