Application Report
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CDCI6214 and CDCE6214-Q1 design with crystal input

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ABSTRACT

CDCI6214 and CDCE6214-Q1 incorporate a crystal driver circuit that can drive an external crystal resonator (XTAL). Design procedures related to crystal input are explained in this article. Both CDCI6214 and CDCE6214-Q1 share the same crystal driver circuit. This appnote assumes basic understanding of crystal resonators and crystal oscillators.

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1 Introduction

A simplified circuit for crystal input is shown in Figure 1. A crystal in series with R_s is connected to Pin 1 and Pin 2 of CDCI6214 / CDCE6214-Q1, where R_s is series resistor used to reduce drive level. C_{L1} and C_{L2} are two single ended load capacitors used to control initial frequency accuracy of the crystal. -R is called "negative resistance". It's generated by the active circuit inside the chip and can effectively "cancel out" the positive resistance in order for the crystal to start and maintain oscillation.

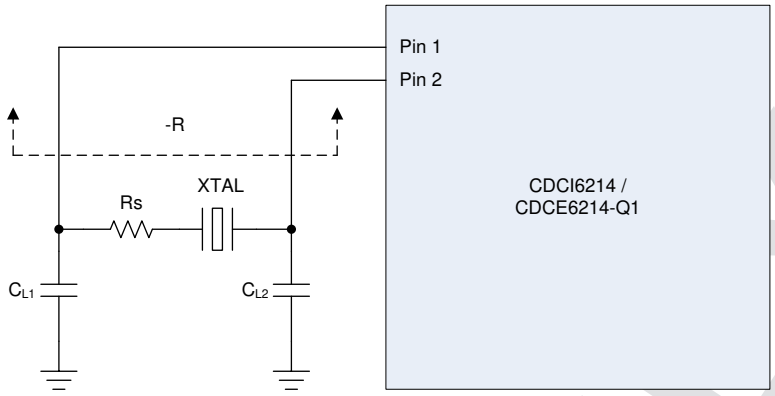

Figure 1. XTAL input schematic

The goals of crystal circuit design are:

1. To make sure that crystal oscillates. This requires the -R to be large enough to provide sufficient power for crystal to oscillate.
2. Not to overdrive the crystal. This requires the -R not to be so large that crystal is overdriven. The consequences of overdriving a crystal are reduced lifetime, accelerated aging and unwanted spurs. R_s is used to reduce power dissipation when drive level is too high. Crystal vendors typically specify maximum drive level which should not be violated.
3. To minimize crystal frequency error. Crystal vendors typically require load capacitance (C_L) of a certain value in order to achieve frequency accuracy. If C_L is too low, actual frequency will be higher than the target frequency, and vice versa.

Based on above discussion, in order to design a circuit for crystal input, designer needs to decide the value of R_s as well as C_{L1} and C_{L2}. Further, CDCI6214 / CDCE6214-Q1 provide controllable driver bias current and programmable internal load capacitance, which make the design much easier once the user understands how it works. This will be explained in detail in later sections.

2 Crystal circuit design description

2.1 Negative resistance and oscillation criteria

For a successful crystal circuit design, the first step is to make the crystal oscillate. This subsection explains the oscillation criteria of a crystal and how to design with sufficient margin. To start with, let's review the concepts of ESR (Equivalent Series Resistance) and negative resistance.

Shown in Figure 2, a crystal resonator can be modeled as an RLC circuit. An RLC circuit cannot start or maintain oscillation without external supply because motional resistance (R_m) is lossy and dissipates power. Therefore, an active network is needed for crystal to oscillate.

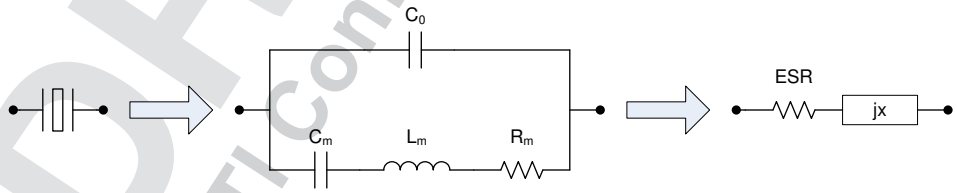

Figure 2. XTAL equivalent circuit

As mentioned before, a crystal driver provides an equivalent "negative resistance" (-R) to effectively eliminate the real part (ESR + R_s). Although *during* oscillation the total impedance is purely imaginary -- meaning that magnitude of -R is equal to ESR + R_s, in order for the XTAL to *start* oscillation, -R needs to be larger than that. A rule of thumb for an oscillator to start oscillating is:

$$abs(-R) = (3 \sim 5) * (ESR + R_s) \quad (1)$$

Meaning that the magnitude of -R should be 3 to 5 times larger than the real part of crystal + Rs. A factor of 3 is the minimum requirement. A factor of 5 is usually recommended for good margin.

ESR can be estimated using Equation 2, where C_0 is shunt capacitance shown in Figure 2. If R_m or C_0 values are unavailable, simply use the max ESR specified in crystal datasheet for a rough estimation.

$$ESR = R_m \left(1 + \frac{C_0}{C_L}\right)^2 \quad (2)$$

-R can be calculated using Equation 3, where ω is angular resonant frequency in rad/s, and g_m values for CDCI6214 / CDCE6214-Q1 are provided in Table 1.

$$-R = -\frac{g_m}{(2\omega C_L)^2} \quad (3)$$

Notice how -R is related to resonant frequency and load capacitance. The higher the frequency and the larger the C_L, the smaller the magnitude of -R, meaning that there is typically less margin of negative resistance at high frequency and with large load capacitance and vice versa.

Table 1. g_m table

R26[5:2] of CDCI6214 or R24[5:2] of CDCE6214-Q1	Bias Current (uA)	gm (mS)
0x0	0	NA
0x1	14	0.02
0x2	29	0.38
0x3	44	0.71
0x4	59	1.01
0x5	148	1.3
0x6	295	2.83
0x7	443	4.92
0x8	591	6.66
0x9	884	8.18
0xA	1177	10.7
0xB	1468	12.78
0xC	1758	14.53

Table 2 shows calculation results using common resonant frequencies (25MHz, 40MHz and 50MHz) and load capacitances (18pF, 12pF and 8pF) based on Equation 3 with a factor of 3. The max ESR of a crystal should not be higher than the numbers listed in this table. A factor of 4 or 5 is recommended for sufficient margin.

Keep in mind that the crystal driver starts to saturate when 1177uA or higher bias current is chosen. Equation 3 should only be applied to bias current below 1177uA. Avoid using 1468uA and 1758uA unless necessary, because with these bias currents, the magnitude of actual -R is lower than what is predicted using the equation. This will be better demonstrated with bench measurement results in later sections.

Table 2. Available negative resistance divided by 3

Bias current (uA)	C_L = 18pF			C_L = 12pF			C_L = 8pF		
	25MHz	40MHz	50MHz	25MHz	40MHz	50MHz	25MHz	40MHz	50MHz
295[(1)]	30	12	7	66	26	17	149	58	37
443	51	20	13	116	45	29	260	102	65
591	69	27	17	156	61	39	352	137	88
884	85	33	21	192	75	48	432	169	108
1177	112	44	28	251	98	63	565	221	141
1468	133	52	33	300	117	75	675	264	169

(1) Bias current below 295uA is not recommended, because phase noise performance with 148uA or lower is inferior. In general, phase noise performance achieves optimum at and above 295uA. It gets slightly better with increase of bias current.

Table 2. Available negative resistance divided by 3 (continued)

Bias current (uA)	C_L = 18pF			C_L = 12pF			C_L = 8pF		
	25MHz	40MHz	50MHz	25MHz	40MHz	50MHz	25MHz	40MHz	50MHz
1758	152	59	38	341	133	85	768	300	192

2.2 Rs, bias current and drive level

According to Table 1 and Table 2, higher bias current provides larger g_m, and hence more negative resistance and more margin for max ESR. Then why not choose the maximum bias current? Because higher bias current also means higher drive level, and as mentioned earlier, if drive level is too high, it will lead to reduced lifetime, accelerated aging and unwanted spurs. In this subsection, we will discuss how to control the drive level so that it is within the max drivel level specified in crystal datasheet (typicall 100uW or 200uW). To start with, let's review the concept of drive level and the effect of Rs.

Drive level is the amount of power dissipated in a crystal. It is calculated using:

$$DL = I_{rms}^2 ESR \quad (4)$$

Where I_{rms} is the RMS current flowing through the crystal. It can be measured using a current probe with crystal deadbugged or flywired. ESR should be calculated using Equation 2. Max ESR in the datasheet is not acceptable for drivel level calculation because it may lead to a much larger value that the actual one. A series resistor R_s can decrease the drive level because I_{rms} is reduced while ESR is unchanged. However, there is hardly any equation that can predict the relationship between R_s and I_{rms} because it is very much dependent on the internal driver circuit which is not disclosed to users. Most of the times board designers either do trial and error or do not know whether or not the crystal has been overdriven at all.

Fortunately, the crystal driver of CDCI6214 / CDCE6214-Q1 was designed in a way such that no R_s is needed. The programmable bias current makes sure that drivel level can be controlled within an acceptable range. An example measurement was done using a certain family of crystals (similar C_0 and R_m across frequency). Drive level vs bias current for 25MHz and 50MHz crystal are shown in Table 3 and Table 4. Note that drive level measured with these crystals is quite high, because the R_m of the crystal is very low and C_0 is small, resulting in a small ESR. For crystals with higher ESR, the drive level may be lower.

Table 3. Drive Level vs Bias Current With 25MHz crystal

Bias current (uA)	R_m (Ω)	C_0 (pF)	C_L (pF)	ESR (Ω)	3.3V		1.8V	
					I_{rms} (mA)	Drive level (uW)	I_{rms} (mA)	Drive level (uW)
295	12.6	1.3	8.0	17.0	1.9	59.2	1.8	52.6
443	12.6	1.3	8.0	17.0	2.3	91.2	1.9	64.7
591	12.6	1.3	8.0	17.0	2.7	122.2	2.2	84.6
884	12.6	1.3	8.0	17.0	2.9	144.6	2.7	126.1
1177	12.6	1.3	8.0	17.0	2.9	146.7	2.8	136.2
1468	12.6	1.3	8.0	17.0	2.8	136.2	2.8	136.2
1758	12.6	1.3	8.0	17.0	2.7	128.1	2.8	136.2

Table 4. Drive level vs bias current with 50MHz crystal

Bias current (uA)	R_m (Ω)	C_0 (pF)	C_L (pF)	ESR (Ω)	3.3V		1.8V	
					I_{rms} (mA)	Drive level (uW)	I_{rms} (mA)	Drive level (uW)
295	13.4	1.3	8.0	18.1	1.1	20.8	0.4	3.3
443	13.4	1.3	8.0	18.1	1.4	37.3	1.1	22.5
591	13.4	1.3	8.0	18.1	1.9	67.3	1.3	29.9
884	13.4	1.3	8.0	18.1	2.4	108.1	1.5	39.6

Table 4. Drive level vs bias current with 50MHz crystal (continued)

Bias current (uA)	R_m (Ω)	C_0 (pF)	C_L (pF)	ESR (Ω)	3.3V		1.8V	
					I_{rms} (mA)	Drive level (uW)	I_{rms} (mA)	Drive level (uW)
1177	13.4	1.3	8.0	18.1	2.7	134.1	1.6	49.3
1468	13.4	1.3	8.0	18.1	2.8	147.1	1.8	60.1
1758	13.4	1.3	8.0	18.1	2.9	156.1	2.0	70.4

Since no R_s is required, drive level should typically fall below 100uW automatically once a proper bias current is selected based on negative resistance needed. Even if drive level is somehow higher than the crystal limit, it can be easily reduced by adjusting bias current.

2.3 Load capacitance

Crystal vendors require a specific load capacitance value in order for the resonator to resonate with minimal frequency error. C_L is defined as equivalent capacitance seen by the crystal. Shown in Figure 3, C_L consists of three parts: external load capacitance (C_{L1} and C_{L2}), internal load capacitance (C_{int_L1} and C_{int_L2}) and stray capacitance (C_{stray}) that includes all kinds of pin and PCB parasitics.

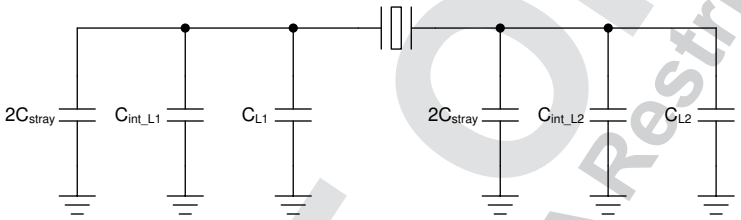

Figure 3. Load capacitance illustration diagram

The equivalent capacitance seen by XTAL is (C_{int_L1} in series with C_{int_L2}) in parallel with (C_{L1} in series with C_{L2}) in parallel with C_{stray}. Therefore, C_L can be calculated using:

$$C_L = \frac{C_{L1}C_{L2}}{C_{L1}+C_{L2}} + \frac{C_{int\_L1}C_{int\_L2}}{C_{int\_L1}+C_{int\_L2}} + C_{stray} \quad (5)$$

C_{int_L1} is equal to C_{int_L2}, and normally, C_{L1} and C_{L2} are also equal. Therefore, above equation can be simplified to:

$$C_L = \frac{C_{L1}}{2} + \frac{C_{int\_L1}}{2} + C_{stray} \quad (6)$$

Programmable C_{int_L1} and C_{int_L2} are controlled by R26[12:8] of CDCI6214 or R24[12:8] of CDCE6214-Q1. Generally, it is recommended to first estimate the stray capacitance, calculate the sum of extra load capacitance needed, then make external load capacitance lower than that value in case the stray capacitance is higher than estimated. If the load capacitance turns out to be lower, then fine tune it using programmable internal load capacitance.

For example, if required load capacitance is 12pF and PCB stray capacitance is estimated to be 3pF, then 9pF of extra capacitance is needed. Set C_{L1} and C_{L2} to 12pF so that there is still 3pF margin. Fine tune the capacitance using internal load cap.

3 Bench measurement examples

In this section, we use bench measurement results to verify Equation 1 and Equation 3. To do so, measure the maximum series resistance with which the crystal can start oscillating, then add to that the ESR of the crystal. The result is the max acceptable ESR with 0 margin.

Table 5. Measured maximum ESR to start oscillation

Bias current (uA)	Measured maximum ESR (Ω)								
	CL = 18pF			CL = 12pF			CL = 8pF		
	25MHz	40MHz	50MHz	25MHz	40MHz	50MHz	25MHz	40MHz	50MHz
295	45	NA(1)	NA(1)	85	45	23	215	75	40
443	65	27	17	135	55	35	335	120	65
591	85	30	19	165	85	43	415	145	90
884	105	33	21	255	100	53	515	185	100
1177	135	37	23	315	115	55	615	220	105
1468	135	41	25	315	120	56	615	225	115
1758	135	43	27	315	120	57	615	225	120

(1) Crystal does not oscillate.

Comparing Table 5 with Table 2, it can be found that the numbers predicted in Table 2 are quite accurate but not with much margin. That's why a factor of 4 or 5 is recommended considering process, voltage and temperature variation.

Notice how available negative resistance stops increasing or increases slowly beyond 1177uA because of crystal driver saturation.

4 Design procedures summary

1. Set R_s = 0. Based on information provided in Section 2.1, determine the negative resistance value and find out the bias current that can provide that.
2. According to Section 2.3, set internal and external load capacitance.
3. After the board is built, send it to crystal vendor to generate a test report. Make sure that -R is 3~5 times of *measured* ESR and drive level is less than what is specified in the crystal datasheet. Adjust the bias current if necessary. Measure the output frequency. Fine tune the frequency by adjusting the internal load cap. Increment frequency by reducing load cap and decrement the frequency by increasing the load cap.

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